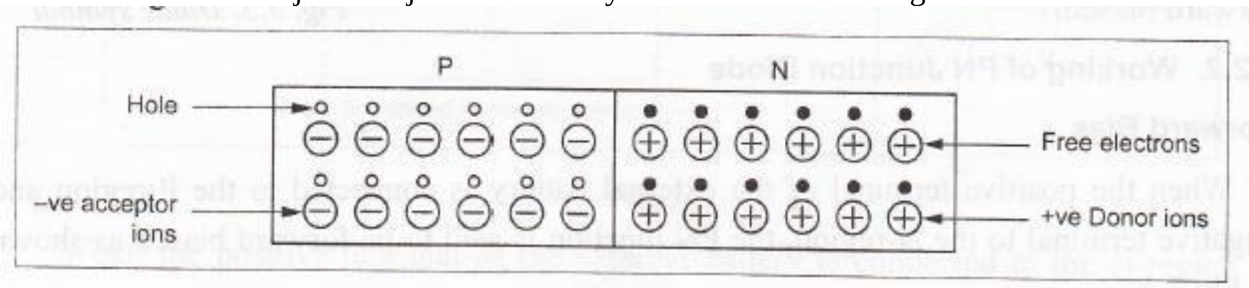
EC3353-ELECTRONIC DEVICES AND CIRCUITS
UNIT-I PN JUNCTION DEVICES
PART - B

PN junction diode: structure, operation & V-I characteristics

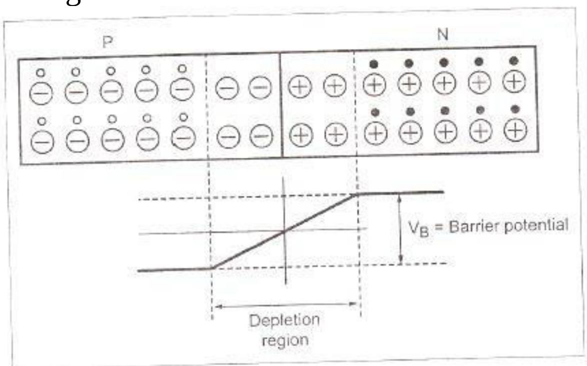
1. With a neat diagram explain the working of a PN junction diode in forward bias And reverse bias and show the effects of temperature on its VI characteristics (NOV/DEC 2012), (May / June 2016), (Nov / Dec 2015)
(OR)
Outline the charge carrier diffusion phenomenon across a PN junction. Explain the effect of forward and reverse biasing on the depletion region. (Nov/Dec 2018 R-13) (April / May 2019-R17)

A **PN junction** is formed from a piece of semiconductor (Ge or Si) by diffusing p-type material (Acceptor impurity Atoms) to one half side and N type material to (Donar Impurity Atoms) other half side. The plane dividing the two zones is known as 'Junction'.

The P-region of the semiconductor contains a large number of holes and N region, contains a large number of electrons. A PN junction just immediately formed is shown in Fig.

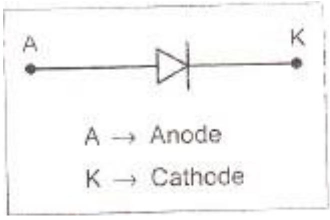


When PN junction is formed, there is a tendency for the electrons in the N-region to diffuse into the p-region, and holes from P-region to N-region. This process is called diffusion. While crossing the junction, the electrons and holes recombines with each other, leaving the immobile ions in the neighborhood of the junction neutralized as shown in Fig.



These immobile + ve and –ve ions, set up a potential across the junction. This potential is called potential barrier or junction barrier. Due to the potential barrier no further diffusion of electrons and holes takes place across the junction. Potential barrier is defined as a potential difference built up across the PN junction which restricts further movement of charge carriers across the junction. The potential barrier for a silicon PN junction is about 0.7 volt, whereas for Germanium PN junction is approximately 0.3 volt.

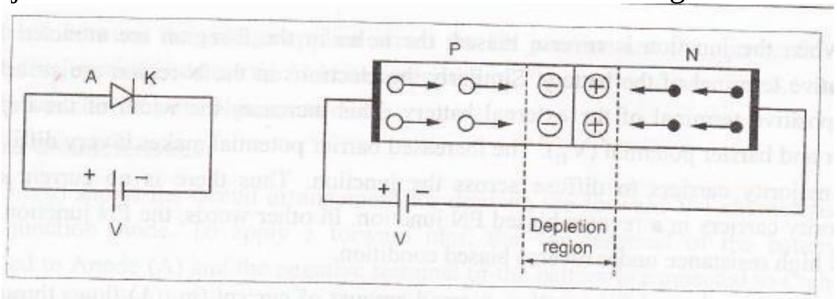
Symbol of Diode:
The symbol of PN junction diode is shown in Fig. The P-type and N-type regions are referred to as Anode and Cathode respectively. The arrowhead shows the conventional direction of current flow when the diode is forward biased.



Working of PN Junction Diode:

Forward Bias:

When the positive terminal of the external battery is connected to the P-region and negative terminal to the N-region, the PN junction is said to be forward biased as shown in Fig.

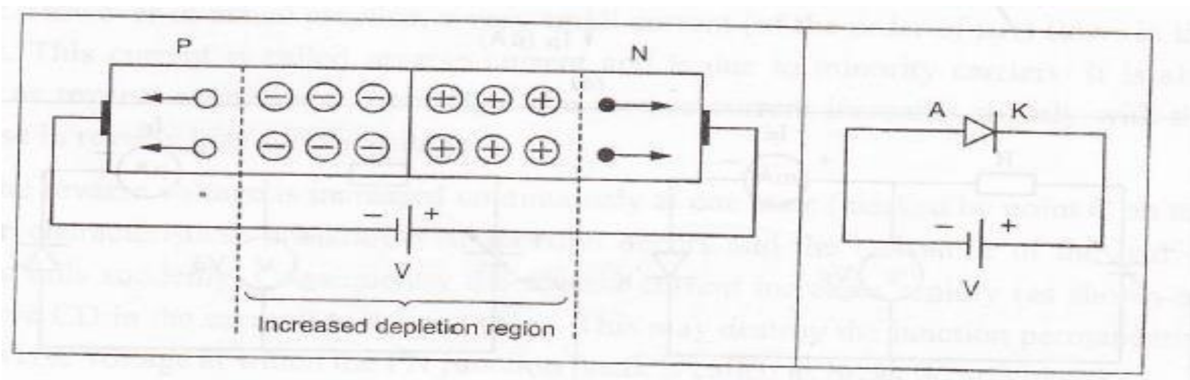


When the junction is forward biased, the holes in the p-region are repelled by the positive terminal of the battery and are forced to move towards the junction. similarly, the electrons in the N-region are repelled by the negative terminal of the battery and are forced to move towards the-junction.

This reduces the width of the depletion layer and barrier potential. If the applied voltage is greater than the potential barrier v_r, then the majority carriers namely holes in P-region and electrons in N-region, cross the barrier. During crossing some of the charges get neutralized the remaining charges after crossing, reach the other side and constitute current in the forward direction. The PN junction offers very low resistance under forward biased condition.

Since the barrier potential is very small (nearly 0.7 V for silicon and 0.3 V for Germanium junction), a small forward voltage is enough to completely eliminate the barrier. once the potential barrier is eliminated by the forward voltage, a large current start flowing through the PN junction.

Reverse Bias:

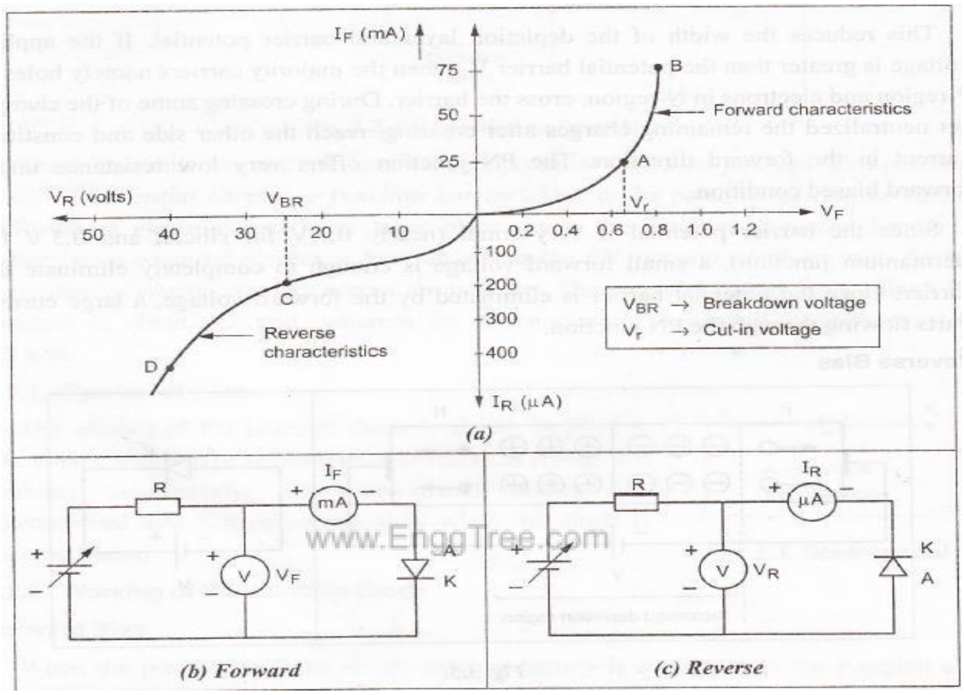


When the positive terminal of the external battery is connected to the N-region and negative terminal to the p-region, the PN junction is said to be reverse biased. When the junction is reverse biased, the holes in the P-region are attracted by the negative terminal of the battery. Similarly, the electrons in the N-region are attracted by the positive terminal of the external battery. This increases the width of the depletion layer and barrier potential (Vs).

The increased barrier potential makes it very difficult for the majority carriers to diffuse across the junction. Thus, there is no current due to majority carriers in a reverse biased PN junction. In other words, the PN junction offers very high resistance under reverse biased condition.

In a reverse biased PN junction, a small amount of current (in µA) flows through the junction because of minority carriers. (i.e., electrons in the P-region and holes in the N region).The reverse current is small because the number of majority carrier in both regions is small.

V-l characteristics of PN-Junction Diode:



A graph between the voltage applied across the PN junction and the current flowing through the junction is called the V-I characteristics of PN junction diode. Fig. shows the V-I characteristics of PN junction diode.

Forward Characteristics:

Fig. (a) shows the circuit arrangement for drawing the forward V-I characteristics of PN junction diode. To apply a forward bias, the +ve terminal of the battery is connected to Anode (A) and the negative terminal of the battery is connected to Cathode (K). Now, when supply voltage is increased the circuit current increases very slowly and the curve is nonlinear (region-OA).

The slow rise in current in this region is because the external applied voltage is used to overcome the barrier potential (0.7 V for Si; 0.3V for Ge) of the PN junction' However once the potential barrier is eliminated and the external supply voltage is increased further, the current flowing through the PN junction diode increases rapidly (region AB). This region of the curve is almost linear. The applied voltage should not be increased beyond a certain safe limit, otherwise the diode will burnout.

The forward voltage at which the current through the PN junction starts increasing rapidly is called by **knee voltage**. It is denoted by the letter V_B.

Reverse Characteristics:

Fig (b) shows the circuit arrangement for drawing the reverse V-I characteristics of PN junction diode. To apply a reverse bias, the +ve terminal of the battery is connected to cathode (K) and - ve terminal of the battery is connected to anode (A).

Under this condition the potential buried at the junction is increased. Therefore, the junction resistance becomes very high and practically no. current flows through the circuit. However, in actual practice, a very small current (of the order of µA) flows in the circuit. This current is called reverse current and is due to minority carriers. It is also called as reverse saturation current (I). The reverse current increases slightly with the increase in reverse bias supply voltage.

If the reverse voltage is increased continuously at one state (marked by point C on the reverse characteristics) breakdown of junction occurs and the resistance of the barrier regions falls suddenly. Consequently, the reverse current increases rapidly (as shown by the curve CD in the current) to a large value. This may destroy the junction permanently. The reverse voltage at which the PN junction breaks is called as break down voltage.

Temperature effects

The cut in voltage decreases as the temperature increases. The reverse saturation current increases.

$I_{02} = 2^{(\Delta T/10)} I_{01}$

I_{01}, I_{02} are the reverse current at T_1°C, T_2°C

$\Delta T = T_2 - T_1.$

The voltage equivalent of temperature V_T also increases. The reverse breakdown voltage increases.

2. Derive the PN diode current equation.

The applied voltage and current though diode are related by the equation

$$I = I_0 \left(e^{V/yV_T} - 1\right)$$

Where,

Io = Reverse saturation current
V = Applied voltage
I = Diode current
VT = Volt equivalent temperature

$$V_T = \frac{\bar{k}T}{q}$$

$\bar{k} = 1.38 \times 10^{-23}$ J/K
T = temperature of the diode junction
I = diode current
Q = change of electron 1.602×10^{-19} C
At any temperature

$$V_T = \frac{kT}{q} = \frac{1.38 \times 10^{-23}}{1.602 \times 10^{-19}} = \frac{T}{11600}$$

At room temperature

$$V_T = \frac{300}{11600} = 26mV$$

The value of η=1 for germanium and 2 for silicon.

For forward bias voltage the current equation reduces to

$$I = I_0\,(e^{V/yV_T})$$

At room temperature for germanium transistor

$$I = I_0(e^{40})$$

When the diode is reverse biased

$$I = I_0\,(e^{V/yV_T} - 1)$$

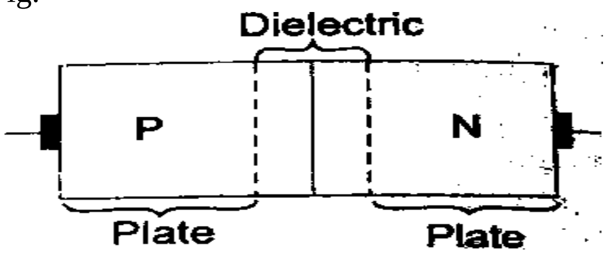
$$I \cong I_0$$

<u>Diffusion and transient capacitance</u>

3. Explain diffusion and transition capacitance of diode

Depletion layer capacitance (or) transition capacitance (or) space charge capacitance (May / June 2016)(Nov/Dec 2016)(May 2017)

• When a PN junction is reverse biased, a layer of positive and negative immobile ions, called depletion layer, is formed on either side of the junction. It is also known as depletion-region, space-charge region or transition region. The depletion-layer acts as a dielectric *(i.e.,* non-conductive) medium between P-region and N-region. We know that the P-region and N-region on either side of the junction, has a low resistance. Therefore, these regions act as two plates of a capacitor, separated by a dielectric *(i.e.,* depletion layer) as shown in Fig.



The capacitance formed in a junction area is called depletion layer capacitance. It is also called depletion region-capacitance, space charge capacitance, transition region capacitance or simply junction capacitance.

• Since the depletion layer width *(d)* increases with the increase in reverse bias voltage, the resulting depletion layer capacitance will decrease with the increased reverse bias.

• The depletion layer capacitance depends upon the nature of a PN junction, semiconductor material and magnitude of the applied reverse voltage. It is given by the relation,

$$C_T = \frac{K}{(V_B - V)^n}$$

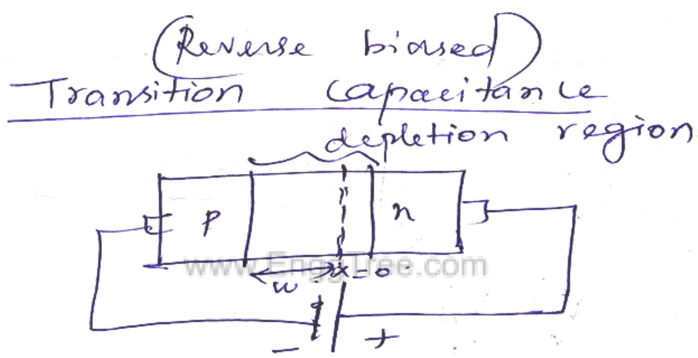
Where
K = A constant, depending upon the nature of semiconductor material
VB = barrier voltage. 0.6V for silicon and 0.3V for germanium
V = applied reverse voltage
n a constant depending upon the nature of junction.
The value of the K is

$$K = A \times \frac{\epsilon . q}{2}\left(\frac{N_A . N_D}{N_A + N_D}\right)$$

• The value of 'n' is taken as 1/2 for step or abrupt junction, 1/3 for linearly graded junction.

• It is the evident from the above relation that the value of depletion layer capacitance (CT) can be controlled by varying the applied reverse voltage. This property of variable capacitance, possessed by reverse biased PN junction, is used in the concentration of a device called varactor.
Reverse biased.

Derivation:



Connection P side is less
Doping less in P side (N_A)
N side (N_D)
Potential & change density Relation

$$N_A < N_D \frac{d^2V}{dx^2} \text{---------------} 1$$

X – distance measured from junction

$$\varepsilon \rightarrow \varepsilon_o \varepsilon_r$$

$$N_A < N_D \frac{d2V}{dx^2} = \frac{qND}{s} \text{----------------} 2$$

Integrating 2

$$\int \frac{d^2V}{dx^2} = \int \frac{qN_D}{\varepsilon}$$

$$\frac{dv}{dx} = \frac{qN_AX}{\varepsilon}$$

To get potential from 0 to w

$$\int_o^{V_B} \frac{dv}{dx} = \int_o^{w} \frac{qN_AX}{\varepsilon} dx$$

Where $V=V_B$

X=w

$$V_B = \frac{qN_A}{s} \times \frac{w^2}{2} \text{-------------------------} 3$$

$$W=\sqrt{V_B}$$

Q=No of change particle × change on each particle

=(N_A × volume) × q

$Q=qN_AAW$.............................2

Diff 3 w.r.to V

$$V_B = \frac{qN_A}{\varepsilon} \times \frac{w^2}{2}$$

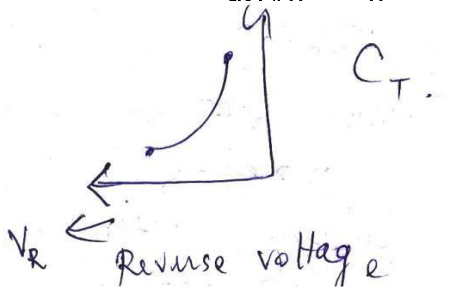
$$1=\frac{qN_A}{s} \times \frac{1}{2}\frac{dw}{dv}2w$$

$$\frac{dw}{dv} = \frac{\varepsilon}{qN_Aw}$$

Diff 2

$$\frac{dQ}{dv} = qN_AA\frac{dw}{dv}$$

$$C_T = qN_AA\frac{\varepsilon}{qN_Aw} = \frac{A\varepsilon}{w}$$



Ex : Varactor diode (or) Tuning diode

Diffusion capacitance C_D:(May 2017)

The junction behaves like a capacitor. The capacitance, which exists in a forward-biased junction is called a *diffusion* or *storage capacitance.* It is different from the transition or depletion layer capacitance, which exists in a reverse-biased junction. The diffusion capacitance arises due to the arrangement of minority carrier density. And its value is much larger than the depletion layer capacitance.

Width of depletion region ↓ As applied voltage ↑, the concentration of injected charged particle also increases. This rate of change of injected change with applied voltage is capacitance.

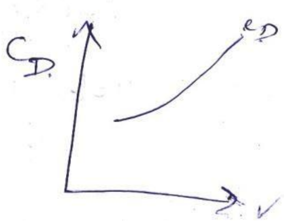
r = mean lifetime of the carrier

I = value of forward current

η = A constant (1 for Ge and 2 for Si)

V_T=volt equivalent of temperature.

$$C_D = \frac{dQ}{dv}$$



$C_D$is >C_T

$I=I_{pn(0)} + I_{np\,(0)}$

$I_{pn(0)}$ → hole diffusion current n region

$I_{np\,(0)}$ → electron diffusion current in p region

$$I_{np(0)} \backsimeq 0$$

P side heavily doped

$$J_{p(x)} = -qD_p \frac{dp_n}{dx}$$

$$J = \frac{I}{A}$$

$I_p(X) = -qAD_p \frac{dp_n}{dx}$ ------------------------ 1

$P_n(X) = P_{n(0)} e^{-X/L_P}$ -------------------------- 2

Hole concentration in the right side of p material $P_{n(0)}$ ie junction

Diff 2

$$\frac{dp_n(x)}{dx} = P_{n(0)} e^{-X/L_P} \left(\frac{-1}{L_P}\right)$$

$I_p(X) = -qAD_p P_{n(0)} e^{-X/L_P}$. -1/$L_P$

At x=0 $I_p(X) = I_{pn(0)} = I$

$$I = \frac{QAD_P}{L_P} Pn(0)$$

$Pn(0) = \frac{I\,L_P}{QAD_P}$ --- A

Now the excess minority charge exists only on n side and given by

$Q = \int_0^\infty Aq\,Pn(0) e^{-X/L_P} dx$

$= AqPn(0) \left[\frac{e^{-X/L_P}}{\frac{-1}{L_P}}\right]_0^\infty$

$= AqLpPn(0)[e^{-\infty} - e^{-0}]$

$Q = -AqLpPn(0)$

$Q = AqLpPn(0)$------------------B

Put A in B

$Q = \frac{AqLpIL_P}{qADp} = \frac{L_P^2}{Dp}. I$

Assume

$\frac{L_P^2}{Dp} = r$

$Q = rI \Rightarrow \frac{dQ}{dI} = r$

W.K.T

$$C_D = \frac{dQ}{dI} \cdot \frac{dI}{dV}$$

$$C_D = r. \frac{dI}{dV}$$

$$I = I_o(e^{V/DV_T})$$

$$\frac{dI}{dV} = I. \frac{1}{\eta V_T}$$

$$C_D = r. \frac{I}{\eta V_T}$$

It is evident from the above relation, that diffusion capacitance is directly proportional to the forward current *(I)*.

Rectifiers – Half Wave and Full Wave

Half Wave

4. What is halfwave rectifier? Explain the working principle with neat sketch? (Nov / Dec 2015) (Nov/Dec 2016)

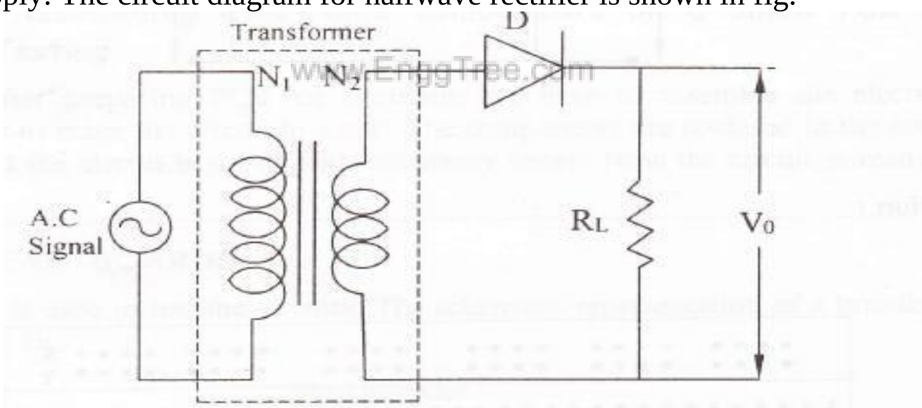
Rectifiers *are a class of circuits whose purpose is to convert ac waveforms (usually sinusoidal and with zero average value) into a waveform that has a significant non-zero average value (dc component)*. Simply stated, rectifiers are ac-to-dc energy converter circuits. Most rectifier circuits employ diodes as the principal elements in the energy conversion process; thus, the almost inseparable notions of diodes and rectifiers.

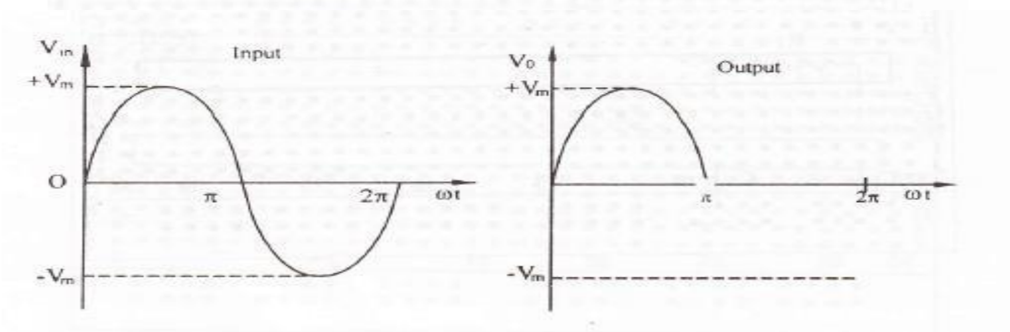
Uncontrolled rectifier: *uncontrolled* refers to the absence of any control signal necessary to operate the primary switching elements (diodes) in the rectifier circuit. (The discussion of controlled rectifier circuits, and the controlled switches themselves, is more appropriate in the context of power electronics applications). Rectifiers are the fundamental building block in dc power supplies of all types and in dc power transmission used by some electric utilities.

There are two types of rectifiers:

(a) Half Wave (HW) rectifier (b) Full Wave (FW) rectifier

Half -wave Rectifier:
It consists of a single diode in series with a load resistor. The input to half wave rectifier is supplied from the 50 Hz a.c supply. The circuit diagram for halfwave rectifier is shown in fig.





Positive half cycle:
During the positive half cycle of the input signal the *anode of the diode becomes positive with respect to the cathode* and hence the diode D conducts. For an ideal to the cathode and hence the diode D conducts. For an ideal diode, the forward voltage drop is zero. So the whole-input voltage will appear across load resistance R_L.

Negative half cycle:
During negative half cycle of the input signal, the *anode of the diode becomes negative with respective to the cathode* and hence the diode D does not contact. For an ideal diode the impedance by the diode is infinity. So the whole input voltage appears across the diode D. hence the voltage drop across R, is zero.

Analysis of Half wave rectifier:

Let Vi be the input voltage to the rectifier

$$V_i = V_m sin\omega t$$

Where,
V_m = Maximum value of the input voltage.
Let I be the current flowing though the circuit when the diode is conducting.

$$i = \begin{cases} I_m sin\omega t & For\ 0 \le \omega t \le \pi \\ 0 & For\ \pi \le \omega t \le 2\pi \end{cases}$$

Where

$$I_m = Maximum\ value\ of\ the\ current$$

$$I_m = \frac{V_m}{R_F + R_L}$$

Where
R_F-Forward dynamic resistance of diode.
R_L-Load resistance.

(a) Average or DC value of output current (I_{dc}):
From Fig., it is seen that the output current is not steady but contains fluctuations even though it is DC current. The average value of this fluctuating current is called DC current (I_{dc}). It can be calculated as follows.

Average value = (Area under the curve / Period)

$$I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} i\, d(\omega t)$$

$$I_{dc} = \frac{1}{2\pi}[\int_0^{\pi} I_m * sin\omega t\, d(\omega t)]$$

$$I_{dc} = \frac{1}{2\pi}[-cos\omega t]_0^{\pi} = \frac{I_m}{2\pi}[-cos\pi - (-cos0)] = \frac{I_m}{2\pi}[-(-1) - (-1)] = \frac{I_m}{\pi}$$

$$I_{dc} = \frac{V_m}{\pi(R_F + R_L)}$$

(b) Average or DC output voltage (V_o):

$$V_{dc} = \frac{I_m}{\pi} \times R_L = \frac{V_m}{\pi}$$

(c) RMS value of output current (I_{rms}):

$$\boldsymbol{I_{rms}} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} i^2 d(\omega t)} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} I_m^2 sin^2\omega t * d(\omega t)} = \sqrt{\frac{I_m^2}{2\pi}\int_0^{\pi} (\frac{1 - cos2\omega t}{2}) * d(\omega t)}$$

$$= \sqrt{\frac{I_m^2}{4\pi}\int_0^{\pi} d(\omega t) - \int_0^{\pi} \cos 2(\omega t) * d(\omega t)} = \sqrt{\frac{I_m^2}{4\pi}\left[\omega t_0^{\pi} - \left(\frac{\sin 2\omega t}{2}\right)_0^{\pi}\right]}$$

$$= \sqrt{\frac{I_m^2}{4\pi}\left[(\pi - 0) - \left(\frac{\sin 2\pi}{2} - \frac{\sin 0}{2}\right)\right]} = \sqrt{\frac{I_m^2}{4\pi}[(\pi - 0) - 0]} = \sqrt{\frac{I_m^2}{4\pi}} = \frac{I_m}{2}$$

(d) Rectification Efficiency (η):

$$\text{Rectification efficiency } (\boldsymbol{\eta}) = \frac{I_{dc}^2 \times R_L}{I_{rms}^2 \times R_L} = \frac{\frac{I_m^2}{\pi} \times R_L}{\frac{I_m^2}{2} \times R_L} = \frac{I_m^2/\pi^2 \times R_L}{I_m^2/4 \times R_L} = \frac{4}{\pi^2} = 0.406$$

(e) Ripple Factor (γ):

$$y = \frac{I'_{rms}}{I_{dc}} = \sqrt{\frac{I_{rms}^2 - I_{dc}^2}{I_{dc}^2}} = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} = \sqrt{\left(\frac{I_{rms}/2}{I_m/\pi}\right)^2 - 1} = \sqrt{\frac{\pi^2}{4} - 1} = \mathbf{1.21}$$

(f) Peak inverse Voltage (PIV):

Peak inverse voltage is defined as the maximum voltage that is applied across the Diode when the diode is reverse biased. [n case of half wave rectifier, maximum Voltage across the diode when it is not conducting is equal to V_m.

$$\boldsymbol{PIV = V_m}$$

(g) From factor:

$$FF = \frac{rms\ value}{average\ value} = \frac{\pi}{2} = 1.57$$

(h) Peak factor:

$$PF = \frac{V_m}{\left(\frac{V_m}{2}\right)} = 2$$

(i) Transformer utilization factor:

$$TUF = \frac{P_{dc}}{P_{ac}}(Transformer\ secondary\ rated) = 0.287$$

Disadvantages of HWR:

- Low output because one half cycle only delivers output
- A.C. component more in the output
- Requires heavy filter circuits to smooth out the output **Peak inverse Voltage.**

Rectifiers – Full Wave using center tap Transformer

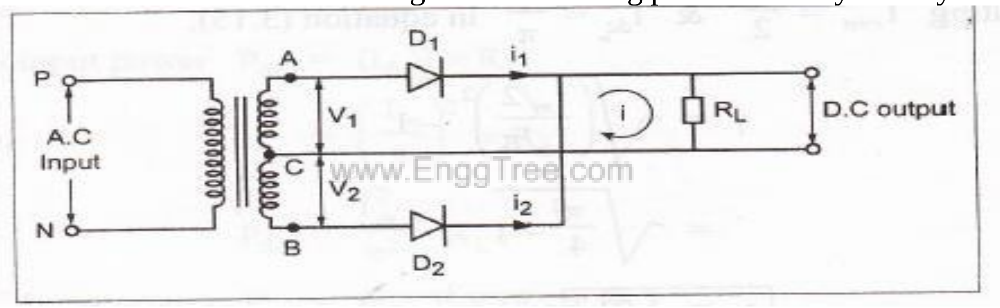
5. Explain the operation of full wave rectifier with center tap transformer. Also derive the following for this rectifier. (Apr/May 2018)

i) DC output voltage (average value) ii) DC output current (average value) iii) RMS output voltage.

In FWR, current flows through the load during both half cycles of the input a.c. supply. Like the half wave circuit, a *full wave rectifier circuit produces an output voltage or current which is purely DC or has some specified DC component*. Full wave rectifiers have some fundamental advantages over their half wave rectifier counterparts. The average (DC) output voltage is higher than for half wave, the output of the full wave rectifier has much less ripple than that of the half wave rectifier producing a smoother output waveform.

Full Wave Rectifier:

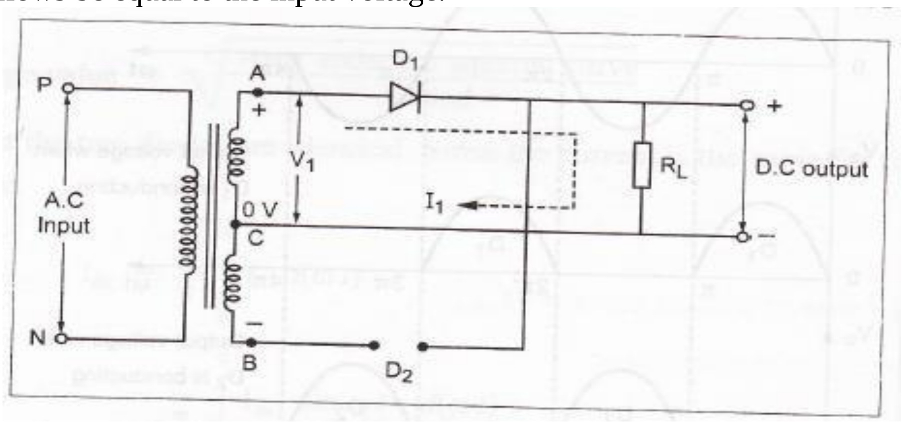
A full wave rectifier is an electronic circuit which converts AC voltage into a pulsating DC voltage using both half cycles of the applied AC voltage. A full wave rectifier is a circuit which allows a unidirectional current to flow through the load during the entire input cycle as shown in fig. The result of full wave rectification is a d.c. output voltage that pulsates every half-cycle of the input. On the other hand a half wave rectifier allows the current to flow through the load during positive half-cycle only.



Positive half cycle:

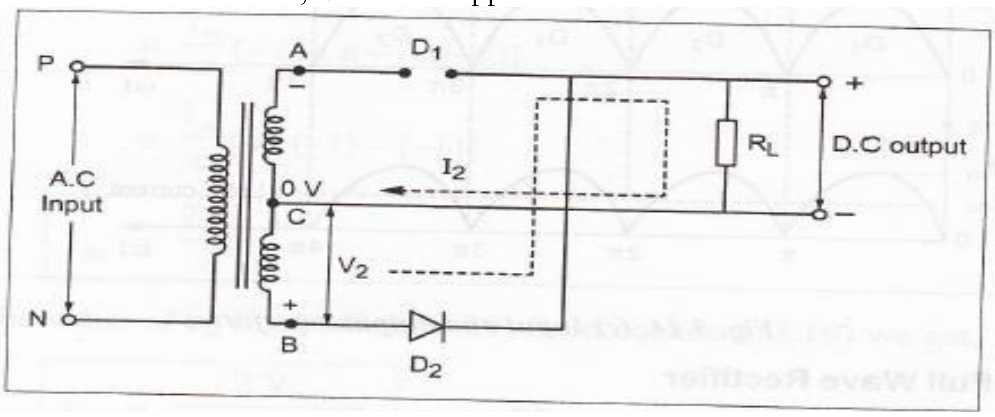
The circuit uses two diodes which are connected to secondary winding of the transformer. The input signal is applied to the primary winding of the transformer. During the positive input half cycle, the polarities of the secondary voltage is shown in fig. This forward bias the diode D, and reverse biases the diode D_1. As a result of this, the diode D, conducts some current whereas the diode D, is off.

The current through load R1 is as indicated in through D_1, and the voltage Drop across R_L will the fig. The load current flows be equal to the input voltage.



Negative half cycle:

During the negative input half cycle, the polarities of the secondary voltage are interchanged. The reverse-bias the diode D, and forward Biases the diode D_2. As a result of this, the diode D_1 is OFF and the diode D_2 conducts some current. The current through the load R, is an indicated in the fig. The load current flows through D_2 and the voltage drop across R_1 will be equal to the input voltage. The maximum efficiency of a fall-wave rectifier is 8l,2%Vo and ripple factor is 0.48.



Analysis of Full Wave Rectifier:

Let Vi be the input voltage to the rectifier, $V_i = V_m sin\omega t$

Where, V_m = Maximum value of the input voltage.

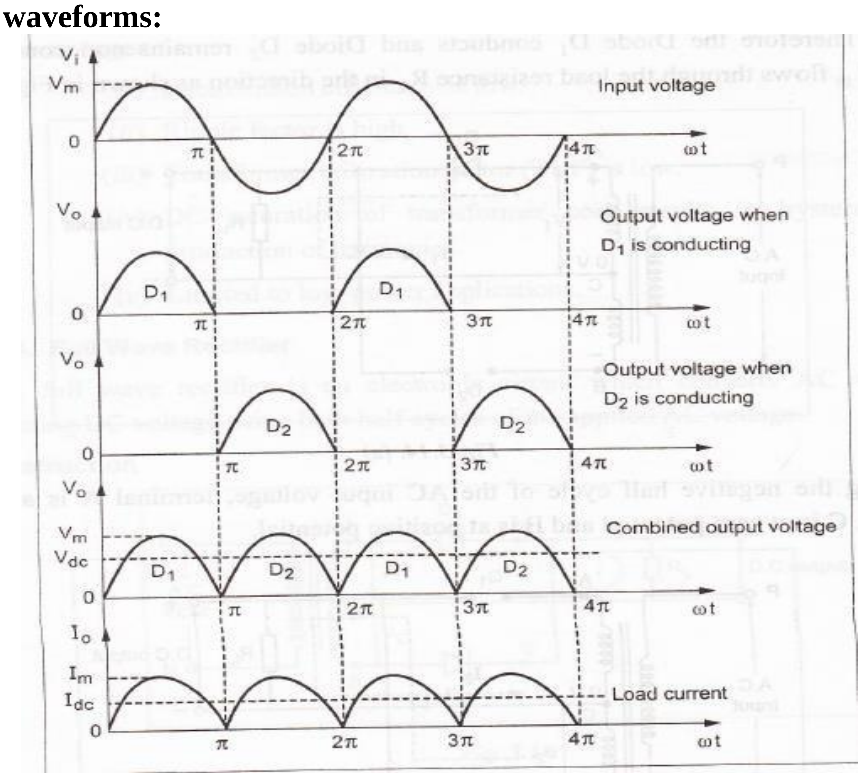
Let I be the current flowing though the circuit when the diode is conducting.

$$i = \begin{cases} I_m sin\omega t & For\ 0 \leq \omega t \leq \pi \\ 0 & For\ \pi \leq \omega t \leq 2\pi \end{cases}$$

Where, $I_m = Maximum\ value\ of\ the\ current$; $I_m = \frac{V_m}{R_F + R_L}$

Where, R_F-Forward dynamic resistance of diode; R_L-Load resistance.

Input and output waveforms:



(a) Average or DC value of output current (I_{dc}):

Average value = (Area under the curve / Period)

$$I_{dc} = \frac{1}{\pi}\int_0^{\pi} i\, d(\omega t)$$

$$I_{dc} = \frac{1}{\pi}\left[\int_0^{\pi} I_m * \sin\omega t\, d(\omega t)\right]$$

$$I_{dc} = \frac{1}{\pi}[-\cos\omega t]_0^{\pi} = \frac{I_m}{\pi}[-\cos\pi - (-\cos 0)] = \frac{I_m}{\pi}[-(-1) - (-1)] = \frac{2I_m}{\pi}$$

$$I_{dc} = \frac{2V_m}{\pi(R_F + R_L)}$$

(b) Average or DC value of output voltage (V_{dc}) :

$$V_{dc} = \frac{2I_m}{\pi} \times R_L = \frac{2V_m}{\pi}$$

(c) RMS value of output current (I_{rms}):

$$\boldsymbol{I_{rms}} = \sqrt{\frac{1}{\pi}\int_0^{\pi} i^2 d(\omega t)} = \sqrt{\frac{1}{\pi}\int_0^{\pi} I_m^2 \sin^2\omega t * d(\omega t)} = \sqrt{\frac{I_m^2}{\pi}\int_0^{\pi}\left(\frac{1-\cos 2\omega t}{2}\right) * d(\omega t)}$$

$$= \sqrt{\frac{I_m^2}{2\pi}\int_0^{\pi} d(\omega t) - \int_0^{\pi}\cos 2(\omega t) * d(\omega t)} = \sqrt{\frac{I_m^2}{2\pi}\left[\omega t_0^{\pi} - \left(\frac{\sin 2\omega t}{2}\right)_0^{\pi}\right]}$$

$$= \sqrt{\frac{I_m^2}{2\pi}\left[(\pi - 0) - \left(\frac{\sin 2\pi}{2} - \frac{\sin 0}{2}\right)\right]} = \sqrt{\frac{I_m^2}{2\pi}[(\pi - 0) - 0]} = \sqrt{\frac{I_m^2}{2}} = \frac{I_m}{\sqrt{2}}$$

(d) Rectification Efficiency (η):

Rectification efficiency **(η)** $= \frac{I_{dc}^2 \times R_L}{I_{rms}^2 \times R_L} = \frac{\frac{2Im^2}{\pi} \times R_L}{\frac{Im^2}{\sqrt{2}} \times R_L} = \frac{4I_m^2/\pi^2 \times R_L}{I_m^2/2 \times R_L} = \frac{0.812}{(1+\frac{R_F}{R_L})} = 81.2\%$

(e) Ripple Factor (γ):

$$y = \frac{\text{RMS value of Ac component}}{\text{Dc value of wave}} = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} = \sqrt{\left(\frac{I_m/\sqrt{2}}{2I_m/\pi}\right)^2 - 1} = \sqrt{\frac{\pi^2}{8} - 1} = \mathbf{0.48}$$

(f) Peak inverse Voltage (PIV):

Peak inverse voltage is the maximum possible voltage across a diode when it is not conducting. During positive half cycle of the AC input voltage Diode D1, is conducting and Diode D, is not conducting. In this case a voltage V, is developed across the load resistor R_1. Now the voltage across the non-conducting Diode D, is the sum of the voltage across R1 and voltage across the lower half of transformer secondary V_m.

Hence, PIV of Diode D2 = $V_m + V_m = 2V_m$

Similary, PIV of Diode D1 = $V_m + V_m = 2V_m$

Advantages:
1. The D.c load voltage and current are more than halfwave.
2. No D.c current thro transformer windings hence no possibility of saturation.
3. TUF is better.
4. Efficiency is higher.
5. Ripple factor less.

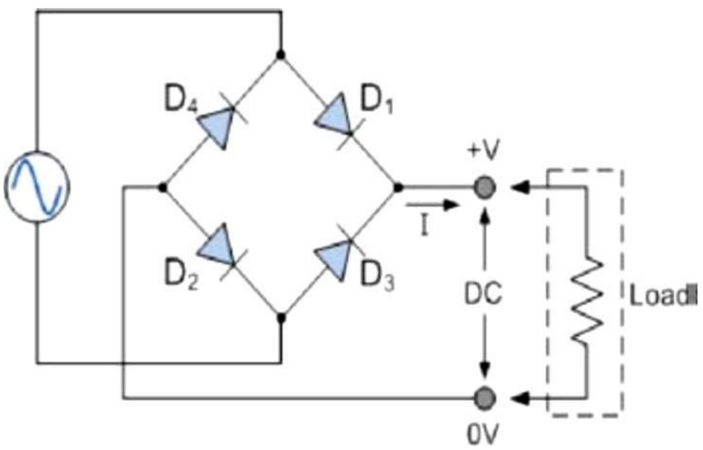
Disadvantages:
1. PIV rating of diode is higher
2. Higher PIV diodes are larger in size ad costlier.
3. Cost of transformer is high.

Rectifiers – Full Wave Bridge type

6. (a) Draw the circuit diagram and explain the working of full wave bridge rectifier & derive the expansion for average amount current & rectification efficiency. (May 2017) (Nov/Dec 2017) (Nov/Dec 2018)

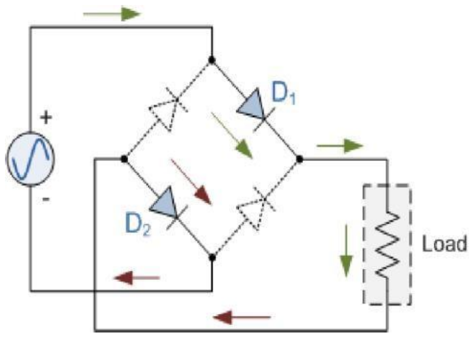
Bridge rectifier (Full Wave Bridge rectifier):

Another type of circuit that produces the same output waveform as the full wave rectifier circuit above is that of the **Full Wave Bridge Rectifier**. This type of single-phase rectifier uses four individual rectifying diodes connected in a closed loop "bridge" configuration to produce the desired output. The main advantage of this bridge circuit is that it does ***not require a special center tapped transformer***, thereby reducing its size and cost. The single secondary winding is connected to one side of the diode bridge network and the load to the other side as shown below.

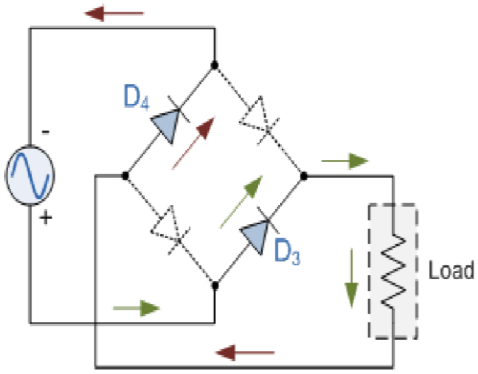


The four diodes labeled D1 to D4 are arranged in "series pairs" with only two diodes conducting current during each half cycle. *During the positive half cycle of the supply, diodes D1 and D2 conduct* in series while diodes D3 and D4 are reverse biased and the current flows through the load as shown below.

During the negative half cycle of the supply, diodes D3 and D4 conduct in series, but diodes D1 and D2 switch of as they are now reverse biased. The current flowing through the load is the same direction as before. As the current flowing through the load is unidirectional, so the voltage developed across the load is also unidirectional the same as for the previous two diode full-wave rectifier.

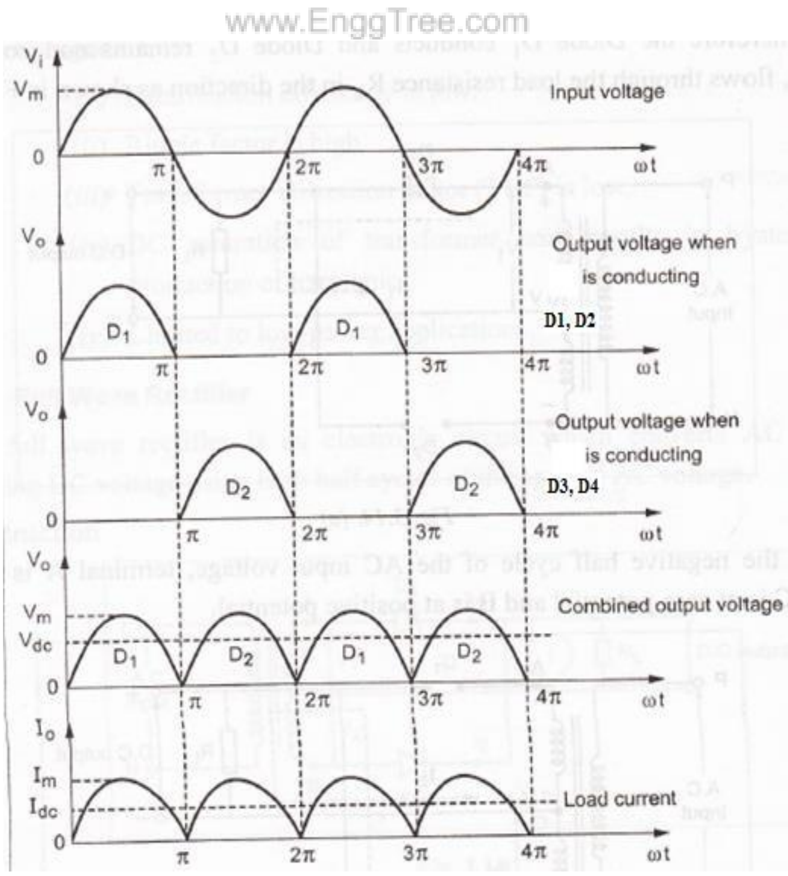


Positive half cycle



Negative half cycle

Waveform:



Analysis of Full Wave Rectifier:

Let Vi be the input voltage to the rectifier, $V_i = V_m sin\omega t$
Where,
V_m = Maximum value of the input voltage.
Let I be the current flowing though the circuit when the diode is conducting.

$$i = \begin{cases} I_m sin\omega t & For\ 0 \le \omega t \le \pi \\ 0 & For\ \pi \le \omega t \le 2\pi \end{cases}$$

Where

$$I_m = Maximum\ value\ of\ the\ current$$

$$I_m = \frac{V_m}{R_F + R_L}$$

Where, R_F-Forward dynamic resistance of diode; R_L-Load resistance.

(a) Average or DC value of output current (I_{dc}):

Average value = (Area under the curve / Period)

$$I_{dc} = \frac{1}{\pi}\int_0^\pi i\, d(\omega t) \qquad I_{dc} = \frac{1}{\pi}[\int_0^\pi I_m * \sin\omega t\, d(\omega t)]$$

$$I_{dc} = \frac{1}{\pi}[-\cos\omega t]_0^\pi = \frac{I_m}{\pi}[-\cos\pi - (-\cos 0)] = \frac{I_m}{\pi}[-(-1) - (-1)] = \frac{2I_m}{\pi}$$

$$I_{dc} = \frac{2V_m}{\pi(R_F + R_L)}$$

(b) Average or DC value of output voltage (V_{dc}): $V_{dc} = \frac{2I_m}{\pi} \times R_L = \frac{2V_m}{\pi}$

(c) RMS value of output current (I_{rms}):

$$\boldsymbol{I_{rms}} = \sqrt{\frac{1}{\pi}\int_0^\pi i^2 d(\omega t)} = \sqrt{\frac{1}{\pi}\int_0^\pi I_m^2 \sin^2\omega t * d(\omega t)} = \sqrt{\frac{I_m^2}{\pi}\int_0^\pi (\frac{1-\cos 2\omega t}{2}) * d(\omega t)}$$

$$= \sqrt{\frac{I_m^2}{2\pi}\int_0^\pi d(\omega t) - \int_0^\pi \cos 2(\omega t) * d(\omega t)} = \sqrt{\frac{I_m^2}{2\pi}[\omega t_0^\pi - (\frac{\sin 2\omega t}{2})_0^\pi]}$$

$$= \sqrt{\frac{I_m^2}{2\pi}[(\pi - 0) - (\frac{\sin 2\pi}{2} - \frac{\sin 0}{2})]} = \sqrt{\frac{I_m^2}{2\pi}[(\pi - 0) - 0]} = \sqrt{\frac{I_m^2}{2}} = \frac{I_m}{\sqrt{2}}$$

(d) Rectification Efficiency (η):

Rectification efficiency **(η)** $= \frac{I_{dc}^2 \times R_L}{I_{rms}^2 \times R_L} = \frac{\frac{2I_m}{\pi}^2 \times R_L}{\frac{I_m}{\sqrt{2}}^2 \times R_L} = \frac{4I_m^2/\pi^2 \times R_L}{I_m^2/2 \times R_L} = \frac{0.812}{(1+\frac{R_F}{R_L})} = 81.2\%$

(e) Ripple Factor (γ):

$$y = \frac{\text{RMS value of Ac component}}{\text{Dc value of wave}} = \sqrt{(\frac{I_{rms}}{I_{dc}})^2 - 1} = \sqrt{(\frac{I_m/\sqrt{2}}{2I_m/\pi})^2 - 1} = \sqrt{\frac{\pi^2}{8} - 1} = \mathbf{0.48}$$

(f) Peak inverse Voltage (PIV):

Peak inverse voltage is the maximum possible voltage across a diode when it is not Conducting. During positive half cycle of the AC input voltage Diode D1, is conducting and Diode D, is not conducting. In this case a voltage V, is developed across the load resistor R_1. Now the voltage across the non-conducting Diode D, is the sum of the voltage across R1 and voltage across the lower half of transformer secondary V_m.
Hence, PIV of Diode D2 = $V_m + V_m = 2V_m$
Similary, PIV of Diode D1 = $V_m + V_m = 2V_m$

Advantages:

1. The D.c load voltage and current are more than half wave.
2. No D.c current thro transformer windings hence no possibility of saturation.
3. TUF is better.
4. Efficiency is higher.
5. Ripple factor less.
6. No centre tapped is required.

Disadvantages:

4 diodes are used therefore voltage drop across the diode is increased. This reduces output voltage.

Applications:
1. In power supply circuits.
2. Used as rectifier in power circuits to convert A.C to D.C

(b) In a bridge rectifier circuit, input supply is 230V, 50 Hz. Primary to secondary turns ratio is 4:1, load resistance is 200 Ω. The diodes are ideal. Find DC output voltage, PIV and output signal frequency. **(Nov / Dec 2018-R17)**

Solution: $E_{py}\,(rms) = 230V, \frac{N_2}{N_1} = \frac{1}{4}, R_L = 200\Omega \quad R_f = R_s = 0\Omega\ as\ ideal$

$$\frac{E_{py}\,(rms)}{E_{sy}\,(rms)} = \frac{N_1}{N_2},\ E_{sy}\,(rms) = \frac{N_1}{N_2}\ X\ E_{py}\,(rms) = \frac{1}{4}\ X\ 230 = 57.5\ V,$$

$$E_{sy\,(max)} = \sqrt{2}\,E_{py\,(rms)} = \sqrt{2}\ X\ 57.5 = 81.31\ V$$

$$I_m = \frac{E_{sm}}{R_s + 2R_f + R_L} = \frac{81.31}{200} = 0.4065\ A \quad I_{DC} = \frac{2\,I_m}{\pi} = \frac{2\ X\ 0.4065}{\pi} = 0.2587\ A$$

$$E_{DC} = I_{DC}\,R_L = 0.2587\ X\ 200 = 51.74\ V$$

PIV = E_{sm} = 81.31V (for full wave rectifier)

Output signal frequency = $2f_s$ = 2 X 50 = 100Hz

Ripple Factor (for Full Bridge Rectifier) = 0.482,

$$\text{Ripple Factor} = \frac{AC\ rms\ output}{DC\ output} = \frac{Ripple\ Voltage}{E_{DC}} \quad 0.482 = \frac{Ripple\ Voltage}{51.74}$$

i.e. Ripple voltage = 51.74 X 0.482 = 24.94 V

7. Compare different types of rectifiers?

Type	HW	CT FW	FW BR
No of diodes used	1	2	4
Need of transformer	Not necessary	Necessary	Not necessary
Ripple factor	1.21	0.48	0.48
Efficiency	40.6%	81.2%	81.2%
PIV	V_m	$2V_m$	V_m
TUF	0.287	0.812	0.693
From factor	1.57	1.11	1.11
Peak factor	2	$\sqrt{2}$	$\sqrt{2}$
Ripple frequency	f	2f	2f

Display devices- LED

8. Discuss the working principle, characteristics and application of LED in detail. (NOV/DEC 2012) (Apr/May 2018)

Explain the principle and operation of light emitting diode (LED) with necessary expressions for current densities and efficiency of light generation. (April / May 2019-R17)

A **light-emitting diode**(LED) is a semiconductor light source LEDs are used as indicator lamps in many devices and are increasingly used for other lighting. Introduced as a practical electronic component in 1962, early LEDs emitted low-intensity red light, but modern versions are available across the visible, ultraviolet, and infrared wavelengths, with very high brightness.

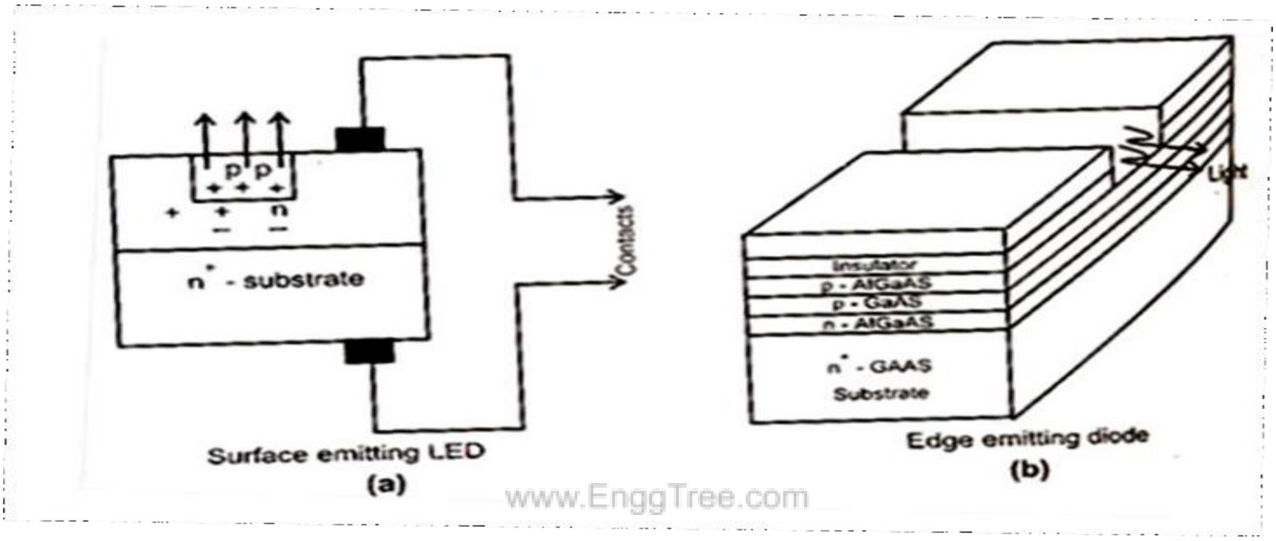
When a light-emitting diode is forward-biased (switched on), electrons are able to recombine with electron holes within the device, releasing energy in the form of photons. This effect is called electroluminescence and the color of the light (corresponding to the energy of the photon) is determined by the energy gap of the semiconductor.

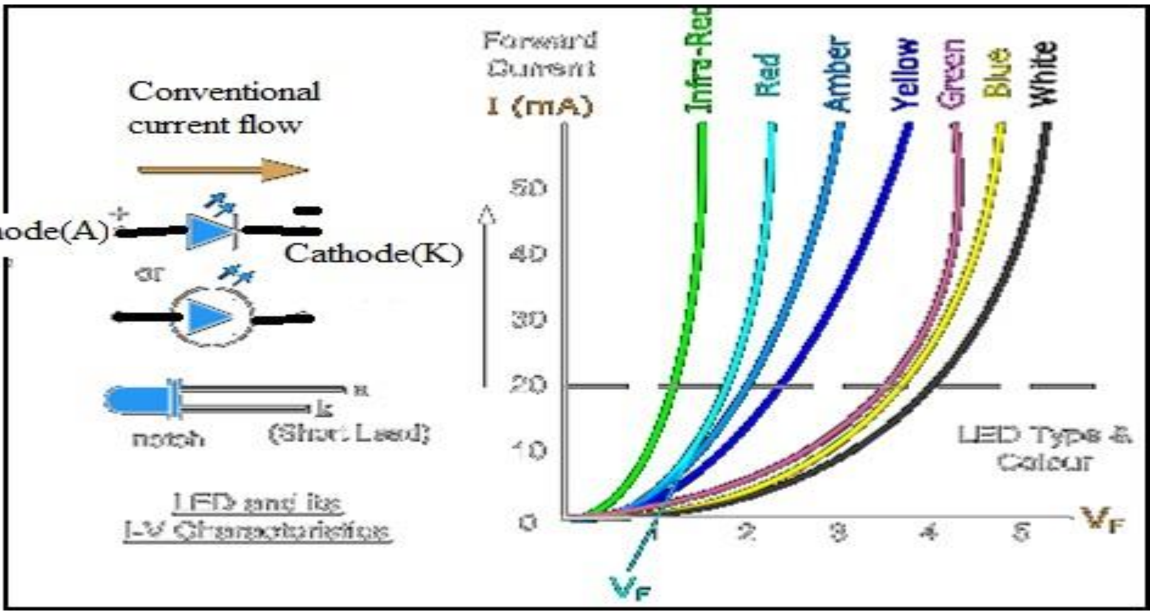
LEDs are often small in area (less than 1 mm^2), and integrated optical components may be used to shape its radiation pattern.[5] LEDs present many advantages over incandescent light sources including lower energy consumption, longer lifetime, improved robustness, smaller size, and faster switching. LEDs powerful enough for room lighting are relatively expensive and require more precise current and heat management than compact fluorescent lamp sources of comparable output.

Light Emitting Diodes are made from exotic semiconductor compounds such as Gallium Arsenide (GaAs), Gallium Phosphide (GaP), Gallium Arsenide Phosphide (GaAsP), Silicon Carbide (SiC) or Gallium Indium Nitride (GaInN) all mixed together at different ratios to produce a distinct wavelength of colour.

Different LED compounds emit light in specific regions of the visible light spectrum and therefore produce different intensity levels.

- Gallium Arsenide Phosphide (GaAsP) - red to infra-red, orange
- Aluminium Gallium Arsenide Phosphide (AlGaAsP) - high-brightness red, orange-red, orange, and yellow
- Gallium Phosphide (GaP) - red, yellow and green
- Aluminium Gallium Phosphide (AlGaP) - green
- Gallium Nitride (GaN) - green, emerald green
- Gallium Indium Nitride (GaInN) - near ultraviolet, bluish-green and blue
- Silicon Carbide (SiC) - blue as a substrate
- Zinc Selenide (ZnSe) - blue
- Aluminium Gallium Nitride (AlGaN) - ultraviolet





Light-emitting diodes are used in **applications** as diverse as aviation lighting, automotive lighting, advertising, general lighting, and traffic signals. LEDs have allowed new text, video displays, live video, and sensors to be developed, while their high switching rates are also useful in advanced communications technology. Infrared LEDs are also used in the remote control units of many commercial products including televisions, DVD players, and other domestic appliances.

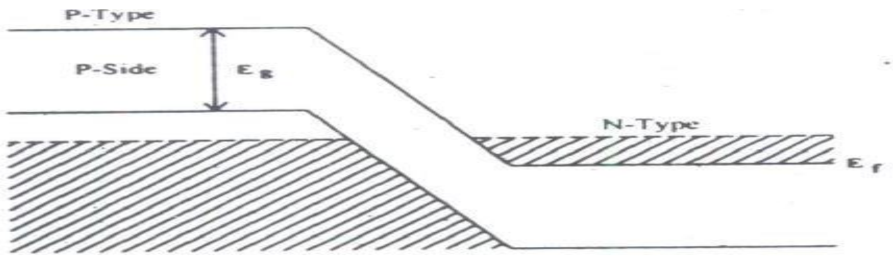
Laser diodes

9. Explain in detail about LASER DIODE? (May / June 2016) (April/May 2018)

The term laser comes from the acronym for light amplification for stimulated emission of radiation. The laser medium can be a gas, liquid, amorphous solid or semiconductor.

Laser Action

The light travelling through a semiconductor, then a single photon is able to generate an identical second photon. This photon multiplication is the key physical mechanism of lasing. The carrier inversion is the first requirement of lasing. It is achieved at the PN junction by providing the conduction bandwith electrons from the N-doped side and the valence band with holes from the P-doped side as shown in Fig. The photon energy is given by the band gap, which depends on the semiconductor material. The optical feedback and the confinement of photon in an optical resonator are the second basic requirement of lasing.



PN Homojunction Laser

It has the material GaAs on both sides of the junction. A pair of parallel planes perpendicular to the plane of the junction are cleared and polished under appropriate biasing in off condition, laser light is emitted from these planes. The other two sides are deliberately roughened to prevent lasing in those directions. Such a cavity is called a Fabryperot resonant cavity with a typical cavity length of 300 |**J**.m. It is a thin layer of material with a narrow band gap. GaAs is sandwiched between layers of a material with band gap. This is usually realized by epitaxy. In such a structure the carrier are better confined in the active region due to the heterojunction barriers. Optical confinement is also better in ***DH*** laser. The propagation of the electromagnetic radiation is confined in a direction parallel to the

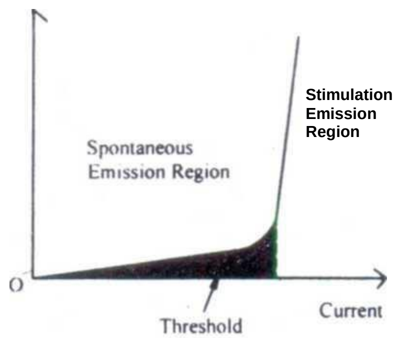
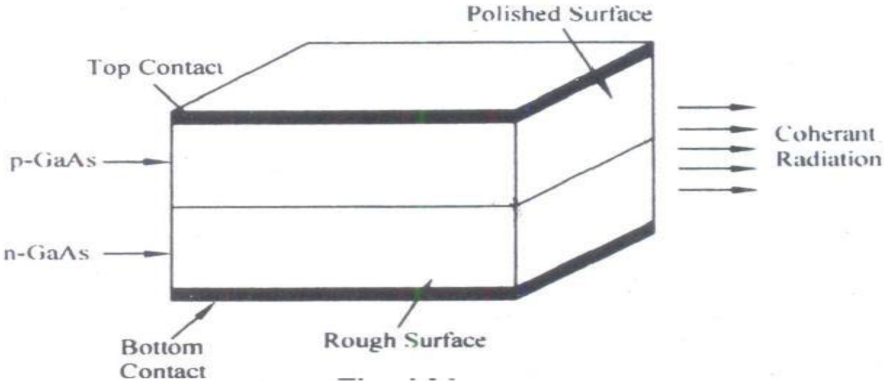
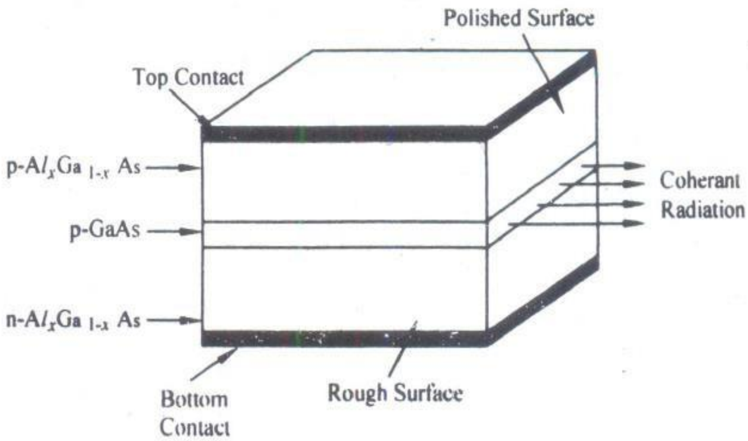


Fig. 4.28

layer interface. The current density required for lasing in lower for ***DH*** lasers compared to homojunction lasers. The double preferred for continuous operation at room temperature.



Double Hetrostructure Laser



Characteristics of Laser Diode

The Ideal light output against current characteristics for semiconductor laser is shown in Fig.4.28. The solid line represents the laser characteristics. It may be observed that the device gives low light output in the region, the threshold with corresponds to spontaneous emission only within the structure. After the threshold current value the light output increases substantially for small increases in current through the device.

ZENER DIODE

10. Explain the construction & working principle of Zener diode.
Explain the Break down mechanisms in semiconductor devices. (May/June 2016), (Nov / Dec 2015)
(OR) Explain the Concept of Zener Breakdown and its VI characteristics. (Nov/Dec 2018-R-13)

ZENER DIODE:
The Zener Diode is a PN junction semiconductor device.
It is fabricated with precise breakdown voltages, by controlling the doping level during manufacturing.
Practically, Zener Diodes are operated in reverse biased mode.

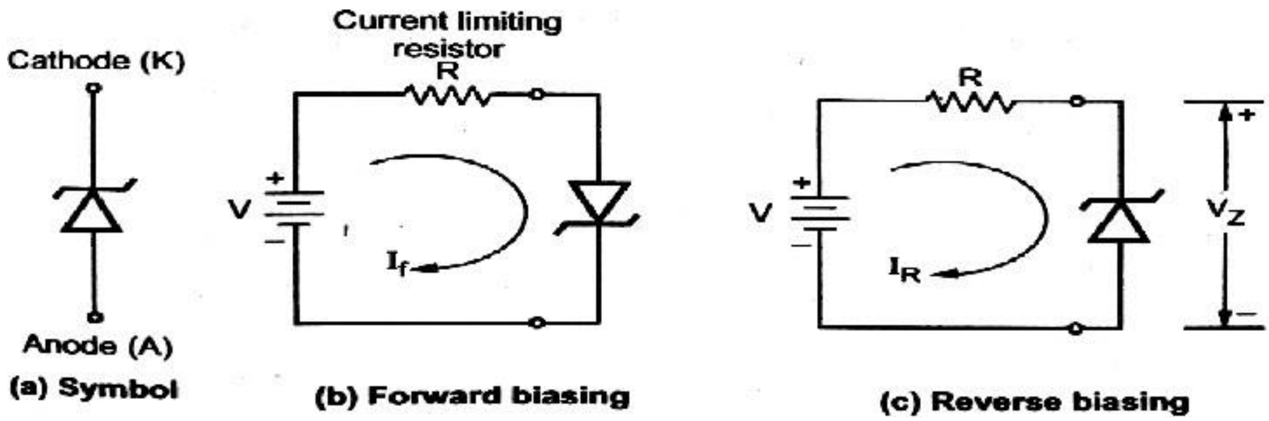


Fig.20 *Zener Diode*

CHARACTERISITCS OF ZENER DIODE:

FORWARD CHARACTERISITCS:

In forward biased condition, the normal rectifier diode and the Zener diode operate in similar fashion.
(Refer: PN diode forward characteristics)

Zener reverse characteristics

REVERSE CHARACTERISITCS:

Zener diode is designed to operate in the reverse biased condition.

In reverse biased condition, the diode carries ***reverse saturation current*** till the reverse voltage applied is less than the reverse breakdown voltage.

When the reverse voltage exceeds reverse breakdown voltage, the current through it changes drastically but the voltage across it remains almost constant.

Such a breakdown region is a normal operating region for a Zener diode.

The normal operating regions for both diode and Zener are shown in below Fig.

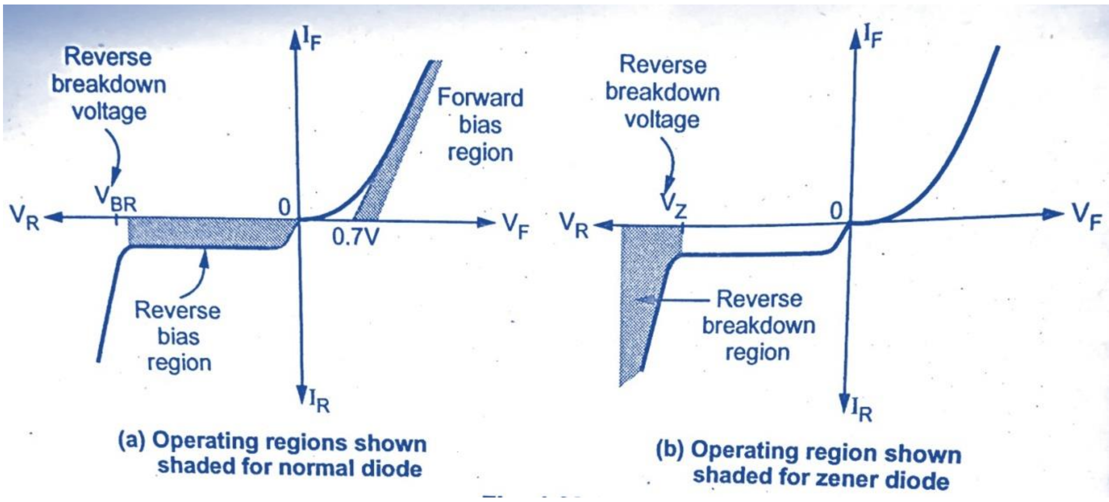


Fig. *The normal operating region for a rectifier diode and Zener diode*

When the applied reverse voltage is increased then, the current through it is very small (few µA) and it is called Reverse Leakage Current (I_o)
At certain reverse voltage, the current will increase rapidly. The breakdown occurs and the current at this point (***knee or Zener knee***) is called ***Zener knee current (I_{ZK} or I_{Zmin}).***
Zener knee current is the minimum Zener current which is must to carry out the operate in Reverse Breakdown Region.
The reverse voltage at which the breakdown occurs is called ***Zener Breakdown Voltage or Zener Voltage (V_Z)***.
The ***V_Z*** is set by controlling the doping level during manufacturing process.

Below the knee, the **reverse breakdown voltage** increases slightly as Zener current (I_Z) increases but, remains almost ***CONSTANT***.
The current at which the nominal Zener breakdown voltage is specified is called ***Zener Test Current (I_{ZT}).***

As the current increases, the power dissipation ($P_Z = V_Z I_Z$) will be increased and if this power dissipation is increased beyond a certain current value, the Zener diode may get damaged. So, there is a maximum current that a Zener diode can carry safely is called ***Zener Maximum Current (I_{ZM} or I_{Zmax}).***

In practical circuits, a current limiting resistor is used in series with Zener diode in order to limit the current between I_{Zmin} to I_{Zmax}.

The complete VI characteristics of Zener Diode is shown in Fig.

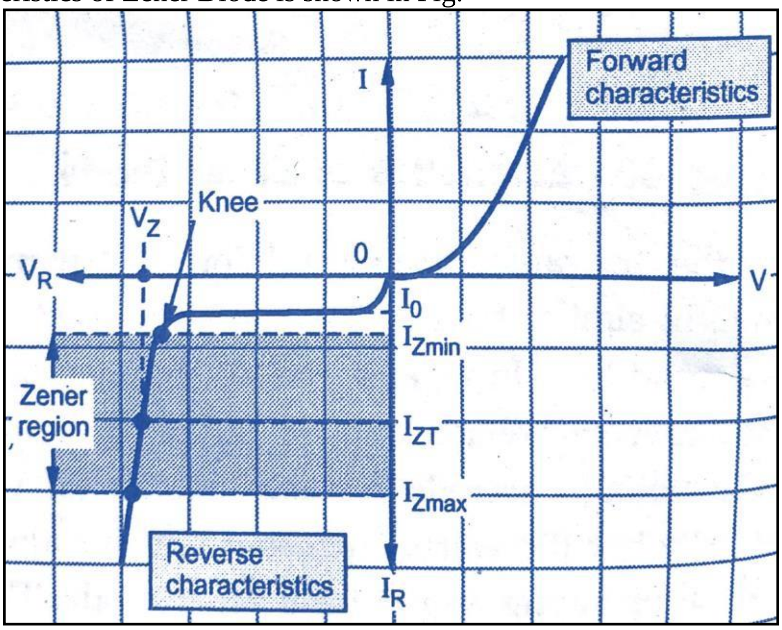


Fig. *VI characteristics of Zener Diode*

EQUIVALENT CIRCUIT OF ZENER DIODE:

When the breakdown occurs then I_Z may increase from I_{Zmin} to I_{Zmax} but voltage across Zener remains almost constant. The internal impedance decreases as current increases in Zener region. But this impedance is very small and hence ideally Zener diode is indicated by a battery of voltage V_Z. This V_Z remains almost constant in the Zener region which is shown in Fig.

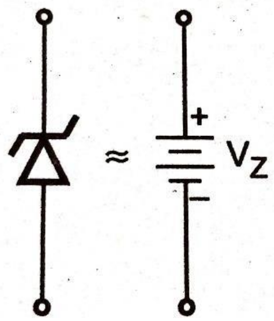
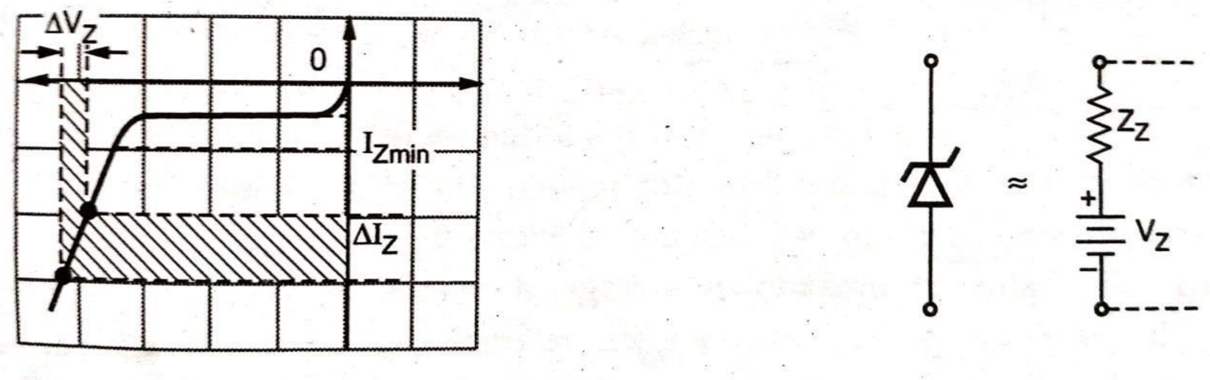


Fig. *Ideal equivalent circuit of Zener diode*

In practical circuit, the Zener internal resistance is to be considered (even though it is very small) and called as ***Zener Dynamic Resistance Z_Z***. Due to this resistance the Zener region is not exactly vertical, i.e., for the small change in the Zener current ΔI_Z produces a small change in Zener voltage ΔV_Z. The ratio of V_Z to I_Z is called ***Zener resistance Z_Z***.
Hence, the practical Zener diode equivalent circuit should be indicated with a battery of V_Z along with series resistance Z_Z as shown in Fig.

Dynamic Resistance, $Z_Z = \frac{\Delta V_Z}{\Delta I_Z} = \frac{1}{[\frac{\Delta I_Z}{\Delta V_Z}]}$

$$Z_Z = \frac{1}{[slope\ of\ the\ reverse\ characteristics\ in\ zener\ region]}$$



(a) Dynamic resistance **(b) A.C. equivalent circuit**

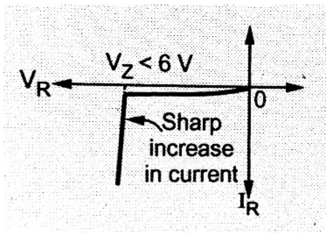
BREAKDOWN MECHANISM IN ZENER DIODE:

Two distinct breakdown mechanism:
- ✓ Zener Breakdown
- ✓ Avalanche Breakdown

For devices with breakdown voltage ***less than 5V - Zener Breakdown***
For devices with breakdown voltage ***between 5V and 8V - Zener Breakdown and Avalanche Breakdown***
For devices with breakdown voltage ***above 8V - Avalanche Breakdown***

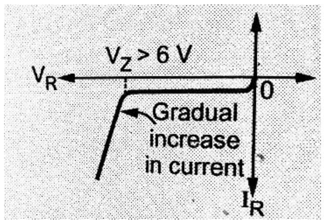
ZENER BREAKDOWN:
Zener breakdown occurs at Reverse biased condition because of heavy doping;
*Practically, **Zener breakdown** is observed in the Zener diodes with breakdown voltage **less than 6V**.*
In Zener breakdown, the value of the breakdown voltage decreases as PN junction temperature increases, i.e. Negative Temperature Coefficient (NTC)

For applied reverse biased voltage of less than 6V causes a high magnitude electric field (3 X 10^5 V/cm) across the depletion region, at the PN junction.
This electric field applies a large force on the valence electron of the atom, tending it to separate them from their respective nuclei. Electron-hole pairs are generated in large numbers and there will be a sudden increase in current. *(To limit this current, a **current limiting resistor** is used in order to protect the Zener diode from being destroyed because of excessive heating at the junction)*



AVALANCHE BREAKDOWN:
Avalanche Breakdown occurs at Reverse biased condition due to ionization of electron and hole pairs
*Practically, **Avalanche breakdown** is observed in the Zener diodes with breakdown **voltage greater than 6V.***
In avalanche breakdown, the value of the breakdown voltage increases as PN junction temperature increases, i.e. Positive Temperature Coefficient (PTC)

For applied reverse biased voltage of greater than 6V causes increased acceleration of minority charge particles. Thus, collision between accelerated charge particles with high velocity and kinetic energy with adjacent atom is involved in breaking the covalent bonds of the crystal structure. This process is called **Carrier Multiplication**.
At this stage, junction is said to be in breakdown and current starts increasing rapidly. *To limit this current below I_{Zmax}, a **current limiting resistor is necessary.***



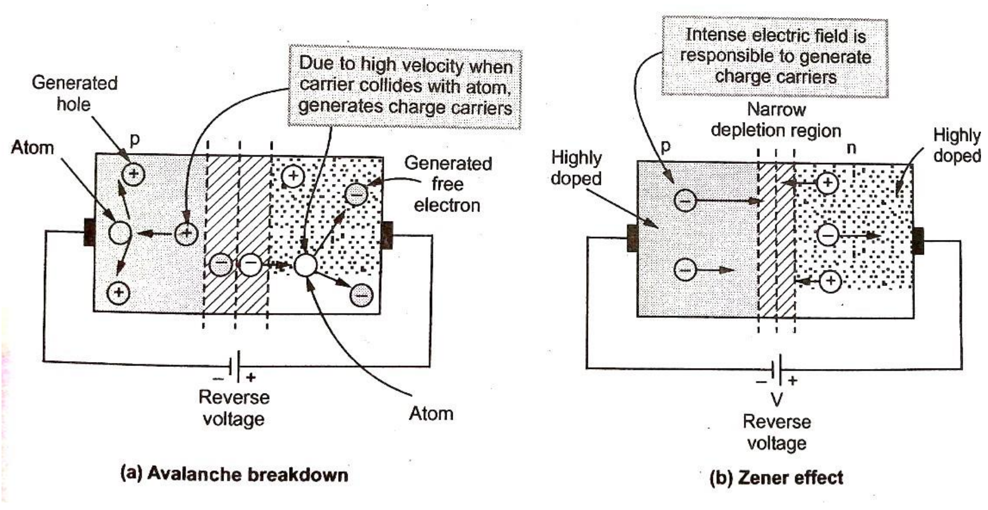


Fig. *Breakdown Mechanism in Zener Diode*

ZENER AS REGULATOR

11. (a) Explain the working of a Zener diode as a regulator? (May 2017) (Nov/Dec 2017) (Nov/Dec 2018 – R17)

The Zener Diode is used to regulate the *Load Voltage*. Here, the Zener is used in reverse biased condition.

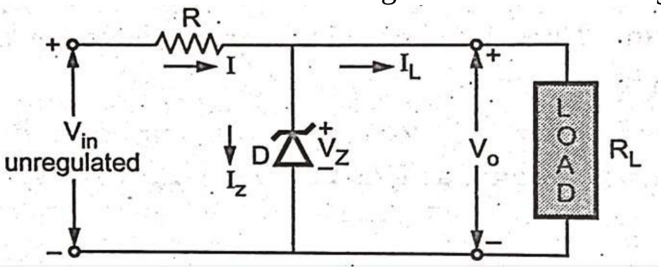


Fig. *Zener Diode as a shunt regulator*

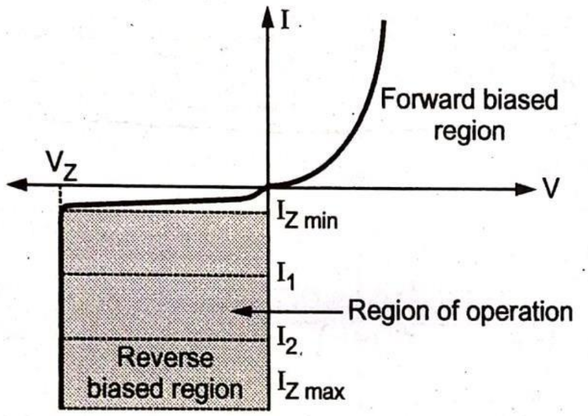


Fig. *VI characteristics of Zener Diode*

{Under reverse biased condition, the current through the zener diode is very small of the order of few µA, up to certain limit. When enough reverse bias voltage is applied, electrical breakdown occurs and large current flows through the zener diode. The voltage at which the breakdown occurs is called **Zener Voltage (V_Z)**.

Under this condition, whatever may be the current, the **voltage** across the Zener is **constant** and **equal to V_Z**}

Since, voltage across the Zener Diode is *CONSTANT* & *equal to* V_Z, it is connected across the load.
∴ The Load Voltage (Vo) is equal to Zener Voltage (V_Z).
i.e. *The Zener Diode acts as an ideal voltage source which maintains a constant load voltage, independent of the current.*

REGULATION WITH VARYING INPUT VOLTAGE *(Line Regulation)*

Zener Regulator under varying input voltage condition is shown in Fig.

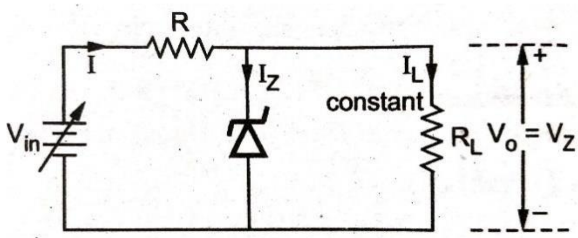


Fig. *Varying input condition*

$Vo = V_Z$ is constant

$$I_L = \frac{Vo}{R_L} = \frac{V_Z}{R_L} = constant$$

And $I = I_Z + I_L$

V_{in} increases →	$I = I_L + I_Z$ increases →	I_L is constant (V_Z/R_L) →	So I_Z increases ($I_Z = I - I_L$) →	As long $I_Z < I_{Zmax}$, V_Z is constant i.e. output voltage is constant
V_{in} decreases →	$I = I_L + I_Z$ decreases →	I_L is constant (V_Z/R_L) →	So I_Z decreases ($I_Z = I - I_L$) →	As long $I_Z > I_{Zmin}$, V_Z is constant i.e. output voltage is constant

As long I_Z is between I_{Zmin} and I_{Zmax}, the V_Z i.e. output voltage V_o is constant. Thus, the changes in the input voltage is get compensated and output is maintained constant.

The **maximum power dissipation** for the zener diode is fixed, $P_D = V_Z\, I_{Zmax}$

REGULATION WITH VARYING LOAD *(Load Regulation)*

Zener Regulator under varying load condition (R_L is variable) and constant input voltage (V_{in} is constant) is shown in Fig.

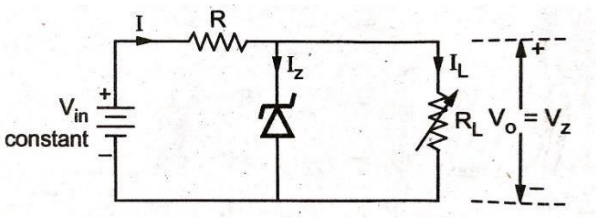


Fig. *Varying load condition*

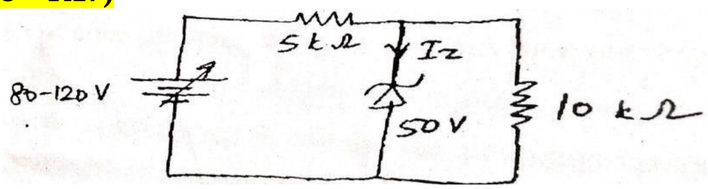
V_o = V_Z is constant and **V_{in}** is Constant, then for constant R, the current (I) is constant.

$I = \frac{V_{in} - V_Z}{R}$ (constant); $I = I_L + I_Z$

R_L increases I_L decreases →	$I = \frac{V_{in} - V_Z}{R}$ constant →	$I_Z = I - I_L$ increases →	As long $I_Z < I_{Zmax}$, V_Z is constant i.e. output voltage is constant
R_L decreases I_L increases →	$I = \frac{V_{in} - V_Z}{R}$ constant →	$I_Z = I - I_L$ decreases →	As long $I_Z > I_{Zmin}$, V_Z is constant i.e. output voltage is constant

As long I_Z is between I_{Zmin} and I_{Zmax} , the V_Z i.e. output voltage V_o is constant. Thus, the changes in the load is get compensated and output is maintained constant.

(b) For the following circuit, find the maximum and minimum values of Zener diode current. **(Nov/Dec 2018 – R17)**



Solution: $V_{in\,(min)} = 80V, V_{in\,(max)} = 120V, \quad V_Z = 50V, \; R_L = 10K\Omega, \qquad R = 5K\Omega$

$$I_L = \frac{V_Z}{R_L} = \frac{50}{10\,X\,10^3} = 5\,X\,10^{-3} = 5mA$$

$$V_{in\,(min)} = V_Z + IR \qquad V_{in\,(max)} = V_Z + IR$$

$$I = \frac{V_{in\,(\min)} - V_Z}{R} \qquad I = \frac{V_{in\,(\max)} - V_Z}{R}$$

$$I_{(min)} = \frac{80 - 50}{5\,X\,10^3} = 6mA \qquad I_{(max)} = \frac{120 - 50}{5\,X\,10^3} = 14mA$$

$$I_{Z\,(min)} = I_{(min)} - I_L \qquad I_{Z\,(max)} = I_{(max)} - I_L$$

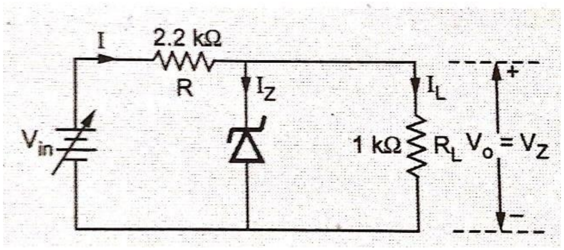
$$I_{Z\,(min)} = 6\,X\,10^{-3} - 5\,X\,10^{-3} = 1mA \qquad I_{Z\,(max)} = 14\,X\,10^{-3} - 5\,X\,10^{-3} = 9mA$$

$\therefore \boldsymbol{Minimum\ zener\ current, I_{Z\,(min)} = 1mA}$ $\qquad \therefore \boldsymbol{Maximum\ zener\ current, I_{Z\,(max)} = 9mA}$

Problems: (Anna University Exam - Solved Problems)

1. **For the zener regulator shown in Fig. 5, calculate the range of input voltage for which output will remain constant.**

$$\boldsymbol{I_{Z\,(min)} = 2.5mA, \quad I_{Z\,(max)} = 25mA, \quad V_Z = 6.1V, \quad r_Z = 0\,K\Omega}$$



Solution:

$I_{Z\,(min)} = 2.5mA, I_{Z\,(min)} = 25mA, \quad V_Z = 6.1V, \quad r_Z = 0\,K\Omega, \quad R = 2.2\,K\Omega, \quad R_L = 1\,K\Omega$

$$I_L = \frac{V_Z}{R_L} = \frac{6.1}{1\,X\,10^3} = 6.1\,X\,10^{-3} = 6.1mA \quad (\boldsymbol{CONSTANT})$$

$For\,V_{in\,(min)};\quad I_{(min)} = I_{z(min)} + I_L$

$I = 2.5\,X\,10^{-3} + 6.1\,X\,10^{-3} = 8.6mA$

$For\,V_{in\,(mzx)};\quad I_{(max)} = I_{Z(max)} + I_L$

$I = 25\,X\,10^{-3} + 6.1\,X\,10^{-3} = 31.1mA$

$V_{in\,(min)} = V_Z + IRV_{in\,(max)} = V_Z + IR$

$V_{in\,(min)} = 6.1 + 8.6\,X\,10^{-3}X\,2.2\,X\,10^{-3} = 25.02V$

$V_{in\,(min)} = 6.1 + 31.1\,X\,10^{-3}X\,2.2\,X\,10^{-3} = 74.52V$

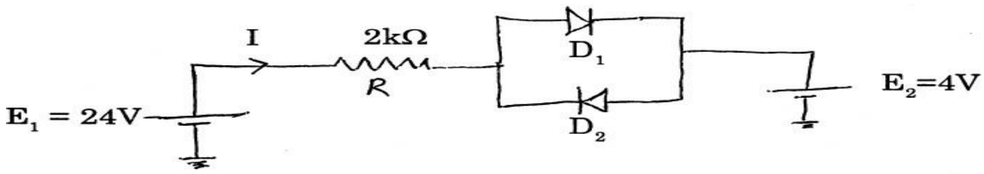
$\boldsymbol{\therefore V_{in\,(min)} = 25.02V} \qquad \boldsymbol{\therefore V_{in\,(max)} = 74.52V}$

2. **A silicon diode has a saturation current 7.5μ A at room temperature 300K.Find the saturation current at 400k. I_{01}=7.5 x 10-6 A at T_1=300° K=27° C and T_2=400 °K=127° C. (Nov/Dec 2016 – R13)**

Solution: The saturation current at 400°K is

$$I_{02}=I_{01} \times 2^{\frac{\Delta T}{10}} = 7.5\,X\,10^{-6}\,X\,2^{(127-27)/10} = 7.68mA$$

3. **Find the current I in the following circuit. (Nov/Dec 2017 – R13)**



Assume the diodes to be of silicon and forward resistance of diodes to be zero.

I = (E1-E2)/R I = (24-4)/2000

I = 1 mA **Current I is 1mA.**

4. **An AC voltage of peak value 20V is connected in series with a silicon diode and load resistance of 500Ω. If the forward resistance of diode is 10Ω find the peak current through the diode. (Nov/Dec 2018-R17)**

Solution: $E_m = 20V, \quad R_L = 500\Omega, \quad R_f = 10\Omega$

$$I_m = \frac{E_m}{R_f + R_L} \qquad I_m = \frac{20}{500 + 10}$$

$$\therefore I_m = 39.22\,mA$$

5. (a) Determine the peak output voltage of a half wave rectifier, if the diode has V_F = 0.7V and the AC input is 22V. (April / May 2019-R17)

Solution: $V_{po} = V_{pi} - V_F$

$V_F = 0.7\,V$, $V_{pi} = \sqrt{2}V_i = \sqrt{2}\,X\,22$, $V_{pi} = 31.1\,V$

$V_{po} = 31.1 - 0.7$, $V_{po} = 30.4\,V$

(b) If load resistance is given as 500Ω, calculate peak output current of the above given half wave rectifier.

Solution: $R_L = 500\Omega$ $I_p = \frac{V_{po}}{R_L} = \frac{30.4}{500}$ $I_p = 60.8\,mA$

(c) Determine the diode peak reverse voltage (PIV). PIV = V_{pi} = 31.1 V

6. What value of series resistor is required to limit the current through a LED to 20 mA with a forward voltage drop of 1.6 V when connected to a 10V supply? (Nov/Dec 2017)

Series resistor, $R_S = \frac{V_S - V_D}{I_F}$

$V_S = 10\text{ V}; \quad V_D = 1.6\text{ V}; \quad I_F = 20\text{ mA} = 20 \times 10^{-3}\text{ A}$

$\therefore \quad R_S = \frac{10 - 1.6}{20 \times 10^{-3}} = \mathbf{420\ \Omega}$

7. In a semiconductor at room temperature(300°K), the intrinsic carrier concentration and resistivity are1.5 * 10^{16}/cm^3 and 2 *10^3Ω-mrespectively. It is to an extrinsic semiconductor with a doping concentration of 10^{20}/cm^3 for the extrinsic semiconductor.
Calculate (a) Majority carrier concentration, (b) Shift in fermilevel due to doping (c) Minority carrier concentration when its temperature is increased to a value at which the intrinsic concentration 'n_i' doubles. (NOV/DEC 2012)

Assume the mobility of majority and minority carriers are same and **KT=26 meT** at room temperature.

a) Minority carrier concentration=$\frac{n_i^2}{\text{Doping concentration}}$

$=\frac{(1.5\times10^{16})}{10^{20}} = 2.25 \times 10^{12}\frac{\text{atoms}}{\text{m}^3}$

We know$\sigma = nq(\mu_n + \mu_p)$

or$(\mu_n + \mu_p) = \frac{\sigma}{nq} = \frac{1}{\rho nq}$

$=\frac{1}{(2\times10^3)(1.5\times10^{16})(1.6\times10^{-19})} = \frac{1}{4.8}$

In this case the concentration of majority and minority carriers are same, thus

$$\mu_n + \mu_p = 2\mu_n = \frac{1}{4.8} \text{ or } \mu_n = o.1042\,\frac{m^2}{\text{Volt} - \text{sec}}$$

b) Because of doping concentration>> minority concentration conductivity.

$\sigma = qn\,\mu_n = (1.6 \times 10^{-19})(10^{20})(0.10242)$=1.6672

Thus resistivity R=$\frac{1}{\sigma}$ = 0.599Ωcm

Shift interm level $E_F$computed as follows

C) $E_A - E_i = KT\ \log e\frac{n_o}{n_i} = 0.026\log_e(\frac{10^{20}}{10^{16}\times15})$

=0.229$_e$V.

Thus E_F lies0.229$_e$V above from fermilevel.

d) Minority carrier concentration=$\frac{(2ni)^2}{\text{doping concentration}}$ $=\frac{[2(1.5\times10^{16})^2]}{10^{20}}$ $= \frac{9\times10^{32}}{10^{20}}$ =9× 10^{12}atoms/cm^3.

Additional Questions: PART-A

1. **Define valence electron.**
Electrons that are in shells close to nucleus are tightly bounced to the atom and have low energy. Whereas electrons that are in shells farther from the nucleus have large energy and less tightly bound to the atom. Electrons with highest energy level exist in the outermost shell of an atom. These electrons determine the electrical and chemical characteristic of each particular type of atom. These electrons are known as valence electrons.

2. **What is meant by energy band?**
In a single isolated atom, the electron in any orbit possesses define energy. Due to an interaction between atoms the electrons in a particular orbit of one atom have slightly different energy levels from electrons in the same orbit of an adjoining atom. This is due to the fact that no two electrons see exactly the same pattern of surrounding charges. Since there are billions of electrons in any orbit, slightly different energy levels form a cluster or band known as energy band.

3. **Define conduction band & valence band.**
   - The conduction band is defined as the range of energies possessed by conduction electrons.
   - Valence band is defined as the range of energies possessed by valence electros.

4. **What are conductors, Insulators and semiconductors?**
   - A conductor is a material, which easily allows the flow of electric current. The best conductors are copper, silver, gold and aluminum.
   - An Insulator is a material that does not conduct electric current. In these materials valence electrons are tightly bound to the atoms.
   - A semiconductor is a material that has an electrical conductivity that lies between conductors and insulators. A semiconductor in it's pure state is neither a good conductor not a good insulator. The most common semiconductors are silicon, Germanium, and carbon.

5. **What are the classifications of semiconductors?**
Semiconductors are classified as intrinsic and extrinsic semiconductors. A pure semiconductor is called intrinsic semiconductor. A doped semiconductor is called extrinsic semiconductor.

6. **What is meant by doping? How the extrinsic semiconductors are classified?**
The process of adding impurities to a semiconductor is known as doping.
   - n-type semiconductor
   - p-type semiconductor

7. **How a *n*-type semiconductor & p-type semiconductor can be obtained?**
   - A n-type semiconductor can be obtained by adding pentavalent impurities to an intrinsic semiconductor. These are atoms with five valence electrons. Typical examples for pentavalent atoms are Arsenic. Phosphorous, Bismuth and Antimony.

   - A p-type semiconductor can be obtained by adding trivalent impurities to an intrinsic semiconductor. These are atoms with three valence electrons. Typical examples for trivalent atoms are boron(B), indium (In) and gallium (Ga).

8. **Define Fermi level.**
Fermi level is the energy at which the probability of occupation by an electron is exactly 0.5.

9. **What is the energy band gap of silicon and Germanium at 300°*K*?**
For Germanium: 0.66_e and for Silicon: 1.12_ev

10. **What are the different types of voltage regulators?**
Based on how regulating element is connected to the load, voltage regulators are classified as
    - Series regulator
    - Shunt regulator
    - Switch-mode regulators or switched mode power supply (SMPS)

Additional Questions (PART-B)

1. Draw and explain the energy band diagram for the following
(i) conductors (ii) Insulators (iii) semiconductors

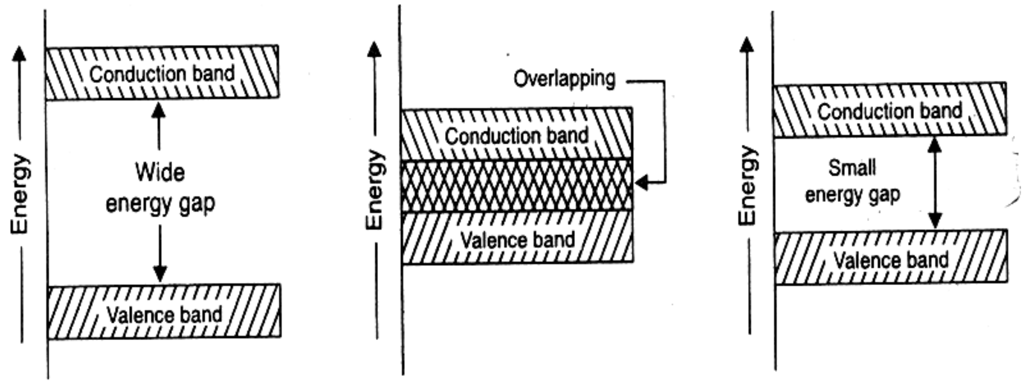
Insulators :

The materials in which the condition band and valence bands are seperated by a wide energy gap (≈ 15 eV) as shown in figure.

A wide energy gap means that a large amount of energy is required, to free the electrons, by moving them from the valence band into the condition band ;

Since at room temperature, the valence electrons of an insulator do not have enough energy to jump in to the condition, therefore insulator do not have an ability to conduct current. Thus insulators have very high resistively (or extremely low conductivity) at room temperatures.

However if the temperature is raised, some of the valence electrons may acquire energy and jump in to the conduction band. It causes the resistively of insulators to decrease.Therefore an insulator have negative temperature co-efficient of resistance.



(*a*) Insulators (*b*) Conductors (*c*) Semiconductors

Conductors :-

The materials in which conduction and valence bands overlap as shown in figure are called conductors. The overlapping indicates a large number of electrons available for conduction.Hence the application of a small amount of voltage results a large amount of current.

Semiconductors :-

The materials, in which the conduction and valence bands are separeated by a small energy gap (1eV) as shown in figure are called semiconductors.

Silicon and germanium are the commonly used semiconductors.

A small energy gap means that a small amount of energy is required to free the elctrons by moving them from the valence band in to the conduction band.

The semiconductors behave4 like insulators at 0K, because no electrons are available in the conduction band.

If the temperature is further increased, more valence elctrons will acquire energy to jump into the conduction band.Thus like insulators, semiconductors also have negative temperature co-efficient of resistance. It means that conductivity of semiconductors increases with the increases tempertature.

2. Explain the classification of semi-conducteurs.

Classification of semi-conducteurs :-

Semiconductors are classified in to two types

- o Intrinsic Semiconductors
- o Exterinsic semi-conducteurs
  - ➢ n-type semi-conductor
  - ➢ p-type semi-conductor

o **Intrinsic seiconductor**

A semiconductor in an extremely pure form is known as an intrinic semiconductor. An Intrinsic semiconductor, even at room temperature, hole-electron pairs all created. When electric field is applied across an semiconductor intrinisic semiconductor, the current conduction takes place by two process, namely by free electrons and holes.

Free electrons are produced due to the breeding up of fome co-valent bonds by thermal energy. At the same time holes are created in the co-valent bond itself.When electric field is applied across the semi-conducteurs material electrons will move towards the positive terminal of supply, holes will move towards negative terminal of the supply.

Thus current conduction inside this intrinisic semiconductor material is due to movement of holes & electrons.

But the current in the external wire is only because of electrons. Since while applying electric field, holes are attracted towards negative terminal. There one new electron is introduced. This electron will combine with the hole, thus cancelling them.

At the same time electrons are moving towards positive terminal, while leacing from this intrinisic material it leaves a hole. Again this holes are attracted towards negative terminal.

- **Extrinisic semiconductor :**

The current conduction capability of intrinisic semiconductor is very low at rom temperature. So we can not use it in electric devices.

Hence the current conduction capability must be increased. This can be achieved by adding impurities to the intrinisic semiconductor. So that it become impurity semiconductor (or) Extrinisic semiconductor.The process of adding impurity is known as doping.

The amount & type of impurities have to be closely controlled during the preparation of extrinisic semiconductor. Generally, for 10^8 atoms of semiconductor, one impurity atom is added.

The purpose of adding impurity is to increase either the number of free electrons or holes in the semiconductor crystal. If the pentavalent impurity is adding to the semiconductor, a large number of free electrons are produced in the semiconductor.

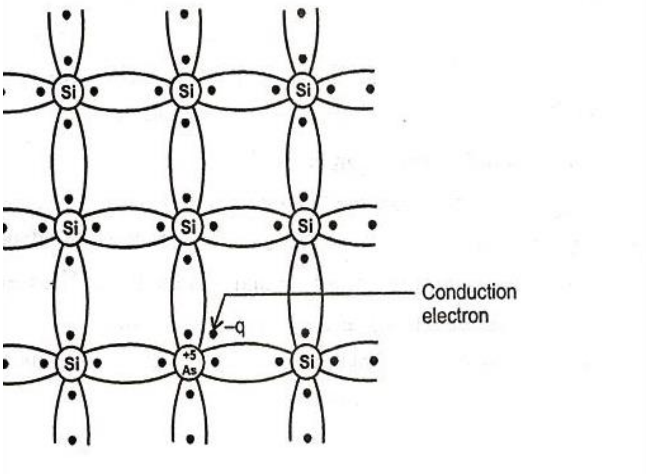
On the other hand if the trivalent impurtiy is added it introdued large number of holes. Depending upon the type of impurity added, extrisic semiconductors are classified into

- n – type Semiconductor
- p – type Semiconductor

n – type Semiconductor :

The number of free electrons in an instrinsic silicon can be increased by adding a pentavalent atom to it. These are atoms with five valence electrons. Typical example for pentavalent atoms are Arsenic, Phosphorous, Bismuth and Antimony.

Four of the pentavalent atoms valence electrons form covalent bond with the valence electrons of Silicon atom, leaving an extra electron. Since valence orbit cannot hold no more than eight electrons the extra electron becomes a conduction electron.



Crystal lattice of a Si atom displaced by arsenic atom

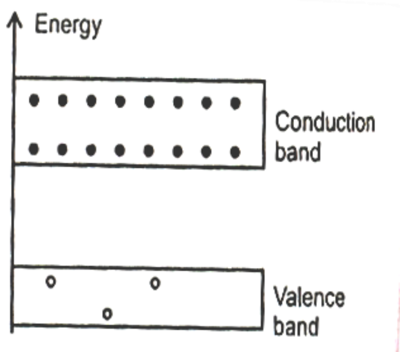
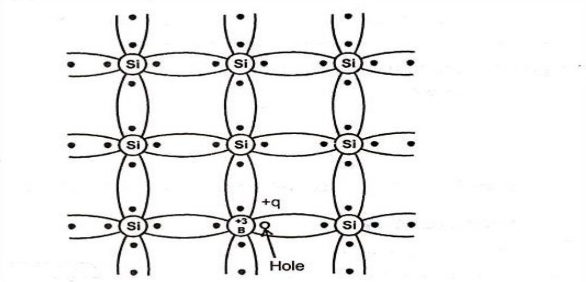


Fig. 1.12 Energy band diagram of a n-type semiconductor

Since the pentavalent atom donnates this extra conduction electron it is often called as a donor atom. For each pentavalent atom added, one free electron exists in a silicon crystal. A small amount of pentavalent impurity is enough to get more number of free electrons is greater than the nuumber of holes this extrinsic semiconductor is known as an n type semiconductor.

When a pentavalent atom is added a number of conduction band electrons are produced. Only a few holes exist in the valence band, created by thermal energy. Therefore in an n-type semiconductor, electrons are majority carriers and holes are minority carriers.

p-type semiconductor



Crystal lattice with a Si atom displaced by Boron atom

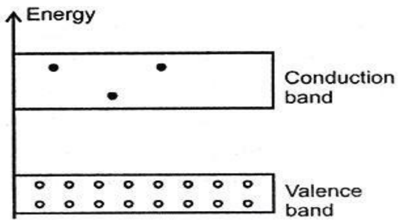


Fig. 1.14 Energy band diagram of a p-type semiconductor

A p-type semiconductor (p for Positive) is obtained by carrying out a process of doping by adding a certain type of atoms (acceptors) to the semiconductor in order to increase the number of free charge carriers (in this case positive holes).

When the doping material is added, it takes away (accepts) weakly bound outer electrons from the semiconductor atoms. This type of doping agent is also known as an acceptor material and the vacancy left behind by the electron is known as a hole.

The purpose of p-type doping is to create an abundance of holes. In the case of silicon, a trivalent atom (typically from Group 13 of the periodic table, such as boron or aluminium) is substituted into the crystal lattice. The result is that one electron is missing from one of the four covalent bonds normal for the silicon lattice. Thus the dopant atom can accept an electron from a neighboring atom's covalent bond to complete the fourth bond. This is why such dopants are called acceptors.

The dopant atom accepts an electron, causing the loss of half of one bond from the neighboring atom and resulting in the formation of a "hole". Each hole is associated with a nearby negatively charged dopant ion, and the semiconductor remains electrically neutral as a whole. However, once each hole has wandered away into the lattice, one proton in the atom at the hole's location will be "exposed" and no longer cancelled by an electron.

This atom will have 3 electrons and 1 hole surrounding a particular nucleus with 4 protons. For this reason a hole behaves as a positive charge. When a sufficiently large number of acceptor atoms are added, the holes greatly outnumber thermal excited electrons. Thus, holes are the majority carriers, while electrons become minority carriers in p-type materials.

EC8353-ELECTRONIC DEVICES AND CIRCUITS

UNIT-II TRANSISTORS & THYRISTORS

PART – A

BJT (Bipolar Junction Transistor)

1. **What is transistor** (BJT)**? What are the types of circuit connections known as configurations, for operating a transistor?**
   Transistor (BJT) is a three-terminal device: ***Base (B), Emitter (E) & Collector (C)***.
   Transistor can be operated in three configurations *Common **B**ase (**CB**), **C**ommon **E**mitter (**CE**) & **C**ommon **C**ollector (**CC**).*
   According to configuration it can be used for ***voltage*** as well as ***current amplification***.

2. **Brief the types of transistors?**
   1. **UJT** *(**U**nipolar **J**unction **T**ransistor)*: In unipolar transistor, the current conduction is only due to one type of charge carriers (majority carriers).
   2. **BJT** *(**B**ipolar **J**unction **T**ransistor)*: In bipolar transistor, the current conduction is only due to both the types of charge carriers *(Holes and Electrons).*

3. **Why an ordinary transistor is called bipolar?**
   Because the transistor operation is carried out by two types charge carriers (both majority and minority carriers).

4. **What are the types of BJT?**
   Types of BJT:
   1. NPN
   2. PNP

5. **Brief the construction of BJT. Draw the symbol and structure and of BJT.**
   BJT is a three- layer semiconductor device consisting of two PN junctions.
   If a layer of P-type material is sandwiched between two layers of N-type the transistor is known as **NPN transistor**.

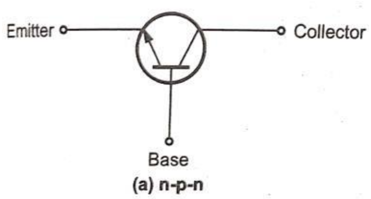


Fig. *Symbol of BJT (NPN type)*

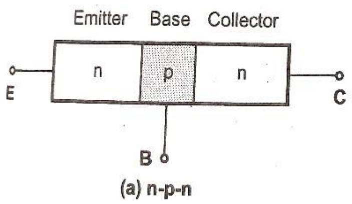


Fig. *Structure of BJT (NPN type)*

On the other hand, if a layer of N-type material is sandwiched between two layers of P-type, the transistor is known as **PNP transistor.**

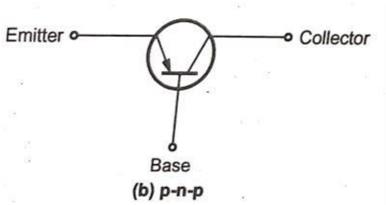


Fig. *Symbol of BJT (PNP type)*

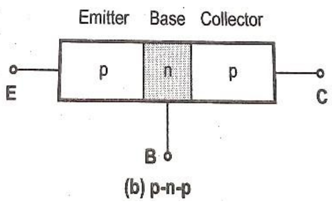


Fig. *Structure of BJT (PNP type)*

6. **Why collector is made larger than emitter and base?**
   Collector is made physically larger than emitter and base because collector is to dissipate much power.

7. **Why the width of the base region of a transistor is kept very Small as compared to other regions?**
   Base region of a transistor is kept very small and lightly doped so as to pass most of the injected charge carriers to the collector.

8. How transistor is used as an amplifier? (OR) Explain the word transistor.

The amplification in the transistor is achieved by passing input current signal from a region of low resistance to a region of high resistance.

{This concept of transfer of resistance has given the TRANSfer-resISTOR (TRANSISTOR)}

9. Why silicon is preferred to germanium while manufacturing semiconductor devices?

As the knee voltage of silicon is higher (0.7V) than the knee voltage of germanium (0.3V), silicon will be more stable for temperature variation than germanium.

10. Why transistor (BJT) is called current controlled device?

The output voltage, current or power is controlled by the input current in a transistor. So, it is called the Current Controlled device.

11. State the advantages of a transistor.

1. Low operating voltage
2. Higher efficiency
3. Small size and ruggedness
4. 4. Does not require any filament power

12. Compare the performance of a transistor in three different configurations. (Nov/Dec 2012) *(OR)* Compare the input resistance, output resistance and voltage gain of CB, CC and CE configuration. (OR) Compare the performance of CE and CC configuration. (May 2017)

Property	CB	CE	CC
Input resistance	Low (about 100Ω)	Moderate (about 750 Ω)	High (about 750 kΩ)
Output resistance	High (about 450 Ω)	Moderate (about 45 Ω)	Low (about 25Ω)
Current gain	1	High	High
Voltage gain	About 150	About 500	Less than 1
Phase shift	0 or 360°	180°	0 or 360°
Between input & output voltages Applications	For high frequency circuits	For audio frequency circuits	For impedance matching

13. Define Early effect? (Nov/Dec 2016)

As the collector voltage V_{CC} is made to increase the reverse bias, the space charge width between collector and base tends to increase, with the result that the effective width of the base decreases. This known as early effect or base width modulation.

14. What is peak point Voltage?

When V_{EE} exceeds the value $(V_D+\eta V_{BB})$, the diode is forward biased and starts to conduct. The value of emitter voltage which makes diode to conduct is called **Peak Point Voltage**.

$$V_p=(V_D+\eta V_{BB})$$

<u>JFET (Junction Field EffectnTransistor)</u>

15. What are the different types of FET?

Types of FET:

1. Junction Field Effect Transistor (JFET)
2. Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

16. Draw the symbol and structure of JFET.

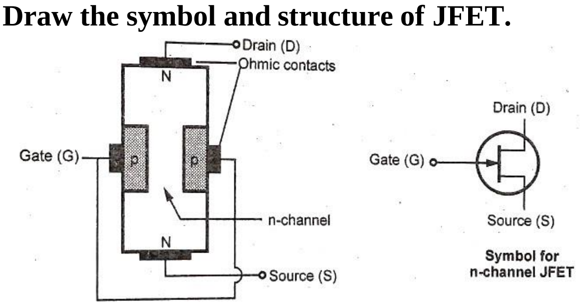


Fig. Structure and for n-channel JFET

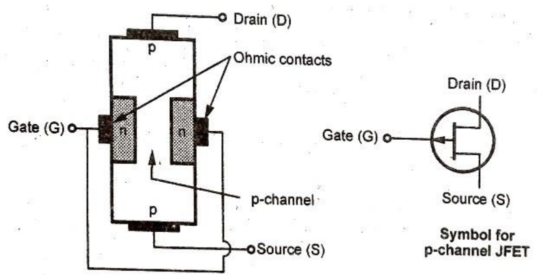


Fig. Structure and for p-channel JFET

17. What are the features of JFET?

a) The operation of JFET depends upon the flow of majority carriers only.
b) The input impedance of JFET is very high, in the order of MΩ.
c) The JFET is less noisy than BJT.
d) It exhibits no offset voltage at zero drain current.
e) It is simple to fabricate.
F) It occupies less space in an integrated circuit.

18. Draw the transfer and drain characteristics curves of JFET? (May / June 2016)

Drain Characteristics:

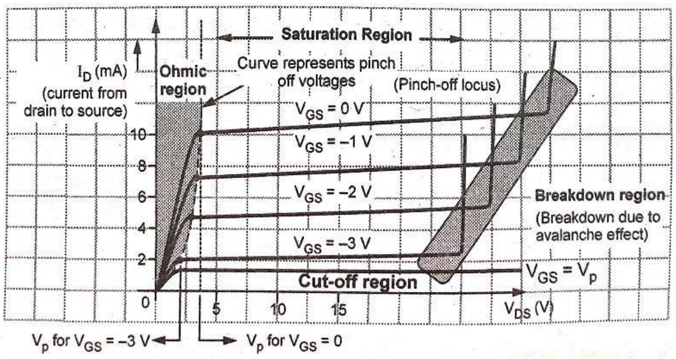


Fig. Drain VI characteristics of n-channel JFET

Transfer Characteristics:

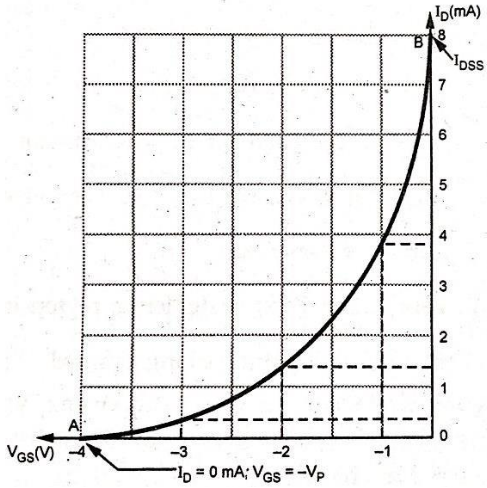


Fig. Transfer characteristics of n-channel JFET

Drain Characteristics:

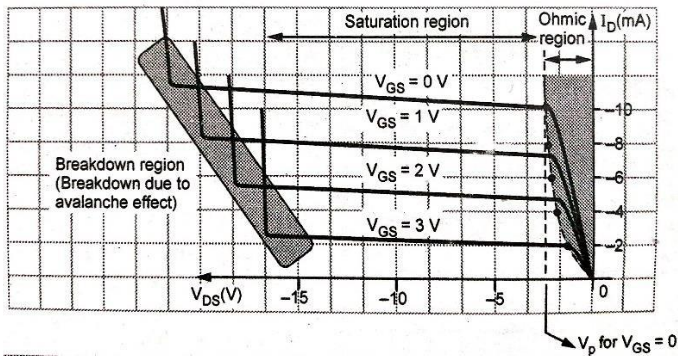


Fig. Drain VI characteristics of p-channel JFET

Transfer Characteristics:

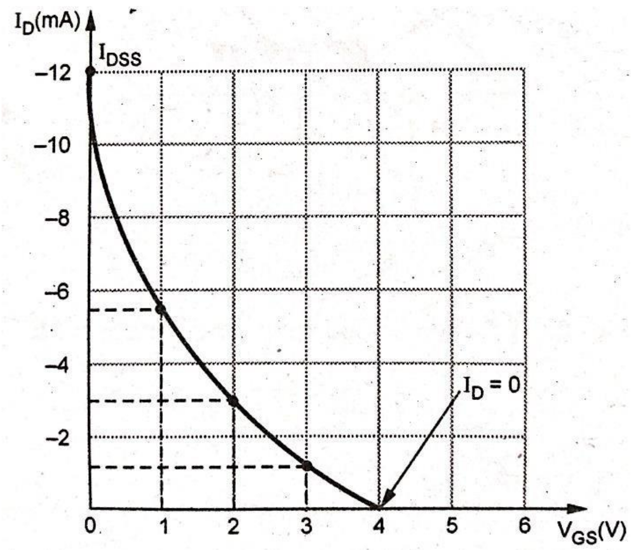


Fig. Transfer characteristics of p-channel JFET

19. Define pinch-off voltage of a FET? (Nov/Dec-2012, May/June-2013)

Pinch-off voltage (V_P) is defined as the drain to source voltage above which drain current becomes almost constant.

20. Mention the disadvantages of FET compared to BJT. (Nov/Dec-2012)

Gain bandwidth product of FET is relatively small as compared to BJT.

21. Define drain resistance.

The drain resistance or output (r_d) is defined as the ratio between change in drain-source voltage (V_{DS}) and change in drain current (I_D) at constant gate-source voltage (V_{GS}).

$$r_d = \frac{\partial V_{DS}}{\partial i_D} \, V_{GS}$$

22. Differentiate FET and BJT (Nov/Dec 2018)

S.No	FET	BJT
1	Unipolar device (that is current conduction by only one type of either electron or hole).	Bipolar device (current conduction by both electron and hole).
2	High input impedance due to reverse bias.	Low input impedance due to forward bias.
3	Gain is characterized by trans conductance	Gain is characterized by voltage gain.
4	Low noise level	High noise level

23. What are the applications of JFET?

a) JFET is used as a buffer in measuring instruments since it has high input impedance and low output impedance.

b) JFET is used in RF amplifier in FM tuners and communication equipment.

c) JFET is used in digital circuit's ii computers and memory circuits because of its small size.

d) It is used oscillators because the frequency drift is low.

24.* FET has lower thermal noise than BJT - Justify.** ***(April / May 2019-R17)

The FET has high gate-to-main current resistance, on the order of 100MΩ or more providing a high degree of isolation between control and flow. Because base current noise will increase with shaping time, a FET typically produces less noise than a Bipolar Junction Transistor (BJT).
Thus, found in noise-sensitive electronics such as tuners and low noise amplifiers for VHF and satellite receivers. It is relatively immune to radiation.

25.* What is the difference between BJT and JFET?** ***(Nov/Dec 2017) (Apr/May 2018) (Nov/Dec 2018-R17)

S. No.	Bipolar junction transistor (BJT)	Junction field effect transistor (JFET)
1	Bipolar device (current conduction is by both electrons and holes)	Unipolar device (current is by only one type of carrier-either electrons or holes)
2	Low input impedance due to forward bias	High input impedance due to reverse bias
3	Current control device	Voltage control device
4	Gain is characterized by voltage gain	Gain is characterized by Tran conductance.
5	High noise level	Low noise level

MOSFET

26. What are the different types of MOSFET? (May/June-2012, 2013)

The modes of operation of the MOSFET are divided into two types.

a) Depletion mode MOSFET
b) Enhancement mode MOSFET

27. What is the other name for MOSFET? (May/June-2012, 2013)

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is also called as I**nsulated Gate** Field Effect Transistor **(IGFET)**

28. **If the gate-to-source voltage in an Enhancement MOSFET is zero, what is the current from drain to source?**
In an Enhancement MOSFET if the gate-to-source voltage is zero, then the current from drain to source is also zero.

29. **What is the major difference in construction of the D-MOSFET and the E-MOSFET?**
The depletion MOSFET has a structural channel, whereas the enhancement-MOSFET does not.

30. **If the gate-to-source voltage in depletion MOSFET is zero, what is the current from drain to source?**
When gate –source voltage is zero for depletion MOSFET, the drain-source current is equal to I_{DSS}. (I_D_I_{DSS})

31. **What are the precautions to be taken when handling MOSFET?**
a) MOSFET should be shipped and stored in a conduction foam rubber.
b) Prior to soldering, the technician should use a shorting strap to discharge his static electricity.
c) The soldering iron tip to be grounded. d) MOSFETs should never be inserted into or removed from a circuit with the power on.
e) The assembler should wear antistatic clothes and ground wrist beads.
f) All the instruments and metal benches used to test the MOS devices should be connected to ground.
g) Always avoid touching the device terminals and pick up the transistor by its casing.

32. **What are the applications of MOSFET?**
a) It can be used as input amplifiers in oscilloscope, electric voltmeters etc.
b) It is used in logic circuits.
c) It is used in computer memories.
d) It is used in phase shift oscillators.
e) It is used in FM and TV receivers.

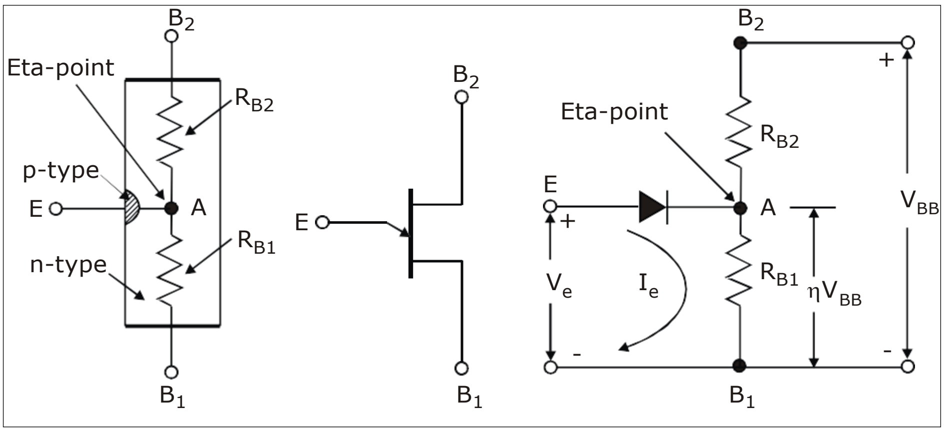
33. **Depletion MOSFET is commonly known as "Normally-ON" MOSFET why?**
The depletion MOSFET can conduct even if the gate to source voltage (V_{GS}) is zero. Because of this reason depletion MOSFET is community known as "Normally-ON" MOSFET.

34. **What is the difference between JFET and MOSFET? (May / Jun 2016)**

S. No.	JFET	MOSFET
1	Reverse bias for gate	Positive or negative gate voltage
2	Gate is formed as a diode	Gate is formed as a capacitor
3	Operation only depletion mode	Can be operated either in depletion mode or in enhancement mode.
4	High input impedance	Very high input impedance due to capacitive effect.

UJT

35. **Draw the structure of UJT. (Nov/Dec 2017)**



36. What is UJT?

Uni junction transistor is a three terminal semiconductor device consisting of only one PN junction. It differs from ordinary PN diode in the sense that it has three terminals namely Emitter, Base 1 and Base 2.

37. Describe the construction of UJT?

UJT consists of lightly doped TV type is semiconductor bar with a heavily doped ***P*** type material.

N type bar is called **base** and ***P*** type region is called **emitter.** Hence ***PN*** junction is formed between emitter and base region.

Since base is lightly doped the resistivity of the base material is very high.

The direction of arrowhead in the UJT symbol represents the conventional direction of current flow when UJT is in conduction state.

38. State two applications of UJT. (Nov/Dec 2018)

1. UJT is used to trigger other devices like SCR.
2. Also used in sawtooth wave generators and some timing circuits.
3. It is used as relaxation oscillator to obtain short pulses for triggering of SCR.

39. What is intrinsic stand OFF ratio of UJT and its equivalent circuit? (May 2017)

The intrinsic stand OFF radio (r|) is defined as the ratio between the internal dynamic resistance ***(R_{Bl})*** and the inter base resistance ***(R_{BB})-***

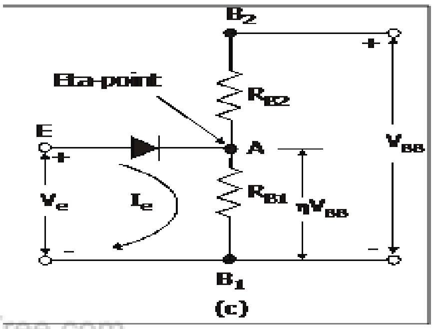
$\eta = \frac{R_{B1}}{R_{B2}}$

Where,

$R_{BB} = R_{B1} + R_{B2}$

R_{B1} – internal dynamic resistance

R_{B2} – inter base resistance



40. What are the different regions in characteristics of UJT?

- Cut off Region
- Negative Resistance Region
- Saturation Region

THYRISTOR

41. Describe the basic structure of SCR?

SCR consist of four semiconductor layers forming a PNPN structure. It has three PN junctions namely J_1 , J_2 anode (A), cathode ***(K)*** and the gate (G).

42. What are the different methods used to turn ON SCR?

1. Gate triggering
2. Forward break over voltage
3. Light triggering
4. Rate - effect (or) triggering

43. What is forward break over voltage? (Apr/May 2018)

SCR is forward bias with a small voltage, it is in 'OFF' and no current flows through the SCR. The applied forward voltage is increased, a certain critical voltage called forward break over voltage ***(V_{B0}).***

44. Define holding current? What is the latching current in SCR? (April / May 2019-R17)

Holding current is the current below which the SCR switches from the conduction state (ON state) to ***the forward blocking state.***

Latching Current is the minimum current required to trigger the device from its OFF state to ON state.

45. What is the forward blocking region?

This region corresponding to the OFF condition of the SCR when anode is positives.

46. What is the turn OFF mechanism used for SCR?

To turn OFF a SCR, the following methods are applied.

(i) Reversing polarity of anode-to-cathode voltage called as Gate turn OFF switch (GTO).

(ii)The second method is anode current interruption. Changing anode current by means of momentarily series or parallel switching arrangement.

(iii)Third method is forced commutation. In this, the current through SCR is reduced below the holding current

47. Give the applications of SCR.

Main applications of an SCR are as a power control device. Common areas of applications include

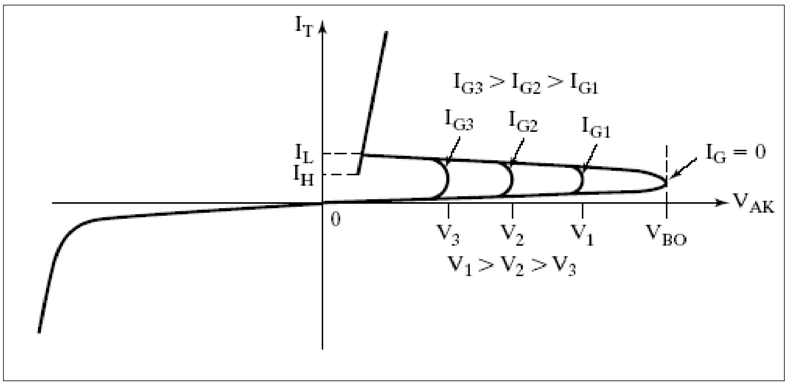
(a). As over light detector
(b). Relay control
(c). Regulated power supplies
(d). Static switches
(e). Motor control
(f). Battery charges
(g). Heater controls
(h). Phase controls
(i). For speed control of DC shunts motor.

48. What are the advantages of SCR?

> SCR controls large current in the load by means of a small gate current.
> SCR size is very compact.
> Switching speed is high.

49. Show how an SCR can be triggered on by the application of a pulse to the gate terminal. (Nov / Dec 2015)

SCR is forward bias with a small voltage, it is in 'OFF' and no current flows through the SCR. The applied forward voltage is increased, a certain critical voltage called forward break over voltage ***(V_{B0}).*** *The forward break over voltage is reduced by application of gate pulses.*



<u>IGBT, DIAC & TRIAC</u>

50. IGBT is a voltage controlled device. Why?

Because the controlling parameter is gate-emitter voltage.

51. Why IGBT is very popular nowadays? MAY/JUNE-2012

1. Lower gate requirements 2. Lower switching losses 3. Smaller snubbed circuit requirements

52. What is DIAC?

A DIAC is two terminal semiconductor device and three-layer bidirectional device, which can be switched from of its OFF to ON state for either negative or positive polarity of applied voltage.

53. What are the applications of DIAC?

The DIAC is used as a triggering device; it is not a control device. It is used in.

- Temperature control
- Triggering of TRIAC
- Light diming circuits
- Motor speed control

54. What is TRIAC?

TRIAC is a three terminal semiconductor switching device which can conduct in either forward or reverse direction. The TRIAC is the combination of two SCR's connected in parallel but in opposite direction.

55. What are the applications of TRIAC?

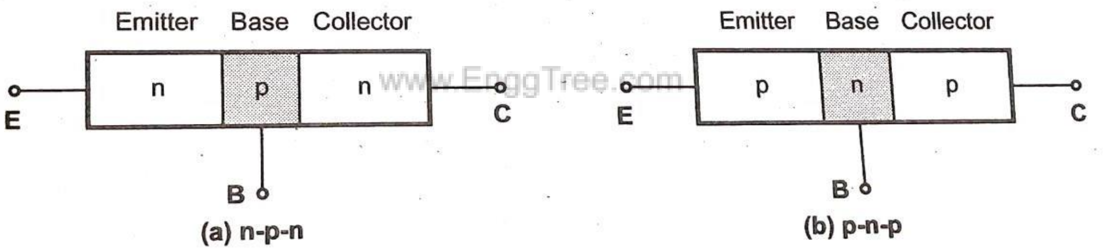
- Heater control
- Phase control
- Light dimming control
- Static switch to turn A.C power ON and OFF.
- Speed control of motor.

PART-B

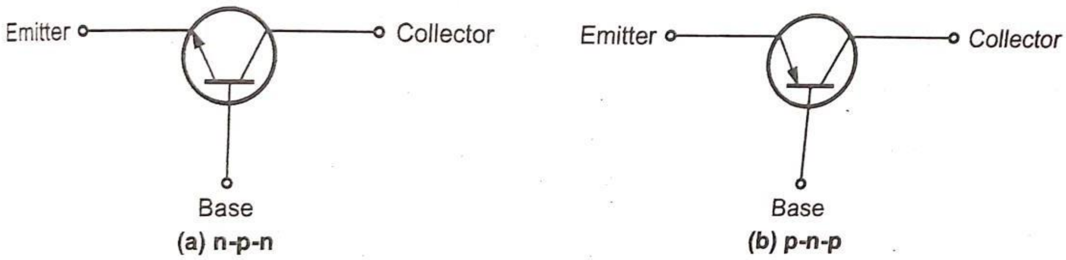
BJT-Structure, Operation & Characteristics

1. Explain about the transistor (BJT) operation.

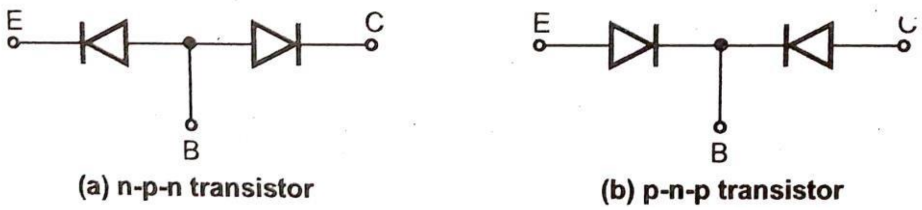
Structure:



Symbol:



Two-diode transistor analogy

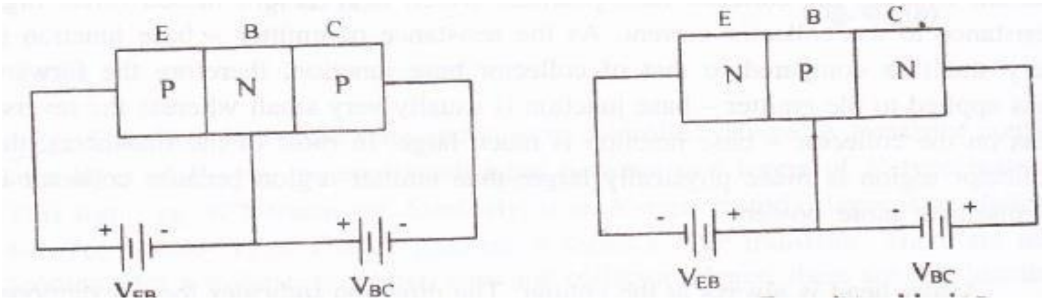


Applying external voltage to a transistor is called biasing. In order to operate transistor properly as an amplifier, it is necessary to correctly bias the two PN junctions with external voltages. Depending upon external bias voltage polarities used, the transistor works in one of the three regions.

1. Active region *2. Cut-off region* *3. Saturation region*

S. No.	Region	Emitter Base	Collector Base	Operation of a transistor
1	Active	Forward biased	Reverse biased	Acts as an amplifier
2	Cut off	Reverse biased	Reverse biased	Acts as an open switch
3	Saturation	Forward biased	Forward biased	Acts as a closed switch

To bias the transistor in its active region the emitter base junction is forward biased, while the collector-base junction in reverse-biased as shown in Fig. The Fig. shows the circuit connections for active region for both NPN and PNP transistors.



Operation of NPN transistor:

As shown in fig. the forward bias applied to the emitter base junction of an NPN transistor causes a lot of electrons from the emitter region to cross over to the base region. As the base is lightly doped with P-type impurity, the number of holes in the base region is very small and hence the number of electrons that combine with holes in the P – type base region is also very small. Hence a few electrons combine with holes to constitute a base current I_B. The remaining electrons (more than 95%) crossover into the collector region to constitute a collector current I_C. Thus the base and collector current summed up give the emitter current i.e. I_E=-(I_C+I_B).

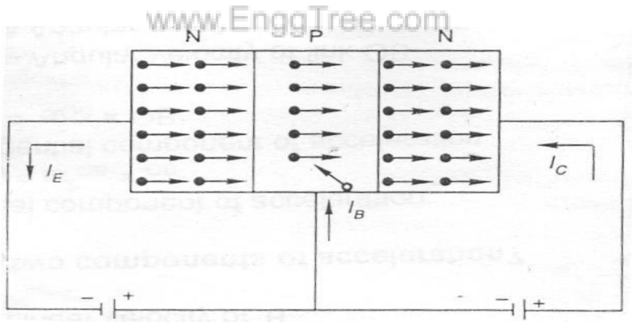


Fig. Current in NPN transistor

In the external circuit of the NPN bipolar junction transistor, the magnitudes of the emitter current I_E, the base current I_B and the collector current I_C are related by I_E=I_C+I_B.

Operation of PNP transistor:

As shown in fig. the forward bias applied to the emitter – base junction of a PNP transistor causes a lot of hoses from the emitter regions to cross over to the base region as the base is lightly doped with N-type impurity. The number of electrons in the base regions is very small and hence the number of holes combined with electrons in the N – type base region is also very small. Hence a few holes combined with electrons to constitute a base current I_B.

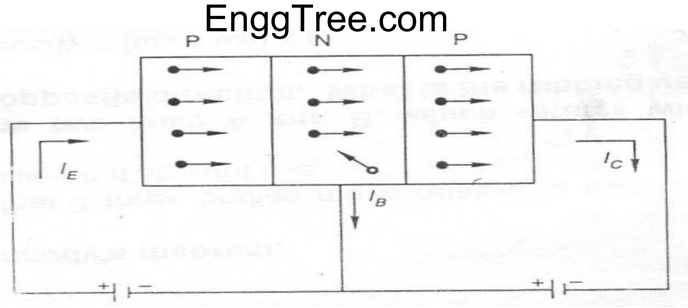


Fig. Current in PNP transistor

The remaining holes (more than 95%) cross over into the collector region to constitute a collector current I_C. Thus, the collector and base current when summed up gives the emitter current.

i.e. $I_E = -(I_C + I_B)$.

In the external circuit of the PNP bipolar junction transistor, the magnitudes of the emitter current I_E, the base current I_B and the collector current I_C are related by

$$I_E = I_C + I_B$$

The equation gives the fundamental relationship between the currents in a bipolar transistor circuit. Also, this fundamental equation shows that there are current amplification factors α and β in common base transistor configuration and common emitter transistor configuration respectively for the static (d.c) currents, and for small changes in the currents.

Large – signal current gain (α). The large signal current gain of a common base transistor is defined as the ratio of the negative of the collector – current increment to the emitter – current change from cut off (I_E=0) to I_E,i.e.

$$\alpha = -\frac{(I_c - I_{CBO})}{I_E - 0}$$

where I_{CBO} (or I_{CO}) is the reverse saturation current flowing through the reverse biased collector – base junction. i.e. the collector to base leakage current with emitter open. As the magnitude of I_{CBO} is negligible when compared to I_E, the above expression can be written as

$$\alpha = \frac{I_C}{I_E}$$

Since I_C and I_E are flowing in opposite directions, α is always positive. Typical value of α ranges from 0.90 to 0.995. Also, α is not a constant but varies with emitter current I_E, collector voltage V_{CB} and the temperature.

2. (a) Explain various characteristics of BJT in Common Base configuration with neat diagram.

Common Base Configuration (CB configuration):

This configuration is also called the grounded base configuration. In this case the input is connected between emitter and base while the output is taken across the collector and base. Thus the base of the transistor is common to both input and output circuits and hence the name, common base configuration. The common base circuit arrangement for NPN transistors is shown in Fig.

Current Amplification Factor (α):

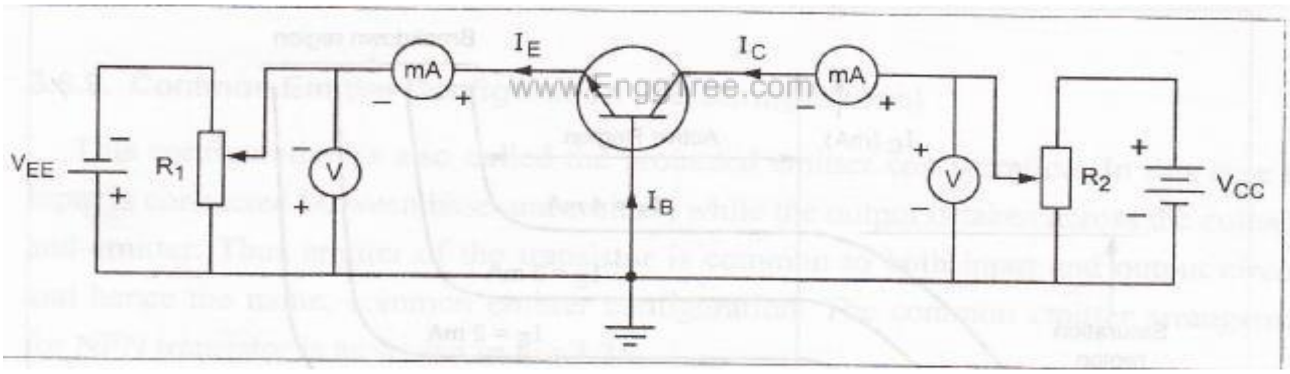
The current amplification factor is defined as the ratio of changes in Collector current (ΔI_C) to the change in emitter current (ΔI_E) when the collector to base voltage (V_{CB}) is maintained at a constant value.

$$\alpha = (\Delta I_C) / (\Delta I_E) \text{ (at constant } V_{CB})$$

The value of α is always less than unity. The practical value of transistors lie between 0.95 and 0.99.

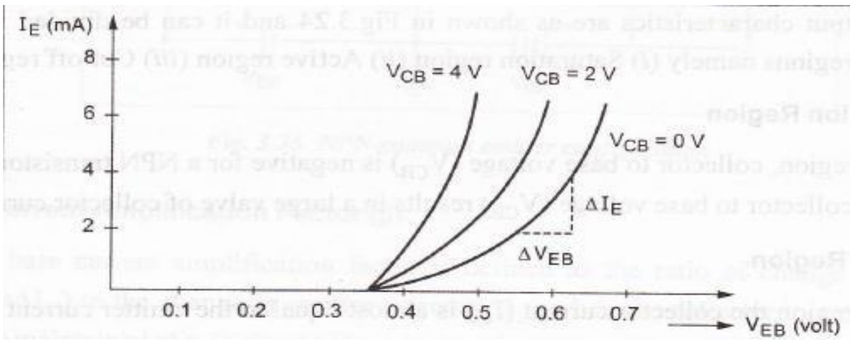
Characteristics of Common Base Configuration:

The circuit arrangement for determining the characteristics of a common base NPN transistors is shown in Fig.In this circuit, the collector to base voltage (V_{CB}) can be varied by adjusting the potentiometer R_2. The emitter to base voltage (V_{EB}) can be varied by adjusting the potentiometer R_1. The DC voltmeters and DC milliammeters are connected in the emitter and collector circuits to measure the voltages and currents.



a). Input Characteristics:

The curve plotted between the emitter current (I_E) and the emitter to base voltage (V_{EB}) at constant collector to base voltage (V_{CB}) are known as input characteristics of a transistor in common base configuration.



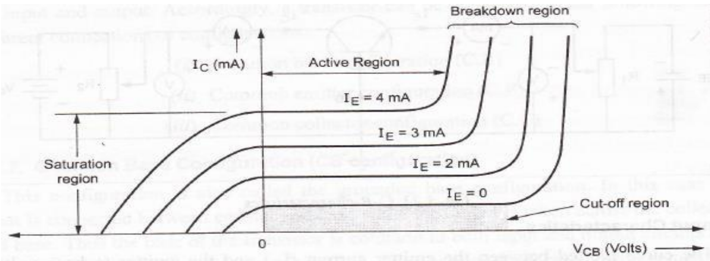
Input Resistance (R_i):

It is the ratio of change in emitter to base voltage (ΔV_{EB}) to the corresponding change in emitter current (ΔI_E) for a constant collector to base voltage (V_{CB}).

$$R_i = \frac{\Delta V_{EB}}{\Delta I_E} \quad \text{(at constant } V_{CB}\text{)}$$

b). Output Characteristics:

The curve plotted between the collector current (I_C) and the collector to base voltage (V_{CB}) at constant emitter current (I_E) are known as output characteristics of a transistor is common base configuration.



The output characteristics are as shown in Fig. and ***it can be divided into three important regions namely (i) Saturation region (ii) Active region (iii) Cut-off region.***

(i). Saturation Region:

In this region, collector to base voltage (V_{CB}) is negative for a NPN transistor. A small change in collector to base voltage (V_{CB}) results in a large valve of collector current.

(ii). Active Region:

In this region the collector current (I_C) is almost equal to the emitter current (I_E). The transistor is always operated in this region. In the active region, the curves are almost flat. A very large change in V_{CB} produces only a very small change in I_C. It means that the circuit has very high output resistance about 500 K Ω.

(iii). Cut-off Region:

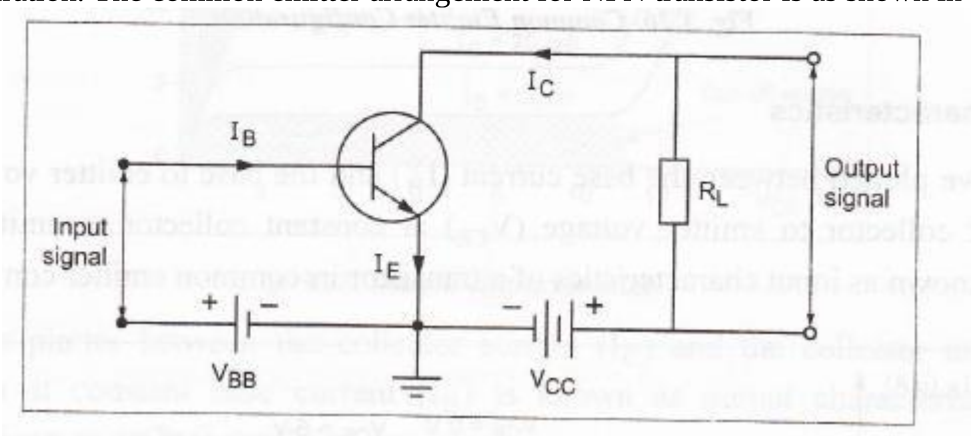
It is the region along the X-axis as shown by shaded or dotted portion. This corresponds to the curve marked I_E=0. In the cut-off region both the junctions of a Transistor are reverse biased. A small collector current flows even when the emitter Current (I_E) is equal to zero.

If the collector to base voltage (V_{CB}) is increased beyond a certain large value, the collector current (I_C) increases rapidly due to avalanche breakdown and the transistor action is lost. This region is called breakdown region.

(b) For a transistor connected in CE configuration, sketch the typical output and input characteristics and explain the shape of characteristics.

Common Emitter Configuration (CE Configuration):

This configuration is also called the grounded emitter configuration. In this case the
input is connected between base and emitter, while the output is taken across the collector and emitter. Thus emitter of the transistor is common to both input and output circuits and hence the name, common emitter configuration. The common emitter arrangement for NPN transistor is as shown in Fig.



Base Current Amplification Factor (β):

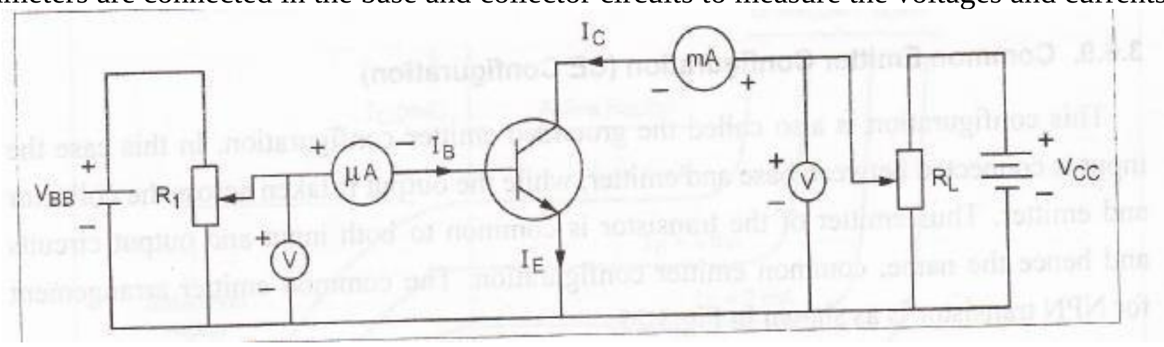
The base current amplification factor is defined as the ratio of change in collector
current (ΔI_C) to the change in emitter current (ΔI_E) when the collector to emitter voltage(V_{CE}) is maintained at a constant value.

$$\beta = \frac{\Delta I_C}{\Delta I_B} \text{ (at constant } V_{CE}\text{)}$$

The value of β is always greater then unity. Practical value of β in commercial
transistors lie between 20 to 500.

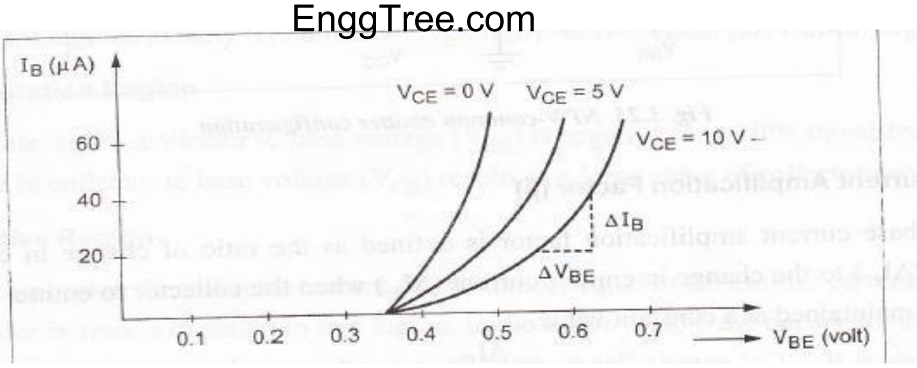
Characteristics of common Emitter configuration:

The circuit arrangement for determining the characteristics of a common emitter NPN transistor is shown inFig.In this circuit, the collector to emitter voltage (V_{EC}) can be varied by adjusting the potentiometer R_2. The base to emitter voltage (V_{BE}) can be varied by adjusting the potentiometer R_1. The DC voltmeters and milliammeters are connected in the base and collector circuits to measure the voltages and currents.



1. **Input Characteristics:**

The curve plotted between the base current (I_B) and the base to emitter voltage (V_{BE}) at constant collector to emitter voltage (V_{CE}) at constant collector to emitter voltage (V_{CE})are known as input characteristics of a transistor in common emitter configuration.

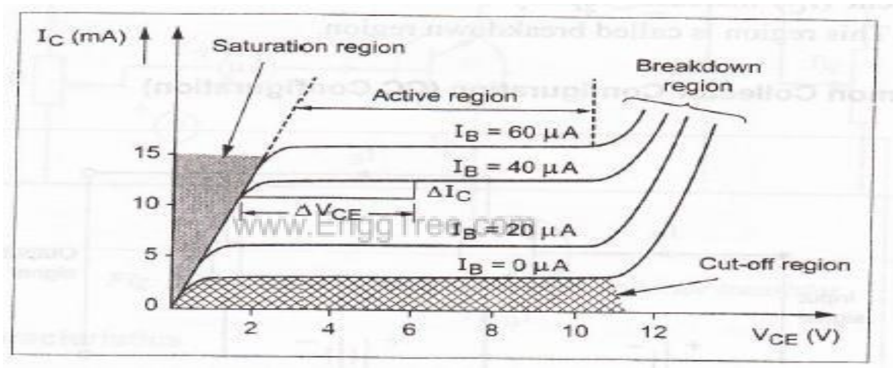


Input Resistance (R_i): It is the ratio of change in base to emitter voltage (V_{BE}) to the Corresponding change in base current (ΔI_B) for a constant collector to emitter voltage (V_{CE}).

$$R_i = \frac{\Delta V_{BE}}{\Delta I_B} \quad \text{(at constant } V_{CE}\text{)}$$

When the collector to emitter voltage (V_{CE}) is increased, the value of base current (I_B) decreased slightly as shown in Fig.

2. Output Characteristics:



The curves plotter between the collector current (I_C) and the collector to emitter Voltage (V_{CE}) at constant base current (I_B) is known as output characteristic of a transistor in common emitter configuration.
The output characteristic may be divided into three important regions namely saturation region, active region, and cut-off region.

(i) Saturation Region:

In this region (shown by dotted area) a small change in collector to emitter voltage (V_{CE}) results in a large value of collector current.

(ii) Active Region:

It is the region between saturation and cut-off region. In this region the curves are almost flat. When the collector to emitter voltage (V_{CE}) is increased. Further, the collector current I. slightly increases. The slope of the curve is little bit more than the output characteristics of common base configuration. Therefore, the output resistance (R_o) of this configuration is less as compared to common base configuration.

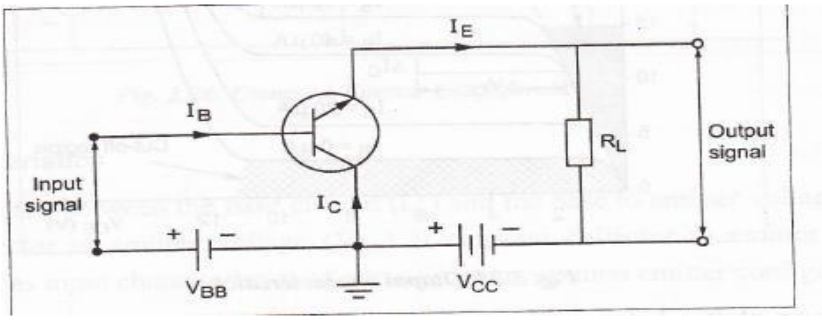
(iii) Cut-off Region:

It is the region along the X-axis is shown by shaded area. This corresponds to the curve marked $I_B = 0$. In the cut-off region both the junctions of a transistor are reverse biased. A small collector current flows even when the base current (I_B) is equal to zero. It is the reverse leakage current (I_{CEo})that flows in the collector circuit.

If the collector to emitter voltage (V_{CE}) is increased beyond a certain large collector current (I_C) increases rapidly due to avalanche breakdown and the action is lost. This region is called breakdown region.

(c) Explain various characteristics of BJT in Common Collector configuration with neat diagram.

Common collector configuration (CC configuration):



This configuration is also called the grounded collector configuration' In this case the input is common between base and Collector. While the output is taken across the emitter and collector. Thus the collector of the transistor is common to both input and output circuits and hence the name common collector configuration. The common collector circuit arrangement for NPN transistor as shown in Fig.

Current Amplification Factor (γ):

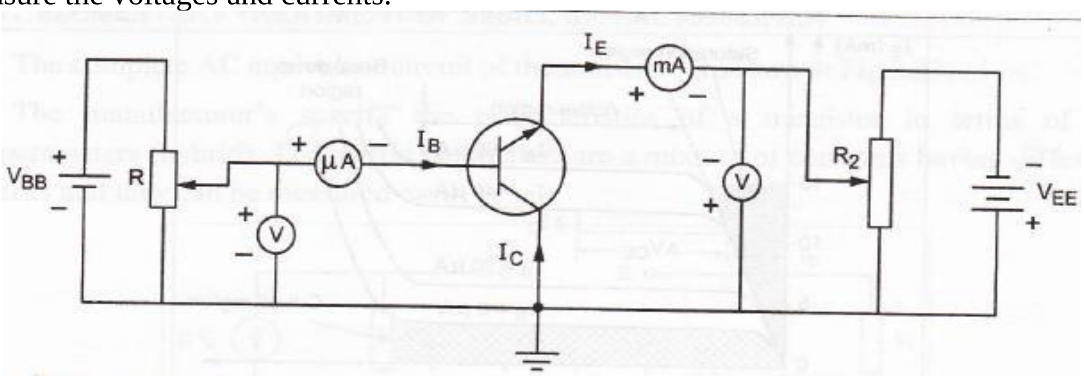
The current amplification is defined as the ratio of change in emitter current (ΔI_E) to the change in base current (ΔI_B). It is generally denoted by γ.

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

The value of γ is nearly equal to β.

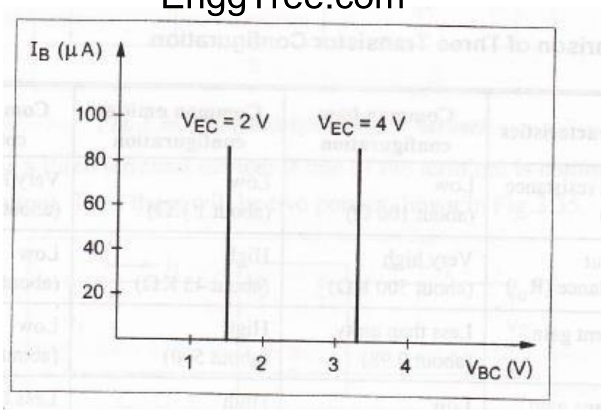
Characteristics of common Collector configuration:

The circuit arrangement for determining the characteristics of a common collector NPN transistor is shown in Fig. In this circuit, the emitter to collector voltage (V_{EC}) can be varied by adjusting the potentiometer R_2. The base to collector voltage (V_{BC}) can be varied by adjusting the potentiometer R_1. The DC voltmeter and millimeters are connected in the base and emitter circuits to measure the voltages and currents.



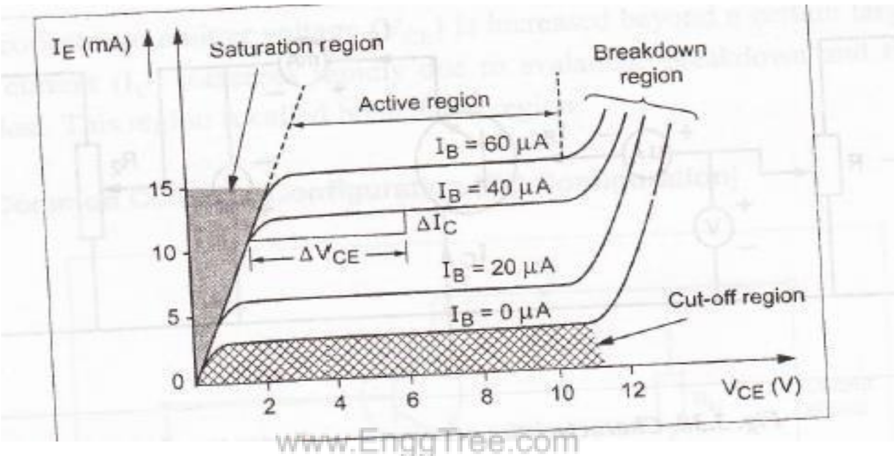
1. **Input Characteristics:**

The curves plotted between the base current (I_B) and the base to collector voltage (V_{BC}) at constant emitter to collector voltage (V_{EC}) are known as input characteristics of a transistor in common collector configuration.



2. Output Characteristics:

The curves plotted between the emitter current (I_E) and the emitter to collector voltage (V_{EC}) at constant base current (I_B) are known as output characteristics of a transistor is common collector configuration.

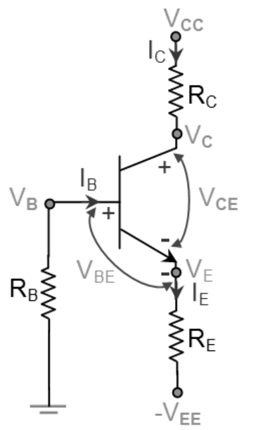


3. Explain the emitter bias method used in transistor amplifier circuits. (Nov/Dec 2017)

Emitter Bias

This biasing network uses two supply voltages, V_{CC} and V_{EE}, which are equal but opposite in polarity. Here V_{EE} forward biases the base-emitter junction through R_E while V_{CC} reverse biases the collector-base junction. Moreover

$$V_E = -V_{EE} + I_E R_E$$
$$V_C = V_{CC} - I_C R_C$$
$$V_B = V_{BE} + V_E$$
$$I_C = \beta I_B$$
$$I_E \approx I_C$$



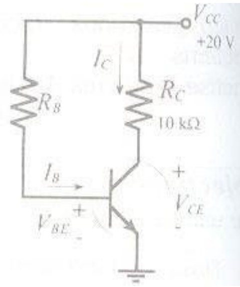
Emitter Bias Circuit

In this kind of biasing, I_C can be made independent of both β and V_{BE} by choosing $R_E >> R_B/\beta$ and $V_{EE} >> V_{BE}$, respectively; which results in a stable operating point.

4. Explain the selection of Q point for transistor bias circuits and discuss the limitations on the output voltage swing. (Nov / Dec 2015)

The dc load line for a transistor circuit is a straight line drawn on the transistor output characteristics. For a common emitter CE circuit. The load line is a graph of collector current versus collector emitter voltage for a given value of collector resistance and a given supply voltage. The load lines show all corresponding levels of I_c and V_{CE} that can exist in a particular circuit.

Consider the common emitter circuit in fig. Note that the polarities of the transistor terminal voltage are such that the base emitter junction is forward biased and the collector base junction is reverse biased. These are the normal bias polarities for the transistor junctions. The dc load line for the circuits in fig drawn on the device common emitter characteristics in fig.



V_{CE} = (Supply voltage) – (Voltage drop across R_C)

$V_{CE} = V_{CC} - I_C R_C$

If the base emitter voltage is zero, the transistor is not conducting and IC = 0. Substituting the V_{CC} and R_C values from fig into equal 5-1

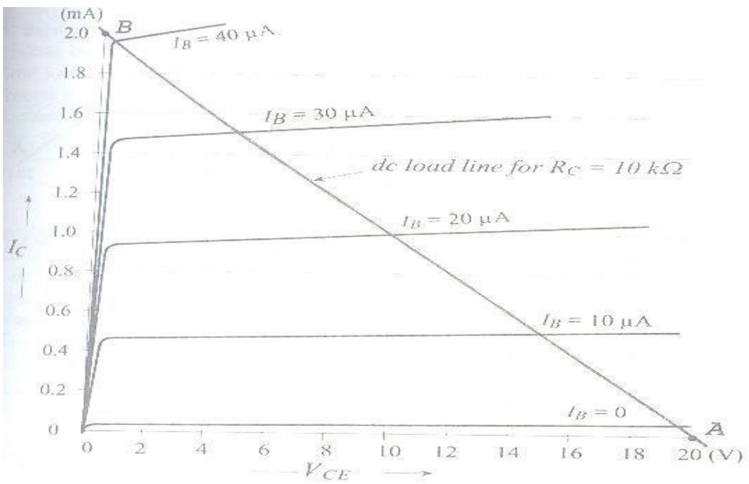
V_{CE} = 20V – (0*10k ohms) =20V

Plot point A on the common emitter characteristics in fig. 5-2 at I_c = 0 and V_{CE} = 20V. This is one point on the dc load line.

Now assume a collector current of 2mA, and calculate the corresponding collector emitter voltage level.

V_{CE} = 20V-(2mA*10k ohms) =0V

Plot point B fig 5-2 at VCE = 0 and I_C = 2mA. The straight line drawn though point A and point B is the dc load line for R_C = 10kohms and V_{CC} = 20V. If either of these two quantities is changed, a new load line must be drawn.



As already stated the dc load line represents all corresponding I_C and V_{CE} levels that can exist in the circuit as represented by Eq. 5-1 for example a point plotted at V_{CE} = 16V and I_C = 1.5mA on fig 5-2 does not appear on the load line. This combination of voltage and current cannot exist in this particular circuit. Knowing any one of I_B, I_C, or V_{CE}, it is easy to determine the other two from a dc load line drawn on the device characteristics. It is not always necessary to have the device characteristics in order to draw the dc load line. A simple graph of I_C versus V_{CE} can be used as demonstrated in example 5-1.

Limitation on the output voltage swing:

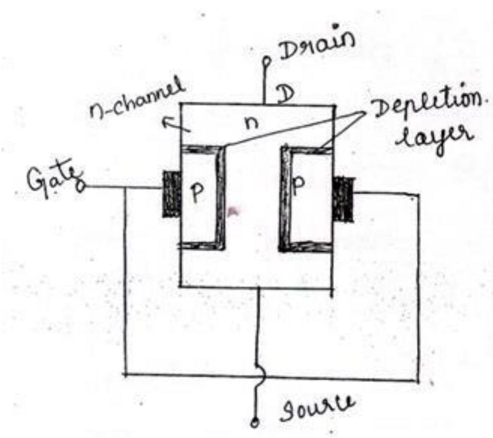
The maximum possible transistor collector emitter voltage swing for a given circuit can be determined without using the transistor characteristics. For convenience, it may be assumed that I_c can be driven to zero at one extreme and to V_{cc} / R_c at the other extreme, [see fig]. This changes the collector emitter voltage from $V_{CE} = V_{cc}$ to $V_{CE} = 0$, as illustrated in fig. thus with the Q point at the center of the load line, the maximum possible collector voltage swing is seen to be approximately $\mp V_{cc}/2$.

JFET- Structure, Operation & Characteristics

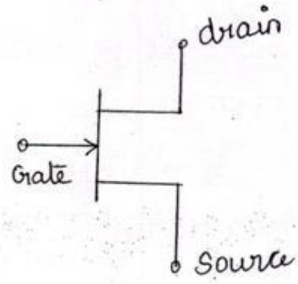
5. **(a) Explain construction and operation of Junction Field Effect Transistor (JFET)? (NOV/DEC 2012) (May/June-2012)**
(b) Explain drain and transfer characteristics of JFET? (May 2017)

(a) Construction and operation:

The basic construction of an n-channel JFET is shown in fig. It consists of an n-type silicon bar referred as the channel. Two small pieces of p-type material are attached to its sides forming pn junctions. If the bar is of n-type the JFET is called as on n-channel JFET, and if the bar is of p-type it is called a p-type channel JFET fig shows schematic diagram of both types of FET's with their symbols.

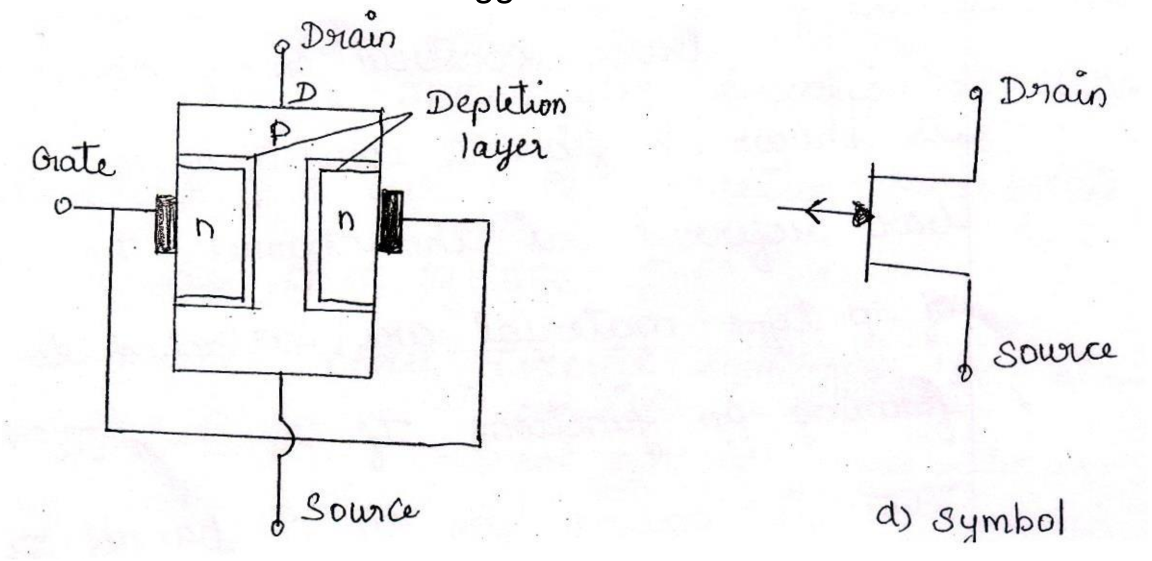


N-channel JFET



Symbol

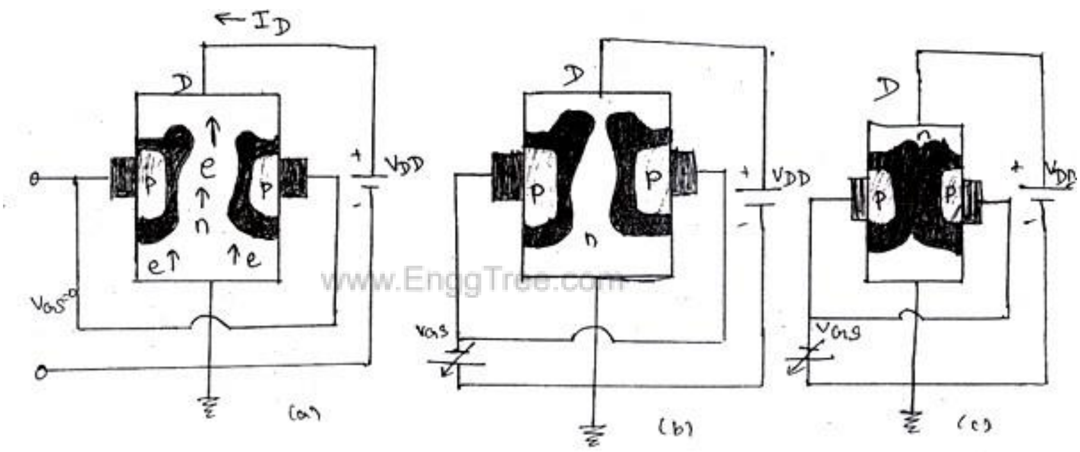
The channel ends are designated as source(S) and drain (D). The source S is the terminal through which the majority carriers enters the bar and drain D is the terminal through which the majority carriers leave the bar. The two p-regions, which are formed by alloying or by diffusion, are connected together and their terminal is called gate. When no bias applied to JFET, depletion regions are formed at two pn junctions as shown in fig. Recall that depletion region is a region depleted of charge carriers and therefore behaves insulators



P-channel JFET

Operation of N-channel JFET

When Vds is of some fixed positive value and reverse bias on Vgs increasing.



Operation of N-channel JFET

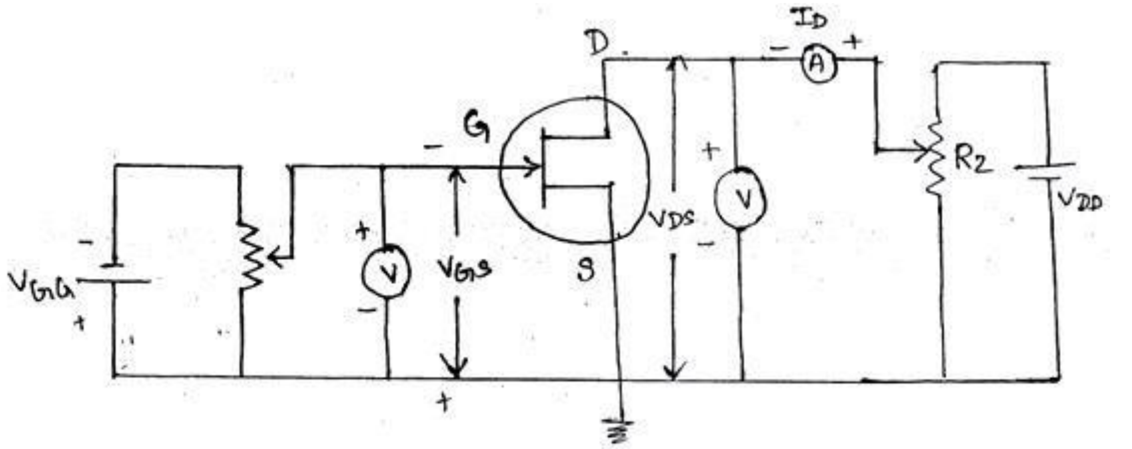
Let us assume that the gate is not biased and a fixed positive voltage is applied between the drain and source terminals as shown in fig. Due to this applied voltage will move through the n-type channel from source to drain. When the gate is negative biased with respect to source, the pn junction are reverse biased and the depletion region are formed. Since the channel is lightly doped compared to heavily doped p-region, the depletion region penetrates deeply into the channel. As a result, the effective channel resistance significantly and reduces the drain current I_D. If the reverse biased on the gate is increased further the depletion will cover the entire width of the channel and ID is cut off completely fig.

2.V_{GS}=0, V_{DS} is varied

First assume that the gate source voltage (V_{GS}) is set to the zero. When the drain source voltage V_{DS} is also zero, the current flowing through FET is also zero that is I_D=0.The instant the voltage V_{DS} is applied, electrons starts flowing from source to drain terminals establishing the current I_D under this condition the channel between drain and source act as a resistance.

(b) Characteristics of JFET:-

The circuit diagram to obtain the characteristics of JFET is shown in fig.



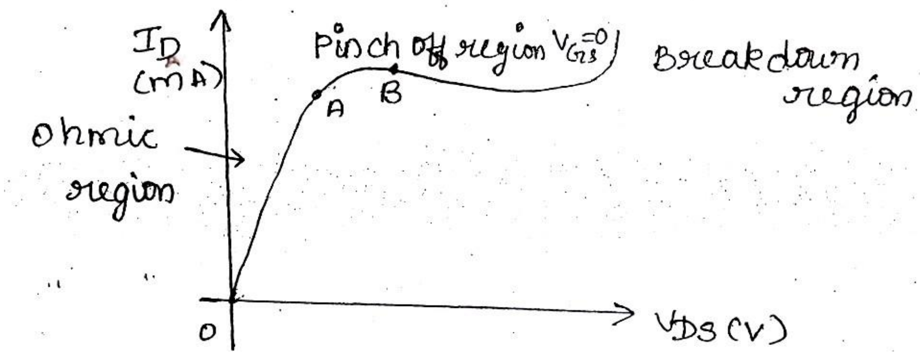
The characteristics that we consider are

i) Drain characteristics ii) Transfer characteristics

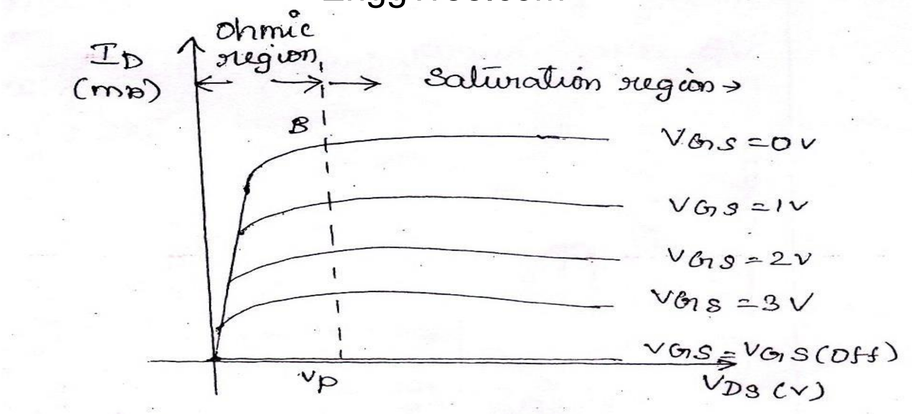
In drain characteristics the relation between Id and VDS for different values of VGS is plotted. In transfer characteristics the relation between ID and VDGS for constant is plotted.

(i) Drain characteristics with V_{GS}=0 (May 2017)

The drain characteristics for V_{GS}=0 is shown in fig. To plot this characteristic the gate to source voltage is kept at zero and V_{DS} is varied from zero. When V_{DS} is zero the drain current I_D is also zero. When V_{DS} is increased the drain, current starts flowing through the channel and FET behaves like a resistor till point A. That is for low values of V_{DS}, current varies directly with voltage following ohm's law. The portion of characteristics where the FET behaves like a resistor is known as ohms region. The FET can be used as a voltage variable resistor in this region if we increase V_{DS}, a stage is reached at which pinch off occurs and the drain current reaches a saturation level. The drain to source voltage at which pinch off occurs is known as pinch off voltage V_P, and corresponding I_D is known as I_{DSS}. The point B at which pinch-off occurs is shown in fig. Even if we increase V_{DS} above V_P the drain current V_{DS} above Vp the drain current does not increase. The region where the drain current is constant inspite of the variation in V_{DS} is known as pinch-off region. If we increase V_{DS} for there a stage is reached at which the gate channel junction FET breakdown and increase rapidly. This region in the characteristics is known as breakdown region. When a bias (-1V) is applied between gate source the pinch off occurs at less drain current less than I_{DSS}. The drain characteristics for different values of V_{GS} shown fig.



Characteristics of JFET for VGS=0



Characteristics of JFET for different values of V_{GS}

(ii) Transfer characteristics

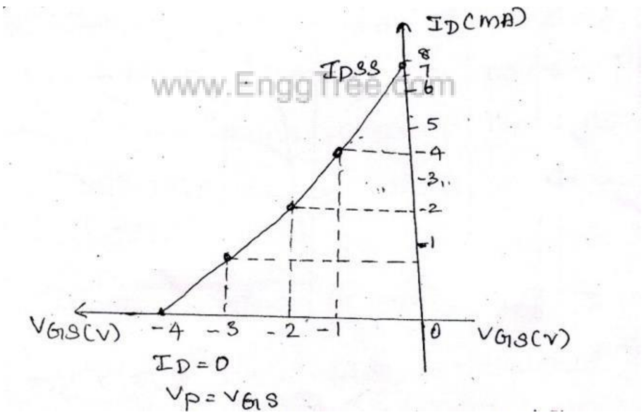
It is a plot of drain current Id versus V_{GS} constant values. To plot the characteristics V_{DS} is kept constant and V_{GS} is varied. When V_{GS}= the current flowing the FET is Equal to I_{DSS} and when V_{GS}=V_{GS} (off), the drain current is zero.

Shockley's equation:-

The relation between V_{GS} and I_D can be represented by Shockley's equation

$I_D = I_{DSS}(1-V_{GS}/Vp)^2$..3.1

Using this mathematically expression, we can develop the plot of I_D versus V_{GS} for any JFET, provide the two parameters I_{DSS} and Vp are known.



Transfer characteristics of JFET.

<u>MOSFET- Structure, Operation & Characteristics</u>

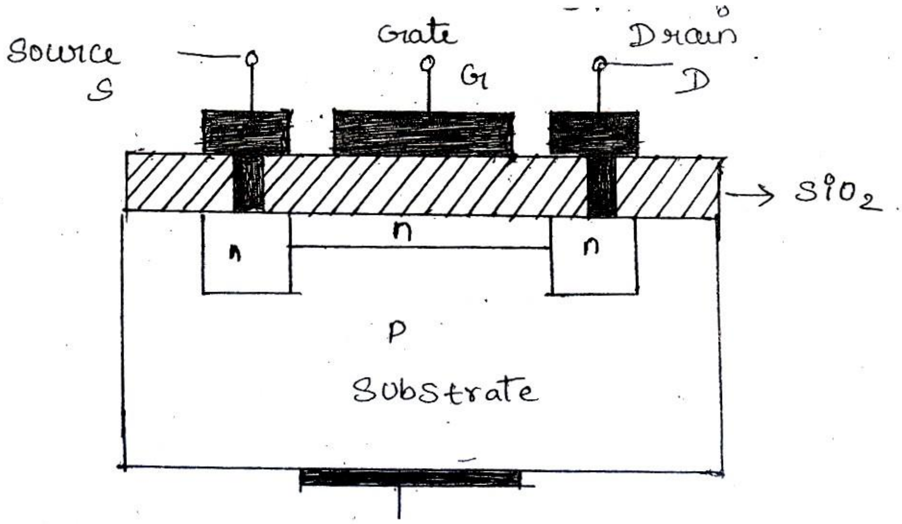
6. **With neat diagram explain the construction & working of depletion MOSFET and enhancement MOSFET with its necessary characteristics curve.** ***(Nov/Dec 2018 R-13) (May/June 2016) (Apr/May 2018)***

OR

Brief about the construction and operation of *n-channel depletion type MOSFET* with a neat diagram. Enumerate the characteristics of *depletion type* MOSFET with a suitable graph. (April/May 2019-R17)

Depletion MOSFET:

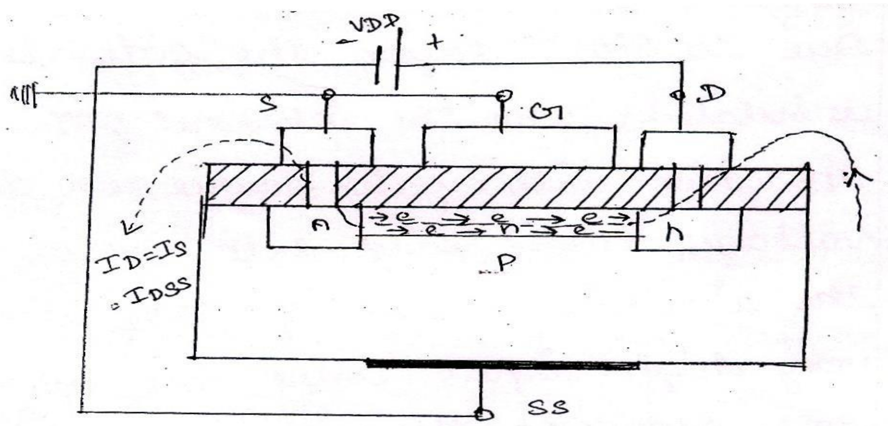
- The construction of an N-channel depletion MOSFET is shown in fig. If consists of a lightly doped p-type substrate in which two highly doped n-regions are diffused. The two heavily doped n-regions act as the source and drain. A lightly doped n-type channel is introduced between the two heavily doped source and drain. A thin layer of (1µm thick) silicon dioxide is coated on the surface. Holes are cut in the oxide layer to make contact with n-regions due to sio_2 layer the gate is completely insulated from the channel. This permits operation with gate source or gate channel voltages above and below zero. In addition the insulated layer of sio_2 accounts for very high input impedance of MOSFET. In some MOSFETS the p-type substrate is internally connected to source, whereas in many discrete devices an additional terminal is provided for substrate labeled SS.



SS substrate

Basic operation:

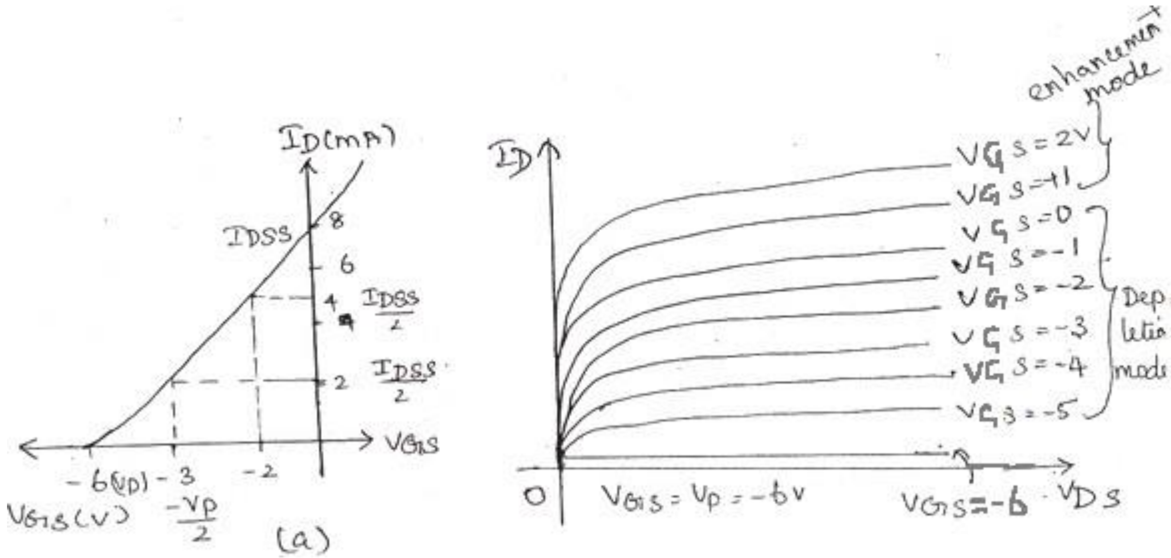
In fig a voltage VDS is applied between the drain and source terminals and the gate to source voltage is set to zer. As a result, current is established from drain to source (conventional direction) similar to JFET like in JFET, the satuarated drain current IDSS flow during pinch-off and it is labeled as IDSS.



If a negative voltage is applied to gate with repeat to source. These holes recombine with electrons and reduce the number of free electrons in the n-channel available for conduction. The more negative the bias, lesser the number of free electrons in the channel. Since the negative voltage on the gate deplete channel, the device is referred to as depletion MOSFET. The depletion mode of operation is similar to JFET operation. When sufficient negative voltage is applied to gate the channel may be completely cut off and the corresponding V_{GS} is called (V_{GS} (OFF)).

If a positive voltage is applied to gate with respect to source then the electrons are induced in the channel. The induced electrons constitute additional current from source to drain. If we increase V_{GS} more in positive direction more number of electrons is induced and hence the drain current increases.

That is, the application of a positive gate –to –source voltage has enhanced the number of charge carriers compared to that of when V_{GS}=0v. For this reason the mode in which the MOSFET. Operates for positive values of gate-to-source voltage is known as enhancement mode.

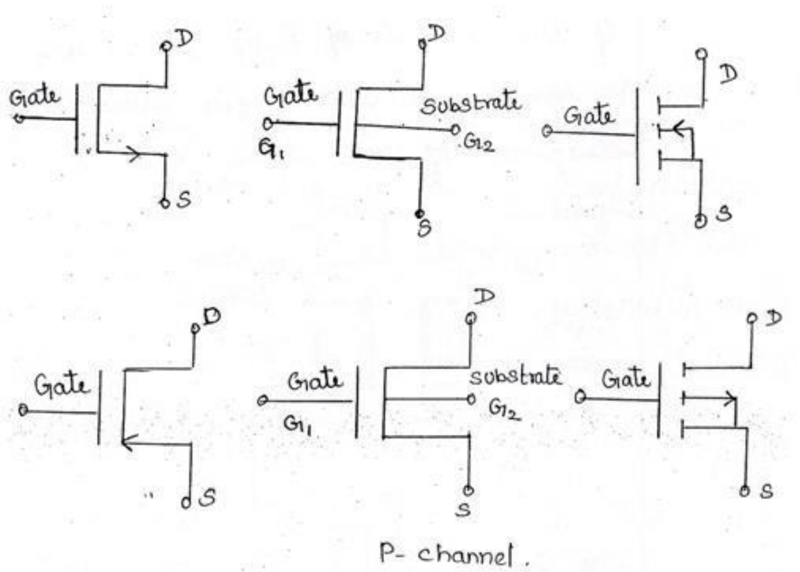


It is a plot of drain current versus drain source voltage for various value of gate-source voltage. The drain characteristics of depletion MOSFET is shown ii fig. Note that for negative of V_{GS} the characteristics of depletion MOSFET is similar to those N-channel JFET. If the gate is made positive additional carrier are introduced in the channel and the channel conductivity increases. Therefore the depletion MOSFET consists of two regions of operation

.

The transfer characteristics of deletion MOSFET is shown in fig. The general shape of the transfer characteristics is similar to those for the JFET. However the deletion MOSFET can be operated with V_{GS}>0. As a result IDSS is not maximum drain current as it is for JFET. The equation fior transfer characteristics curve of depletion MOSFET is same as that of JFET.

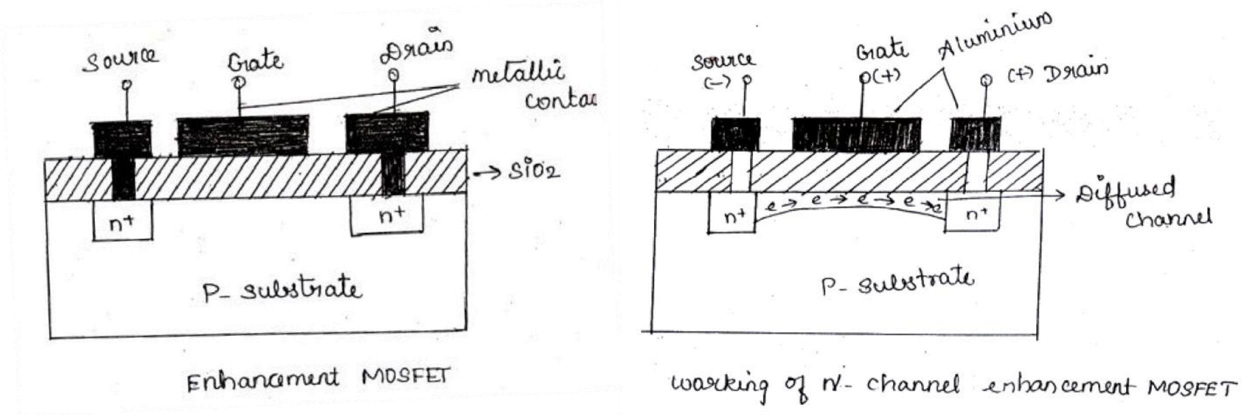
The three circuit symbols for n-channel MOSFET and p-channel MOSFET are shown in fig.



Symbol of N-channel and P-channel MOSFET'S

<u>N-channel enhancement MOSFET</u> ***(May/June-2013), (May/June2016), (Nov/Dec2015) (May 2017) (Apr/May 2018)***

- The construction of *n-channel enhancement MOSFET* is shown in fig. like depletion MOSFET it also consists of a p-type substrate and two heavily doped n-regions that act as source and drain. The sio_2 layer is present to isolate the gate from the region between the drain and source. The source and drain terminals are connected through metallic contacts to n-doped regions. But the enhancement MOSFET does not contain diffused channel MOSFET does not contain diffused channel between the source and drain

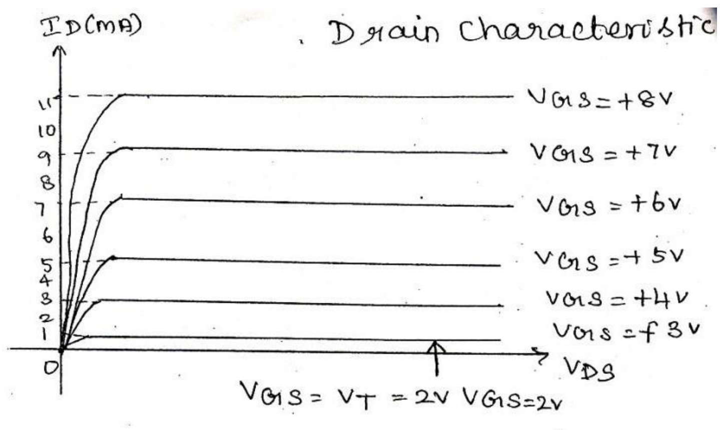


When the drain is made positive with repeat to source and no potential is applied to gate due to absence of the channel, a small drain current (ie., a reverse leakage current) flows. The we apply a positive voltage to that gate with respect to source and substrate, negative charge carriers are induced in the substrate the negative charge carriers which are minority carriers in the p-type substrate form an "inversion layer". As the gate potential is increased more and more negative charge carriers are induced. There negative carriers that are accumulated between source and drain current flows from source to drain through the induced channel. The magnetized of the drain current depends on the gate potential. Since the conduction of the channel is enhanced by the positive bias voltage on the gate the device known as enhancement MOSFET.

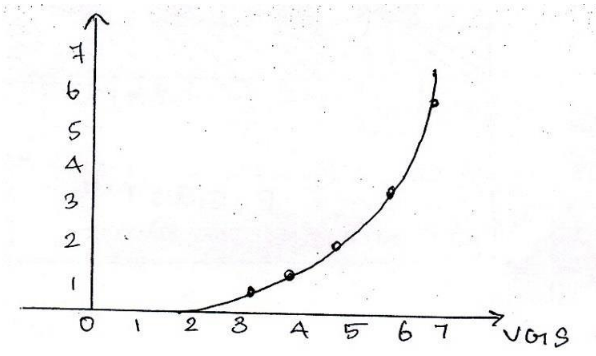
Drain characteristics :

The drain characteristics of enhancement MOSFET is shown in fig.

The current IDSS for VGS=0 is very small of the order of nano amperes shown in fig. Note that the drain current increases with positive increases with positive increase in gate source have voltage.



Transfer characteristics:



The n-channel enhancement MOSFET requires a positive gate to source voltage for its operation fig shows the general transfer characteristics of an n-channel MOSFET. Since the drain current is zero for VGS=0, the IDSS is zero for this device. As VGS is made positive the current ID increases slowly at first and then more rapidly with an increase in VGS. The gate source voltage at which there is significant increase in drain current is called the threshold voltage and is referred to as VT or VGS the equation for the transfer characteristics of enhancement MOSFET differs as the curve states at VGS(th) rather than at VGS. The equation for transfer characteristics is I_D=K$(V_{GS}-V_{GS(th)})^2$

UJT (UNIJUNCTION FIELD EFFECT TRANSISTOR)

7. **(a) Explain the construction operation and characteristics of UJT? (May/June2016), (Nov/Dec2015) (Nov/Dec 2018)**
(b) Describe the operation of UJT as a relaxation oscillator and derive its frequency of oscillation? (Nov/Dec 2016)

(A) UNI-JUNCTION TRANSISTOR (UJT)

Construction:

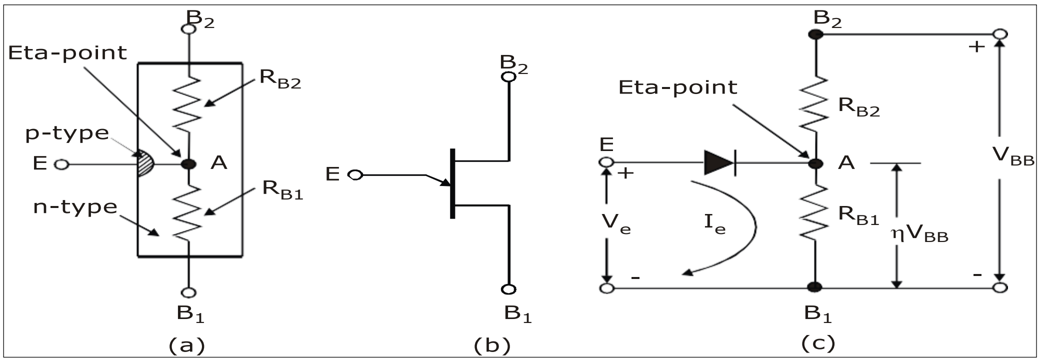


Fig.: (a) Basic structure of UJT (b) Symbolic representation (c) Equivalent circuit

UJT is an n-type silicon bar in which p-type emitter is embedded. It has three terminals base1, base2 and emitter 'E'. Between B_1 and B_2 UJT behaves like ordinary resistor and the internal resistances are given as R_{B1} and R_{B2} with emitter open $R_{BB} = R_{B1} + R_{B2}$. Usually the p-region is heavily doped and n-region is lightly doped. The equivalent circuit of UJT is as shown. When V_{BB} is applied across B_1 and B_2, we find that potential at A is

$$V_{AB1} = \frac{V_{BB}R_{B1}}{R_{B1}+R_{B2}} = \eta V_{BB}\left[\eta = \frac{R_{B1}}{R_{B1}+R_{B2}}\right]$$

η is intrinsic standoff ratio of UJT and ranges between 0.51 and 0.82. Resistor R_{B2} is between 5 to 10KΩ.

OPERATION

When voltage V_{BB} is applied between emitter 'E' with base 1 B_1 as reference and the emitter voltage V_E is less than $(V_D + \eta V_{BE})$ the UJT does not conduct. $(V_D + \eta V_{BB})$ is designated as V_P which is the value of voltage required to turn on the UJT. Once V_E is equal to $V_P \equiv \eta V_{BE} + V_D$, then UJT is forward biased and it conducts.

The peak point is the point at which peak current I_P flows and the peak voltage V_P is across the UJT. After peak point the current increases but voltage across device drops, this is due to the fact that emitter starts to inject holes into the lower doped n-region. Since p-region is heavily doped compared to n-region. Also holes have a longer life time, therefore number of carriers in the base region increases rapidly. Thus potential at 'A' falls but current I_E increases rapidly. R_{B1} Acts as a decreasing resistance.

The negative resistance region of UJT is between peak point and valley point. After valley point, the device acts as a normal diode since the base region is saturated and R_{B1} does not decrease again.

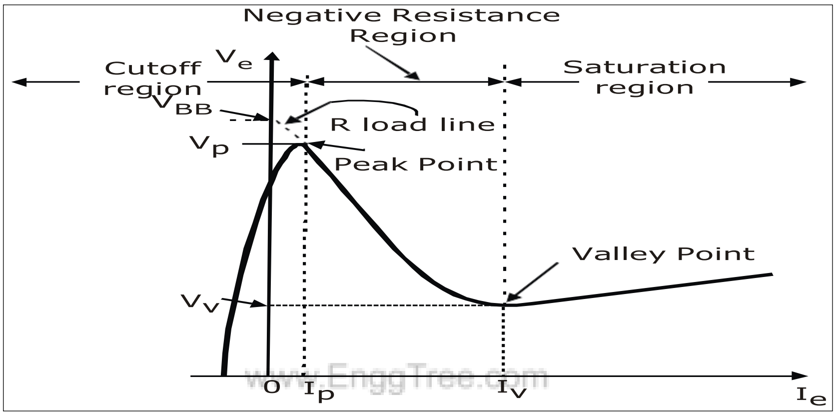


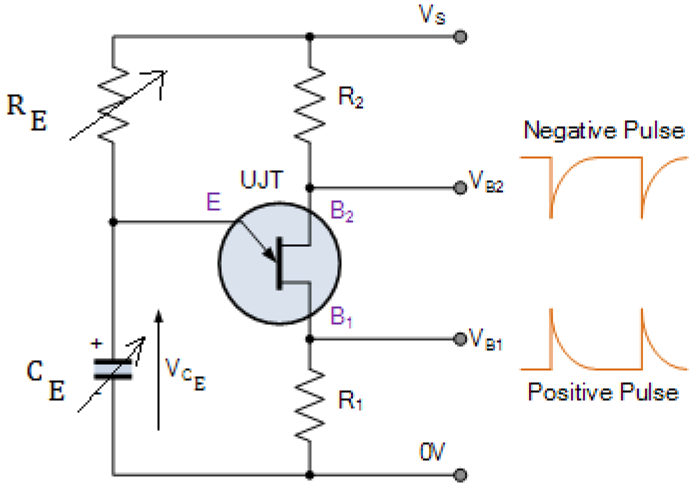
Fig.: V-I Characteristics of UJT

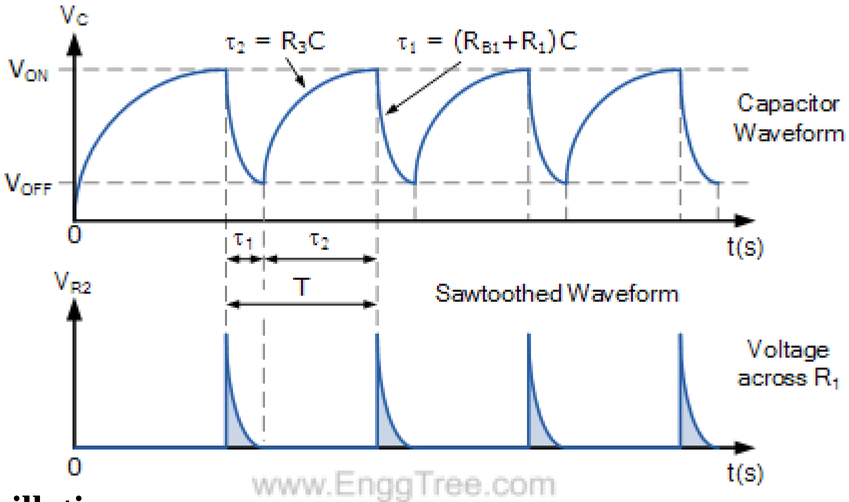
(B) **Operation of UJT as a relaxation oscillator and its derivation- frequency of oscillation.** ***(Nov 2016)***

UJT as a relaxation oscillator consists of UJT and a capacitor C_E which is charged through R_E as the supply voltage V_{BB} is switched ON. The voltage across the capacitor increases exponentially and when the capacitor voltage reaches the peak point voltage V_p, the UJT starts conducting and the capacitor voltage is discharged rapidly through EB_1 and R_1.After the peak point voltage of UJT is reached, it provides negative resistance to the discharge path which is useful in working of the relaxation oscillator. As the capacitor voltage reaches zero the device then cuts off and capacitor C_E starts to charge again. This cycle is repeated continuously generating a saw tooth waveform across C_E.

The inclusion of external resistors R_2 and R_1 in series with B_2 and B1 provides spike waveform. When the UJT fires, the sudden surge of current through B_1 causes drop across R1,which provides positive spikes. At the time of firing fall of V_{EB1} causes I_2 to increases rapidly which generates negative going spikes across R_2.

By changing the value of R_E and C_E the frequency of oscillation changes.





Frequency of oscillation:

Voltage across the capacitance prior to breakdown is given by

$V_c = V_{BB}(1 - e^{-t/R_E C_E})$

$R_E C_E$- Charging time constant

Discharge of capacitor occurs when V_C is equal to the peak point voltage V_p,

$V_p = \eta V_{BB} = V_{BB}(1 - e^{-t/R_E C_E})$

Where $\eta = (1 - e^{-t/R_E C_E})$

$e^{-t/R_E C_E} = 1 - \eta$

Taking Log on both side

$$\frac{t}{R_E C_E} = \log_e \frac{1}{(1-\eta)}$$

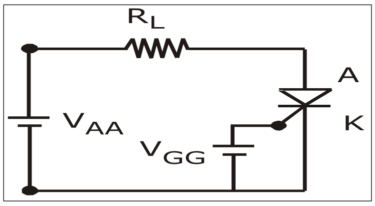
$$t = R_E C_E \ln \frac{1}{(1-\eta)}$$

$$f = 1/t = \frac{1}{R_E C_E \ln \frac{1}{(1-\eta)}}$$

THYRISTOR (SCR)

8. DRAW AND EXPLAIN THE V-I CHARACTERISTICS OF THYRISTOR (SCR) (or) DISCUSS THE DIFFERENT MODES OF OPERATION OF THYRISTOR WITH THE HELP OF ITS STATIC V-I CHARACTERISTICS. (Nov/Dec 2017) (Apr/May 2018) (OR)

Outline the structure of SCR and explain its operation. Also, illustrate its V-I characteristics. (Apr/May 2019-R17)



Circuit diagram

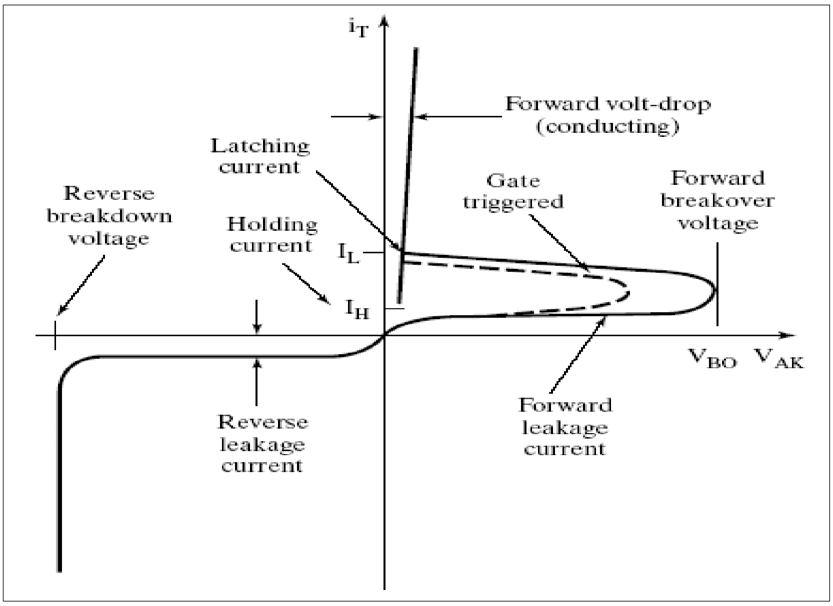


Fig: V-I Characteristics of SCR

A typical V-I characteristics of a thyristor is shown above. In the reverse direction the thyristor appears similar to a reverse biased diode which conducts very little current until avalanche breakdown occurs. In the forward direction the thyristor has two stable states or modes of operation that are connected together by an unstable mode that appears as a negative resistance on the V-I characteristics. The low current high voltage region is the forward blocking state or the off state and the low voltage high current mode is the on state. For the forward blocking state the quantity of interest is the forward blocking voltage V_{BO} which is defined for zero gate current. If a positive gate current is applied to a thyristor then the transition or break over to the on state will occur at smaller values of anode to cathode voltage as shown. Although not indicated the gate current does not have to be a dc current but instead can be a pulse of current having some minimum time duration. This ability to switch the thyristor by means of a current pulse is the reason for wide spread applications of the device.

However once the thyristor is in the on state the gate cannot be used to turn the device off. The only way to turn off the thyristor is for the external circuit to force the current through the device to be less than the holding current for a minimum specified time period.

HOLDING CURRENT I_H

After an SCR has been switched to the on state a certain minimum value of anode current is required to maintain the thyristor in this low impedance state. If the anode current is reduced below the critical holding current value, the thyristor cannot maintain the current through it and reverts to its off state usually I_μ is associated with turn off the device.

LATCHING CURRENT I_L

After the SCR has switched on, there is a minimum current required to sustain conduction. This current is called the latching current. I_L associated with turn on and is usually greater than holding current.

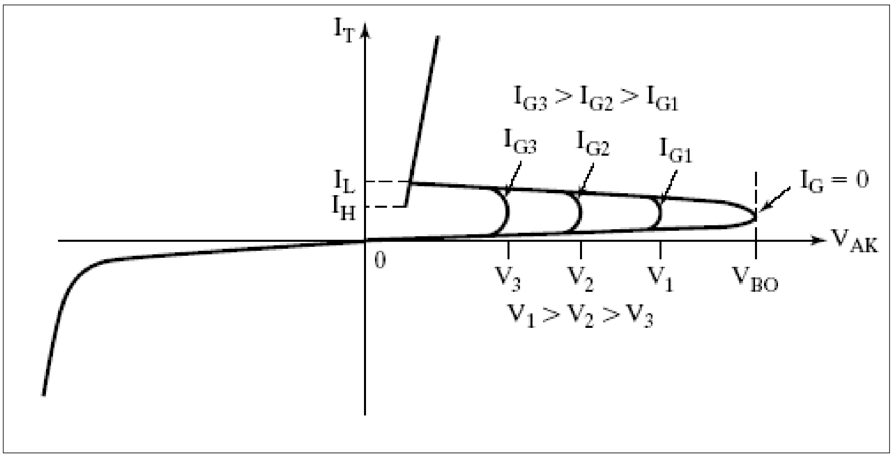


Fig.: Effects on gate current on forward blocking voltage

9. Sketch the four layer construction of an SCR and the two transistor equivalent circuit explains the device operation. (Non / Dec 2016)(May 2017)

A thyristor is the most important type of power semiconductor devices. They are extensively used in power electronic circuits. They are operated as bi-stable switches from non-conducting to conducting state.

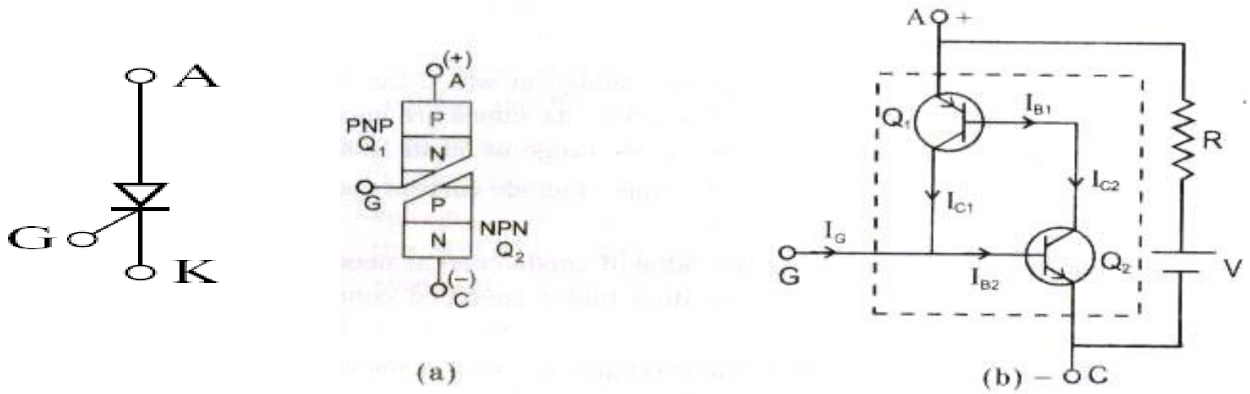
A thyristor is a four layer, semiconductor of p-n-p-n structure with three p-n junctions. It has three terminals, the anode, cathode and the gate.

The word thyristor is coined from thyratron and transistor. It was invented in the year 1957 at Bell Labs. The Different types of Thyristors are

- Silicon Controlled Rectifier (SCR).
- TRIAC
- DIAC
- Gate Turn Off Thyristor (GTO)

SILICON CONTROLLED RECTIFIER (SCR)

The SCR is a four layer three terminal device with junctions J_1, J_2, J_3 as shown. The construction of SCR shows that the gate terminal is kept nearer the cathode. The approximate thickness of each layer and doping densities are as indicated in the figure. In terms of their lateral dimensions Thyristors are the largest semiconductor devices made. A complete silicon wafer as large as ten centimeter in diameter may be used to make a single high power thyristor.



Two transistor model of SCR

OPERATION

When the anode is made positive with respect the cathode junctions J_1& J_3 are forward biased and junction J_2 is reverse biased. With anode to cathode voltage V_{AK} being small, only leakage current flows through the device. The SCR is then said to be in the forward blocking state. If V_{AK} is further increased to a large value, the reverse biased junction J_2 will breakdown due to avalanche effect resulting in a large current through the device. The voltage at which this phenomenon occurs is called the forward breakdown voltage V_{BO}. Since the other junctions J_1& J_3 are already forward biased, there will be free movement of carriers across all three junctions resulting in a large forward anode current. Once the SCR is switched on, the voltage drop across it is very small, typically 1 to 1.5V. The anode current is limited only by the external impedance present in the circuit.

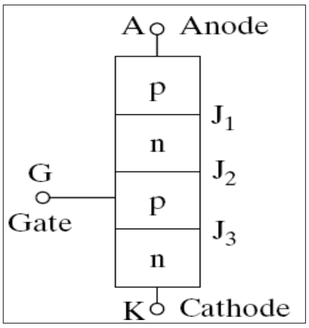
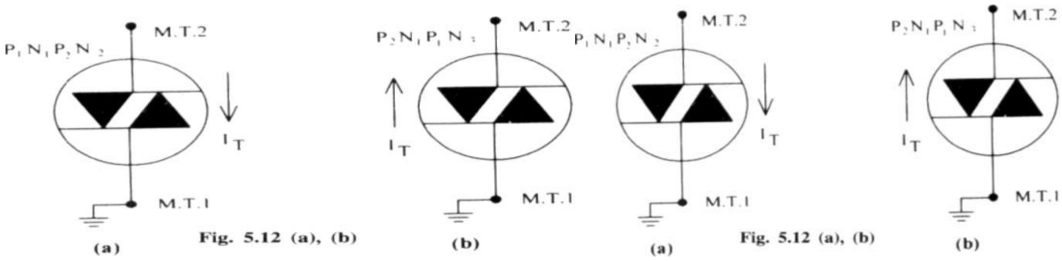


Fig.: Simplified model of a thyristor

Although an SCR can be turned on by increasing the forward voltage beyond V_{BO}, in practice, the forward voltage is maintained well below V_{BO} and the SCR is turned on by applying a positive voltage between gate and cathode. With the application of positive gate voltage, the leakage current through the junction J_2 is increased. This is because the resulting gate current consists mainly of electron flow from cathode to gate. Since the bottom end layer is heavily doped as compared to the p-layer, due to the applied voltage, some of these electrons reach junction J_2 and add to the minority carrier concentration in the p-layer. This raises the reverse leakage current and results in breakdown of junction J_2 even though the applied forward voltage is less than the breakdown voltage V_{BO}. With increase in gate current breakdown occurs earlier.

DIAC

10. Explain in detail about DIAC and its characteristics?



- The DIAC can be turned ON only when the applied voltage across it is main terminal reaches the break - over voltage.
- The M.T.2 is positive with respect to M.T.1, the DIAC passes current through the DIAC $P_1N_1P_2N_2$from M.T.2 to
- M.T.1 as shown in Fig. 5.12 (a). The DIAC turn 'ON' the applied voltage makes M.T.2 negative with respect to the M.T.1, the DIAC current through the diode
- When the current drops below the holding value. It is used as a triggering device.

Characteristics of a DIAC

The DIAC is operated with M.T.2 positive with respect to M.T.1, the V I characteristics obtained is as shown in Fig. 5.13 by the curve marked *OAB.* Similarly the DIAC is operated with its M.T.2 negative with respect to M.T.I, the V-l characteristics obtained as shown in Fig. 5.13 by the curve marked *OCD.*

Applications

The DIAC is used as a triggering device; it is not a control device. It is used in,

- Temperature control
- Triggering of TRIAC
- Light diming circuits
- Motor speed control

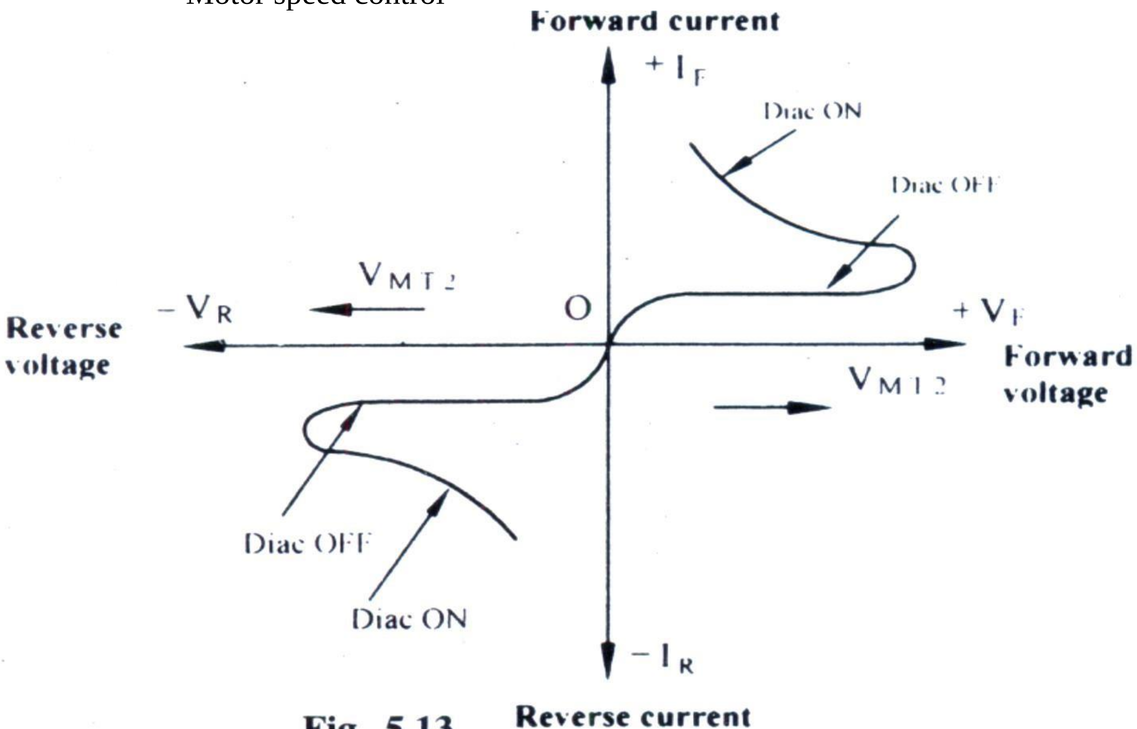


Fig. 5.13

TRIAC

11. EXPLAIN THE CONSTRUCTION, OPERATION & STATIC CHARACTERISTICS OF TRIAC

A triac is a three terminal bi-directional switching thyristor device. It can conduct in both directions when it is triggered into the conduction state. The triac is equivalent to two SCRs connected in anti-parallel with a common gate. Figure below shows the triac structure. It consists of three terminals viz., MT_2, MT_1 and gate G.

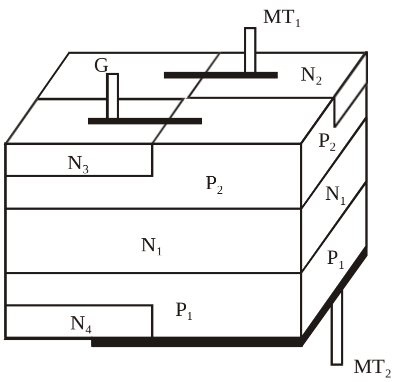


Fig. TRIAC Structure

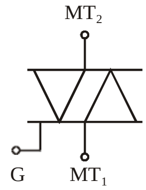


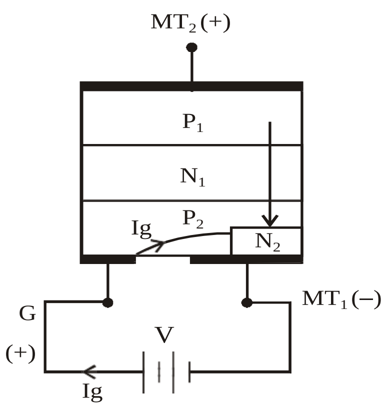
Fig. TRIAC Symbol

The gate terminal G is near the MT_1 terminal. Figure above shows the triac symbol. MT_1 is the reference terminal to obtain the characteristics of the triac. A triac can be operated in four different modes depending upon the polarity of the voltage on the terminal MT_2 with respect to MT_1 and based on the gate current polarity.

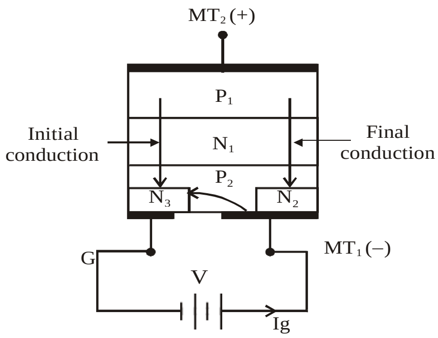
The characteristics of a triac are similar to that of an SCR, both in blocking and conducting states. A SCR can conduct in only one direction whereas triac can conduct in both directions.

MODE 1: MT_2 *positive, Positive gate current* ***(I^+ mode of operation)***

When MT_2 and gate current are positive with respect to MT_1, the gate current flows through P_2-N_2 junction as shown in figure below. The junction P_1-N_1 and P_2-N_2 are forward biased but junction N_1-P_2 is reverse biased. When sufficient number of charge carriers is injected in P_2 layer by the gate current the junction N_1-P_2 breakdown and triac starts conducting through $P_1N_1P_2N_2$ layers. Once triac starts conducting the current increases and it's V-I characteristics is similar to that of thyristor. Triac in this mode operates in the first-quadrant.



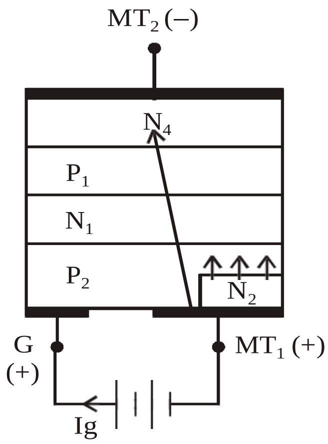
MODE 2: ***MT_2 positive, Negative gate current*** *(I^- mode of operation)*



When MT_2 is positive and gate G is negative with respect to MT_1 the gate current flows through P_2-N_3 junction as shown in figure above. The junction P_1-N_1 and P_2-N_3 are forward biased but junction N_1-P_2 is reverse biased. Hence, the triac initially starts conducting through $P_1N_1P_2N_3$ layers. As a result the potential of layer between P_2-N_3 rises towards the potential of MT_2. Thus, a potential gradient exists across the layer P_2 with left hand region at a higher potential than the right hand region. This results in a current flow in P_2 layer from left to right, forward biasing the P_2N_2 junction. Now the right hand portion P_1-N_1 - P_2-N_2 starts conducting. The device operates in first quadrant. When compared to Mode 1, triac with MT_2 positive and negative gate current is less sensitive and therefore requires higher gate current for triggering.

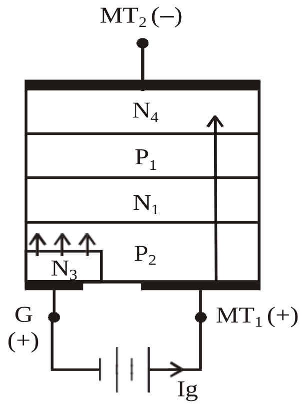
MODE 3: ***MT_2 negative, Positive gate current*** ***(III^+ mode of operation)***

When MT_2 is negative and gate is positive with respect to MT_1 junction P_2N_2 is forward biased and junction P_1-N_1 is reverse biased. N_2 layer injects electrons into P_2 layer as shown by arrows in figure below. This causes an increase in current flow through junction P_2-N_1. Resulting in breakdown of reverse biased junction N_1-P_1. Now the device conducts through layers $P_2N_1P_1N_4$ and the current starts increasing, which is limited by an external load.



The device operates in third quadrant in this mode. Triac in this mode is less sensitive and requires higher gate current for triggering.

MODE 4: *MT_2 negative, Negative gate current* *(III^- mode of operation)*



In this mode both MT_2 and gate G are negative with respect to MT_1, the gate current flows through P_2N_3 junction as shown in figure above. Layer N_3 injects electrons as shown by arrows into P_2 layer. These results in increase in current flow across P_1N_1 and the device will turn ON due to increased current in layer N_1. The current flows through layers $P_2N_1P_1N_4$. Triac is more sensitive in this mode compared to turn ON with positive gate current. (Mode 3).

Triac sensitivity is greatest in the first quadrant when turned ON with positive gate current and also in third quadrant when turned ON with negative gate current. When MT_2 is positive with respect to MT_1 it is recommended to turn on the triac by a positive gate current. When MT_2 is negative with respect to MT_1 it is recommended to turn on the triac by negative gate current. Therefore Mode 1 and Mode 4 are the preferred modes of operation of a triac (I^+ mode and III^- mode of operation are normally used).

TRIAC CHARACTERISTICS

Figure below shows the circuit to obtain the characteristics of a triac. To obtain the characteristics in the third quadrant the supply to gate and between MT_2 and MT_1 are reversed.

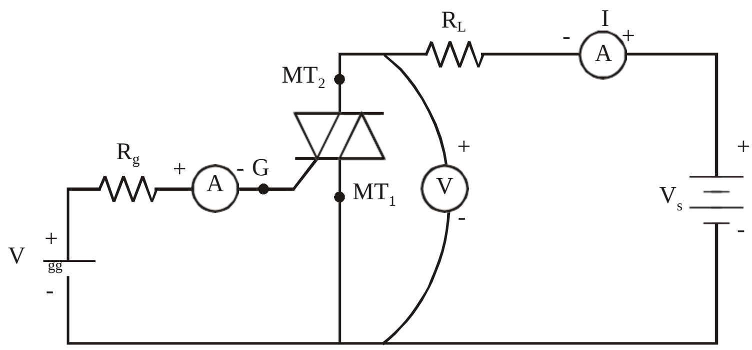


Figure below shows the V-I Characteristics of a triac. Triac is a bidirectional switching device. Hence its characteristics are identical in the first and third quadrant. When gate current is increased the break over voltage decreases.

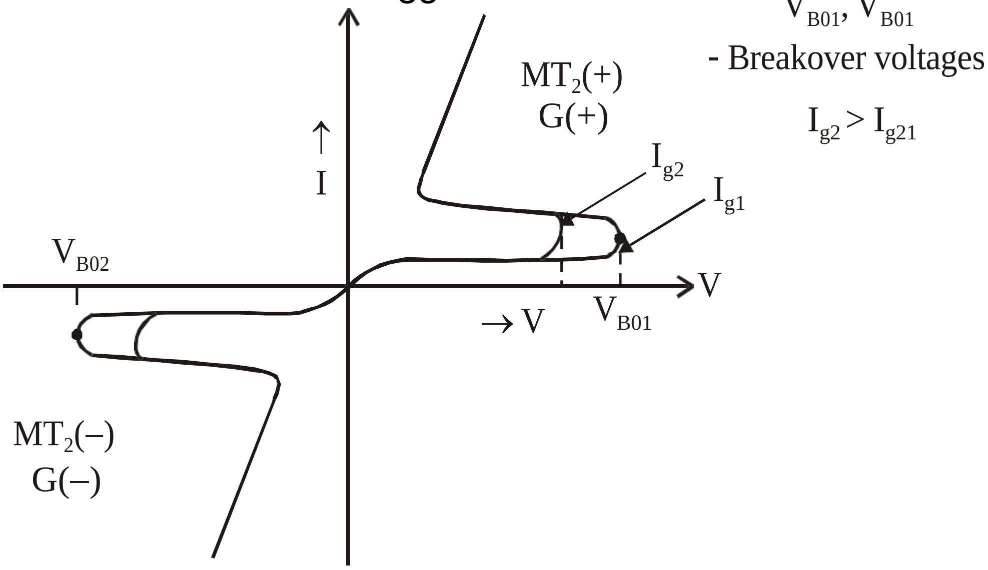


Fig.: Triac Characteristic

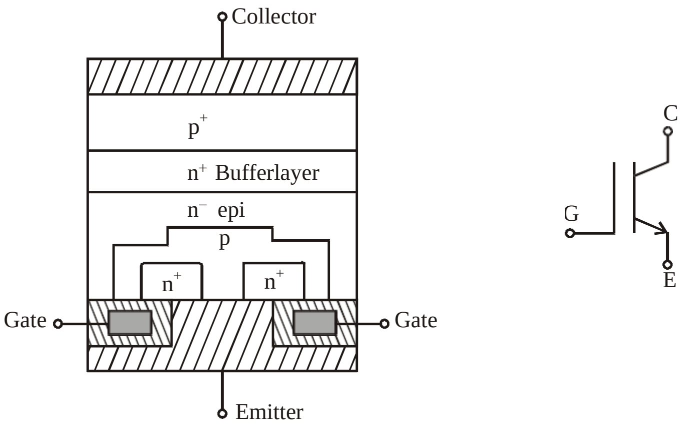
Triac is widely used to control the speed of single-phase induction motors. It is also used in domestic lamp dimmers and heat control circuits, and full wave AC voltage controllers.

<u>IGBT-Structure, Operation & Characteristics</u>

12. **EXPLAIN THE CONSTRUCTION, OPERATION & STATIC CHARACTERISTICS OF INSULATED GATE BIPOLAR TRANSISTOR (IGBT).** ***(NOV/DEC-2012) (May/June2016) (May 2017) (Nov/Dec 2018 R-13)***

IGBT is a voltage-controlled device. It has high input impedance like a MOSFET and low on-state conduction losses like a BJT.

Figure below shows the basic silicon cross-section of an IGBT. Its construction is same as power MOSFET except that n^+ layer at the drain in a power MOSFET is replaced by P^+ substrate called collector.



Structure **Symbol**

Fig.: Insulated Gate Bipolar Transistor

IGBT has three terminals gate (G), collector (C) and emitter (E). With collector and gate voltage positive with respect to emitter the device is in forward blocking mode. When gate to emitter voltage becomes greater than the threshold voltage of IGBT, a n-channel is formed in the P-region. Now device is in forward conducting state. In this state p^+ substrate injects holes into the epitaxial n^- layer. Increase in collector to emitter voltage will result in increase of injected hole concentration and finally a forward current is established.

CHARACTERISTIC OF IGBT

Figure below shows circuit diagram to obtain the characteristic of an IGBT. An output characteristic is a plot of collector current I_C versus collector to emitter voltage V_{CE} for given values of gate to emitter voltage V_{GE}.

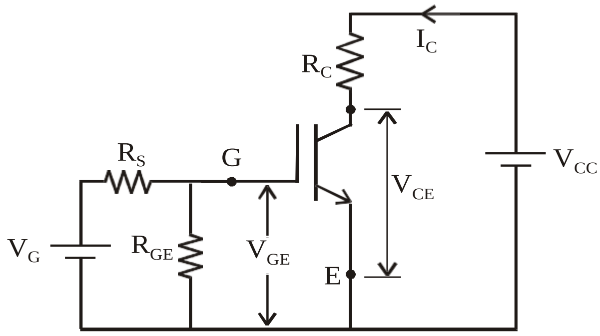


Fig.: Circuit Diagram to Obtain Characteristics

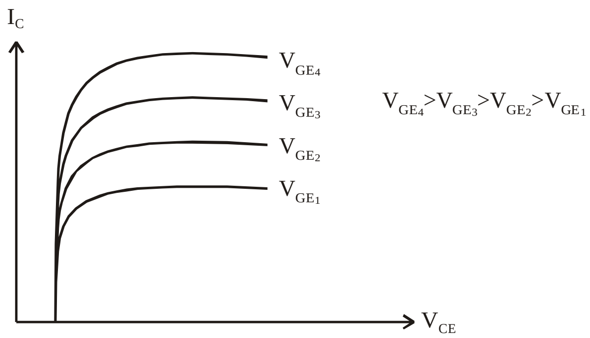


Fig. Output Characteristics

A plot of collector current I_C versus gate-emitter voltage V_{GE} for a given value of V_{CE} gives the transfer characteristic. Figure below shows the transfer characteristic.

Note

Controlling parameter is the gate-emitter voltage V_{GE} in IGBT. If V_{GE} is less than the threshold voltage V_T then IGBT is in OFF state. If V_{GE} is greater than the threshold voltage V_T then the IGBT is in ON state.

IGBTs are used in medium power applications such as ac and dc motor drives, power supplies and solid state relays.

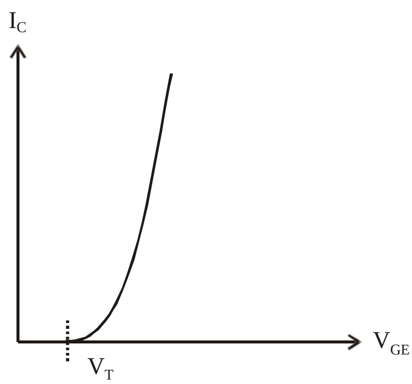
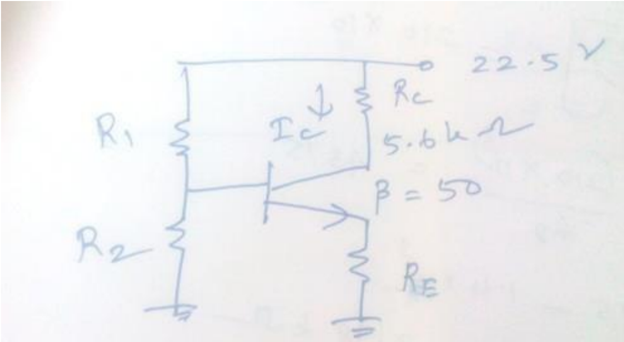


Fig. Transfer Characteristic

Solved Problems:

1. **Design a voltage divider bias circuit for transistor to establish the quiescent point V_{CE}=12v, Ic = 1.5mA, Stability factor S $\le$ 3,** $\mathrm{Q} = \mathbf{50}$, $\boldsymbol{V_{BE} = 0.7V}$, $\boldsymbol{V_{CC} = 22.5\ V\ and\ Rc = 5.6\ K}\Omega$.

(May 2017) (Nov/Dec 2017)



$\beta = 50,\quad V_{BE} = 0.7\,V,\qquad V_{CC} = 22.5\,V,\qquad R_C = 5.6\,k\Omega,\qquad V_{CE} = 12\,V,\qquad I_C = 1.5\,mA,\qquad S \le 3$

$Emitter\ Resistance\ (R_E)$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$12 = 22.5 - (1.5 \times 10^{-3})\,(5.6 \times 10^3 + R_E) = 14.1 - 1.5 \times 10^{-3} R_E$$

$$R_E = 1.4 \times 10^3\Omega = 1.4k\ \Omega$$

$Resistances\ R_1\ and\ R_2$

Stability factor (s)

$$3 = \frac{\beta + 1}{1 + \beta\left(\frac{R_E}{R_{th} + R_E}\right)} = \frac{50 + 1}{1 + 50 \times \frac{1.4 \times 10^3}{R_{th} + 1.4 \times 10^3}} = \frac{51}{1 + \frac{70 \times 10^3}{R_{th} + 1.4 \times 10^3}}$$

$$3\left[\frac{(R_{th} + 1.4 \times 10^3) + 70 \times 10^3}{R_{th} + 1.4 \times 10^3}\right] = 51$$

$$3[(R_{th} + 1.4 \times 10^3)] + (70 \times 10^3) = 51\,(R_{th} + 1.4 \times 10^3)$$

$$48[R_{th} + (1.4 \times 10^3)] = 210 \times 10^3$$

$$R_{th} + 1.4 \times 10^3 = \frac{(210 \times 10^3)}{48} = 4375$$

$$R_{th} = 4375 - 1.4 \times 10^3;\ R_{th} = 2975\ \Omega;\ R_{th} = 2.98\ k\Omega$$

For good voltage divider the value of resistor

$$R_2 = 0.1\beta.R_E = 0.1 \times 50 \times (1.4 \times 10^3) = 7 \times 10^3\Omega = 7k\Omega$$

Thevenin's Resistance (R_{th})

$$2.98 = R_1 \| R_2 = \frac{R_1.R_2}{R_1 + R_2} = \frac{7R_1}{R_1 + 7}$$

$2.98(R_1 + 7) = 7R_1;\qquad\qquad 4.02R_1 = 20.86$

$$R_1 = \frac{20.86}{4.02} = 5.2\ k\Omega$$

2. For an n channel silicon FET with a = 3*10^{-4} cm and N_D = 10^{15} electronics/cm^3 find (a) the pinch off voltage and (b) the channel half width for V_{GS} = ½ VP and I_D = 0. (May / Jun 2016)

Solution:

The relative dielectric constant of silicon is given in table 5-1 as 12, and hence $\epsilon = 12\epsilon_0$. Using the value of e *and* ϵ_0 from appendixes A and B, we have from Eq expressed in mks units,

$$V_P = \frac{1.60 \times 10^{-19} \times 10^{21} \times (3 \times 10^{-6})^2}{2 \times 12 \times (36\pi \times 10^9)^{-1}} = 6.8V$$

b. Solution Eq for b, we obtain for V_{GS} = ½ V_P

$$b = a\left[1 - \left(\frac{V_{GS}}{V_P}\right)^{1/2}\right] = (3 \times 1^{-4})\left[1 - \left(\frac{1}{2}\right)^{\frac{1}{2}}\right] = 0.87 \times 10^{-4}\,cm$$

Hence the channel width has been reduced to about one third its value for V_{GS} = 0

3. Determine the base current for the CB transistor circuit if I_C =80 mA and Q = 170. (Nov/Dev 2016)

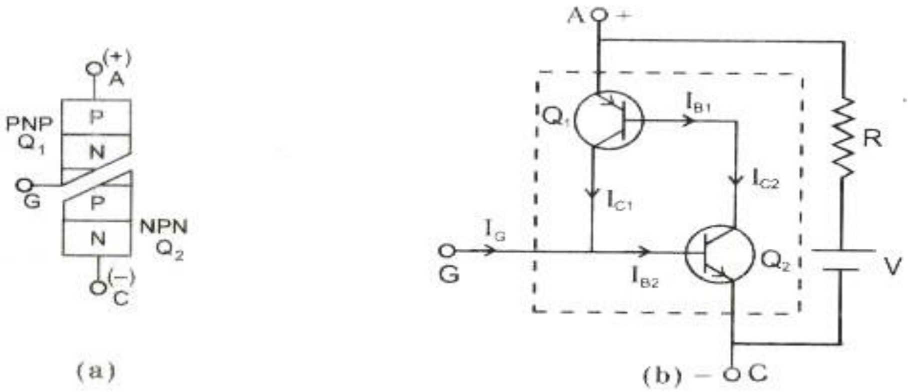
Given

I_C =80 mA

β = 170.

$$\beta = \frac{I_c}{I_B} = \frac{80 \times 10^{-3}}{I_B} = 170 \therefore I_B = \frac{I_c}{\beta} = \frac{80 \times 10^{-3}}{170} = 0.4706 \text{ mA}$$

4. Draw the two-transistor equivalent circuit of SCR? (May 2017)



5. A transistor has a typical Q = 100. If the collector current is 40 mA. What is the value of emitter current? *(May 2017)*

Given: I_C =40 mA β = 100 $\beta = \frac{I_c}{I_B}$

$$\therefore I_B = \frac{I_c}{\beta} = \frac{40 \times 10^{-3}}{100} = 0.0004 \text{ A}$$

$I_E = I_B + I_C$ $I_E = 0.0004 + 40 \times 10^{-3} = 0.0404$ A

6. If the collector current is 2mA and the base current is 25μA, what is the emitter current?

Solution: $I_C = 2mA$, $I_B = 25\mu A$,

$I_E = I_B + I_C = 2mA + 25\mu A$ $\therefore$ **$I_E = 2.025mA$**

7. Calculate I_C and I_E for a transistor that has $\alpha = 0.99$ and $I_B = 150\mu A$. Determine the value of Q_{dc} for the transistor? (Nov / Dec 2015)

Solution:

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.99}{1-099} = 99$$

$$\beta = \frac{I_C}{I_B};\ I_C = \beta \times I_B = 99 \times 150\ \mu A = 14\ mA$$

$$\alpha = \frac{I_C}{I_E};\ I_E = \frac{Ic}{\alpha} = \frac{14}{0.99} = 14.14mA$$

8. A germanium transistor is to be operated at zero signal I_C = 1mA. If the collector supply voltage V_{CC} = 12V, what is the value of R_B in the base resistor method? Assume β = 100. If another transistor of same batch with β = 50 is used, what will be new value of zero signal I_C for same R_B? Comment on the results. ***(Nov/Dec 2018-R17)(13 Marks)***

Solution:

$$V_{CC} = 12\ V, \quad \beta = 100$$

$$V_{BE} = 0.3\ V \quad \because \text{Germanium transistor}$$

$$\text{Zero signal } I_C = 1\ mA$$

$$\therefore \quad \text{Zero signal } I_B = \frac{I_C}{\beta} = \frac{1\ mA}{100} = \mathbf{0.01\ mA}$$

Using the relation, $V_{CC} = I_B R_B + V_{BE}$ we have

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{12-0.3}{0.01\ mA} = \mathbf{1170\ k\Omega}$$

ii) $\beta = 50$

Using the relation, $V_{CC} = I_B R_B + V_{BE}$ we have

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12-0.3}{1170\ k\Omega} = \mathbf{0.01\ mA}$$

$$\therefore \text{Zero signal } I_C = \beta I_B = 50 \times 0.01\ mA = \mathbf{0.5\ mA}$$

Comment: It is clear from the above example that with the change in transistor parameter β, the zero-signal collector current has changed from 1mA to 0.5 mA. Therefore, the base resistor method cannot provide stabilization.

9. The intrinsic stand-off ratio for a UJT is 0.6. If the inter base resistance is 10KΩ, what are the value of R_{B1} and R_{B2}? ***(Nov/Dec 2018-R17) (4 Marks)***

Sol. : $\eta = 0.6,\ R_{BB} = 10\ k\Omega$

$$\eta = \left.\frac{R_{B1}}{R_{BB}}\right|_{I_E=0} \quad \text{i.e.} \quad 0.6 = \frac{R_{B1}}{10}$$

$$\therefore \quad R_{B1} = \mathbf{6\ k\,\Omega}$$

$$R_{BB} = R_{B1} + R_{B2} \quad \text{i.e} \quad 10 = 6 + R_{B2}$$

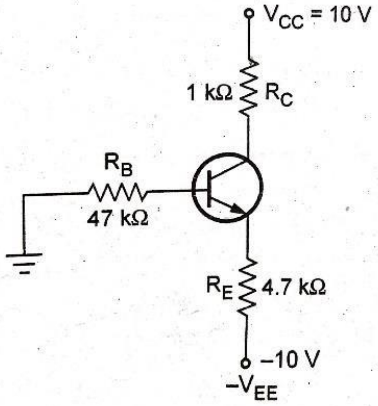
$$\therefore \quad R_{B2} = \mathbf{4\ k\,\Omega}$$

10. **When V_{GS} of a JFET changes from -3.1 V to -3 V, the drain current changed from 1 mA to 1.3 mA. Find the value of transconductance.** ***(Nov/Dec 2018-R17) (2 Marks)***

Solution:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{(1.3-1)\times 10^{-3}}{(3.1-3)} = 3\ mA/V$$

11. **Find the Q point of the transistor shown below. Also draw the DC load line. Give β = 100 and V_{BE} = 0.7V.** ***(Nov/Dec 2018-R17) (15 Marks)***



Sol. :

$$I_B = \frac{V_{EE}-V_{BE}}{R_B+(1+\beta)R_E} = \frac{10-0.7}{47K+(1+100)4.7K} = \mathbf{17.83\ \mu A}$$

$$I_C = \beta I_B = 100\times 17.83\mu A = \mathbf{1.783\ mA}$$

$$I_E = I_C + I_B = 1.783\ mA + 17.83\ \mu A = \mathbf{1.8\ mA}$$

$$V_C = V_{CC} - I_C R_C = 10-(1.783\times 10^{-3}\times 1\times 10^3)$$

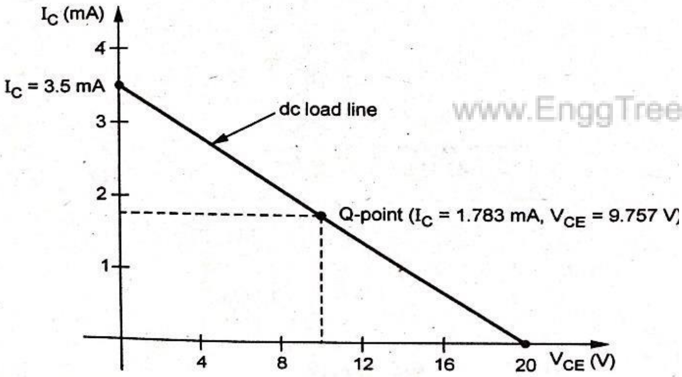
$$= \mathbf{8.217\ V}$$

$$V_E = -V_{EE} + I_E R_E = -10\,V + (1.8\times 10^{-3}\times 4.7\times 10^3)$$

$$= \mathbf{-1.54\ V}$$

$\therefore$ $V_{CE} = V_C - V_E = 8.217 - (-1.54) = \mathbf{9.757\ V}$

$\therefore$ The Q point of the circuit is $\mathbf{V_{CE} = 9.757\ V}$ and $\mathbf{I_C = 1.783\ mA}$

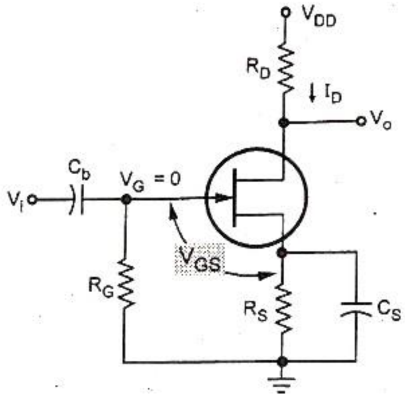


when $V_{CE} = 0$, $I_C = \dfrac{V_{CC}-(-V_{EE})}{R_C+R_E}$

$$= \frac{10+10}{1K+4.7K} = \mathbf{3.5\ mA}$$

when $I_C = 0$, $V_{CE} = V_{CC} - (-V_{EE}) = 10 + 10 = 20\ V$

12. **In a self-bias n-channel JFET, the operating point is to be set at I_D = 1.5mA and V_{DS} =10V. The parameters are I_{DSS} = 5mA and V_{GS} (off) = -2V. Find the values of R_S and R_D if V_{DD} = 20V.** ***(Nov/Dec 2018-R17) (9 Marks)***



Given : I_D = 1.5 mA, I_{DSS} = 5 mA,

$V_{GS(OFF)}$ = –2 V = V_p, V_{DD} = 20 V and V_{DS} = 10 V

Step 1 : Calculate V_{GS}

We have $I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_p}\right]^2$

$$\therefore \quad V_{GS} = V_p\left[1-\sqrt{\frac{I_D}{I_{DSS}}}\right] = -2\left[1-\sqrt{\frac{1.5}{5}}\right] = -0.9 \text{ V}$$

Step 2 : Calculate R_s

$$V_{GS} = V_G - V_S = 0 - V_S = -0.9 \text{ V}$$

$$\therefore \quad V_S = 0.9 \text{ V}$$

$$\therefore \quad R_S = \frac{V_S}{I_D} = \frac{0.9\text{V}}{1.5 \text{ mA}} = 600\ \Omega$$

EC8353-ELECTRONIC DEVICES AND CIRCUITS

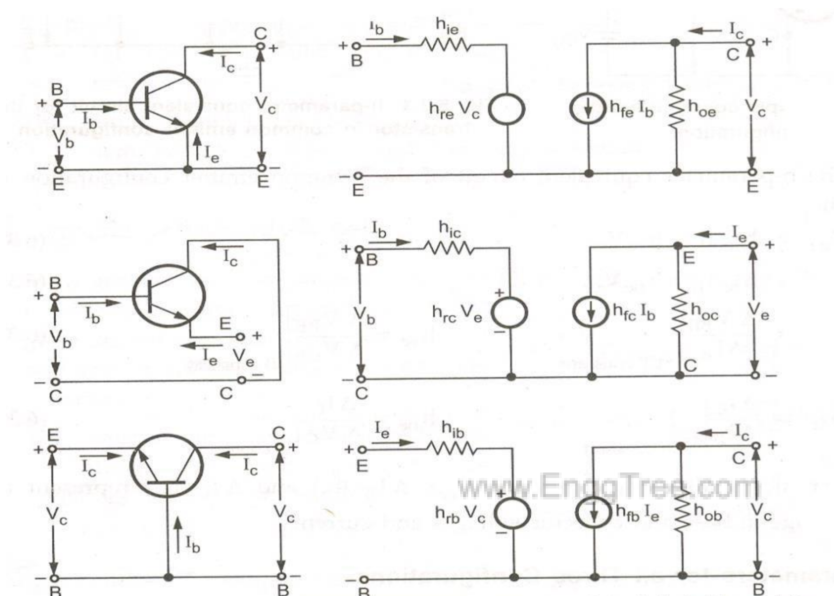
UNIT-III AMPLIFIERS

PART-A

BJT Small Signal Model

1. **Which is the BJT configuration is suitable for impedance matching application and why?**
CC configuration is suitable for impedance matching application because of very high input impedance and low output impedance.

2. **Draw the hybrid small signal model of BJT device. (MAY/JUNE2016)**



Transistor configurations and their hybrid models

CE

$V_b = h_{ie} I_b + h_{re} V_c$
$I_c = h_{fe} I_b + h_{oe} V_c$

CC

$V_b = h_{ic} I_b + h_{rc} V_e$
$I_e = h_{fc} I_b + h_{oc} V_e$

CB

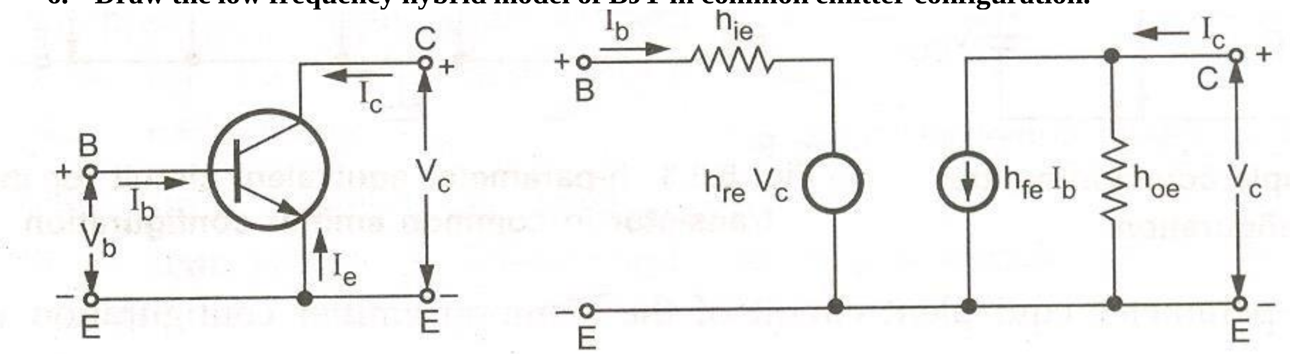
$V_e = h_{ib} I_e + h_{rb} V_c$
$I_c = h_{fb} I_e + h_{ob} V_c$

3. **What are the tools used for small signal analysis of BJT?**
   - h – Parameter circuit model.
   - z – Parameter circuit model.
   - y – Parameter circuit model.
   - Trans-conductance parameter circuit model.
   - Physical model
   - T-model

4. **What are the steps used for small signal analysis of BJT?**
   - Draw the actual circuit diagram
   - Replace coupling capacitors and emitter bypass capacitor by short circuit.
   - Replace dc source by a short circuit. In other words, short V_{CC} and ground lines.

5. **State the phase relationship between input / output currents and phase relationship between the input / output voltages of various transistors configurations. (Nov/Dec 2018)**
For all the transistor configurations, input and output currents are in phase.
The input and output voltages of both CB and CC configuration are in phase. But in common-emitter amplifier the input and output voltages are 180^0 out of phase.

6. **Draw the low frequency hybrid model of BJT in common emitter configuration.**

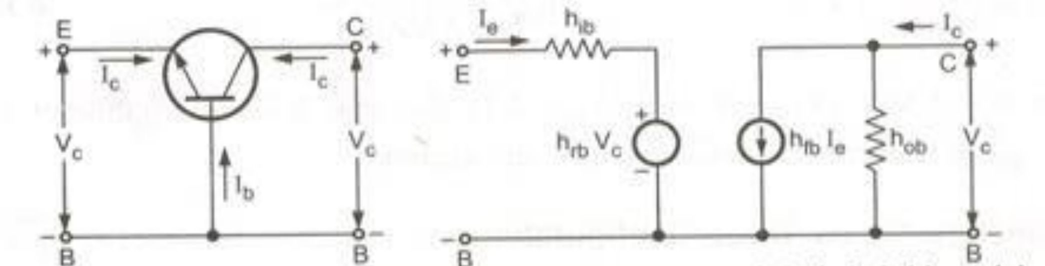


$V_b = h_{ie}I_b + h_{re}V_c$

$I_c = h_{fe}I_b + h_{oe}V_c$

CE, CB, CC Amplifiers-Gain and frequency response

7. **Draw the hybrid small signal model of CB configuration? (Apr/May 2018)**



Transistor configurations and their hybrid models

8. **Why emitter is always forward biased and collector is always reverse biased with respect to base?**
   To supply majority charge carrier to base and to remove the charge carriers away from the collector-base junction.

9. **Why CE configuration is most popular in amplifier circuits?**
   Because it's current, voltage and power gain are quite high and the ratio of output impedance and input impedance are quite moderate.

10. **Give the voltage gain for CE configuration including source resistance.**

$$A_{vs} = A_i \times R_L / R_S + R_i$$
$$= (- h_{fe} / 1 + h_{oe} R_L) \times R_L / (R_S + R_i)$$

11. **Define the h_{ie} and h_{fe} for a common emitter transistor configuration.**
   From the h – parameter equivalent circuit of the common emitter configuration.
   $H_{ie} = \Delta V_{BE} / \Delta I_B \mid V_{CE}$ constant
   $H_{fe} = \Delta I_C / \Delta I_B \mid V_{CE}$ constant

12. **Give the current gain expression for a common emitter transistor configuration.**
   Current gain for common emitter configuration:
   $A_i = - I_C / I_b = - h_{fe} / 1 + h_{oe} R_L$

MOSFET small signal model

13. What is trans-conductance? Give its expression for MOSFET. (Nov/Dec 2017)

The trans-conductance is a ratio of output current to input voltage and hence it represents the gain of the MOSFET.

Tran conductance expression for MOSFET

$g_m = 2 \sqrt{(KI_{DQ})}$

$I_{DQ} = K (V_{GSQ} – V_T)^2$

14. State the values of C_{gd} and C_{gs} in various operating regions of MOSFET.

Values of gate capacitances in Triode Region:

$C_{gs} = C_{gd} = (WL\ C_{ox})\ ½$

Values of gate capacitances in Saturation Region:

$C_{gs} = (WL\ C_{ox})\ 2/3$

$C_{gd}=0$

Values of gate capacitances in Cut - off Region:

$C_{gs} = C_{gd}=0$

$C_{gd} = WL\ C_{ox}$

C_{ox} – Gate Capacitance.

15. List various gate capacitances in MOSFET.

There are three gate capacitances in MOSFET:

$C_{gs –}$ gate source capacitance,

$C_{gd –}$ gate drain Capacitance, and

$C_{gb -}$ gate body Capacitance.

CS and Source follower

16. Explain the effect of source resistor on CS MOSFET amplifier.

The source resistor is introduced to stabilize the Q – point against variations in the MOSFET parameters. In BJT circuits, a source resistor reduces the small gain.

17. What is source follower? (Apr/May 2018)

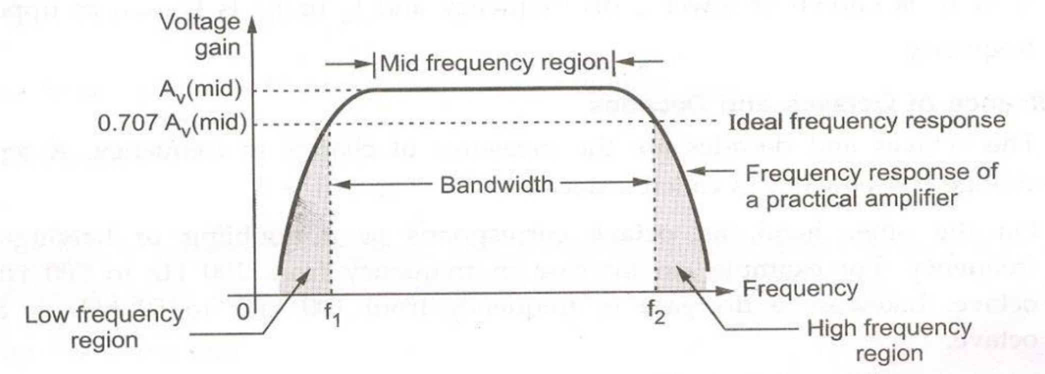
A common-drain amplifier, also known as a source follower, is one of three basic single-stage field effect transistor (FET) amplifier topologies, typically used as a voltage buffer.

Gain and frequency response

18. What is the significance of octaves and decades in frequency response?

- Octaves and Decades are the measure of change in frequency.
- Ten times change in frequency is called a Decade. On the other hand, an Octave corresponds to a doubling of the frequency.
- For example, an increase in frequency from 100Hz to 200Hz is an octave. Likewise, a decrease in frequency from 100Hz to 50Hz is also an octave.
- If the frequency is reduced to one hundredth of fc (from fc to 0.01fc), the drop in the voltage gain is – 40 dB. In each decade the voltage gain drops by – 20 db.

19. Draw *general frequency response* curve (or) *half-power frequencies* of an amplifier.



Frequency response of an RC coupled amplifier

- In the above diagram the frequency f_2 lies in high frequency region, while the frequency f_1 lies in low frequency region.
- These two frequencies are also referred to as half power half – power frequencies since gain or output voltage drops to 70.7% of maximum value and this represents a power level of one half the power at the reference frequency in mid – frequency region.

Additional Questions

20. What is the relation between α and β of the transistor?

$$\alpha = \frac{\beta}{\beta+1}$$

21. Why must the base be narrow for the transistor action?

β is the ratio of IC to IB. IB becomes less if the base width is narrow. Higher value of β can be obtained with lower value of base current.

22. What are emitter efficiency and base transport factor of a transistor?

The ratio of current of injected carriers at emitter junction to the total emitter current is called the emitter injection efficiency. Transport Factor, β= IC / IB

23. What is the relation between the current of a transistor?

$I_E = I_B + I_C$

24. How many h-parameters are there for a transistor?

- h_r–reverse voltage gain
- h_o–output admittance.
- h_i,-input impedance
- h_f-forward current gain

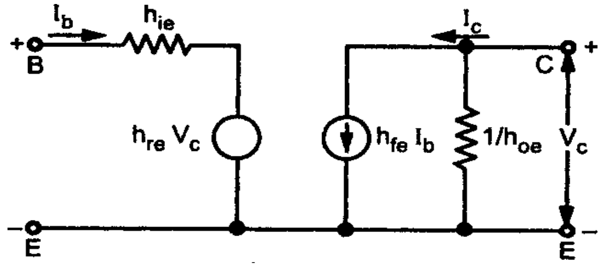
25. Why h-parameters are called hybrid parameters?

Because they have different units are mixed with other parameters.

26. What are the advantages of the h-parameters? (Apr/May 2011)

(1) Real numbers up to radio frequencies
(2) Easy to measure
(3) Determined from transistor static characteristics curve
(4) Convenient to use in the circuit analysis and design
(5) Easily convertible from one configuration to other

27. Draw the hybrid model for a transistor. (Nov/Dec 2012)



28. What are h-parameters? Define the four h-parameters.

One of a set of four transistor equivalent circuit parameters that conveniently specify transistor performance for small voltage and current in a particular circuit also known as hybrid parameter.

Input resistance with output short – circuited, in Ω.

$h_{11} = V_i / I_i \,|\, V_o = 0$

Fraction of output voltage at input with input open circuited. This parameter is ratio of similar quantities, hence unitless.

$h_{12} = V_i / V_o \,|\, I_i = 0$

Forward current transfer ratio or current gain with output short circuited.

$h_{21} = I_o / I_i \,|\, V_o = 0$

This parameter is a ratio of similar quantities, hence unitless. Output admittance with input open – circuited, in mhos.

$h_{22} = I_o / V_o \,|\, I_i = 0$

29. State Miller's theorem. (Nov/Dec 2016)

Miller's theorem states that, if Z is the impedance connected between two nodes node 1 and node 2, it can be replaced by two separate impedance Z_1 and Z_2; where Z_1 is connected between node - 1 and ground, and node Z_2 is connected between node -2 and ground.

The Vi and Vo are the voltages at the node – 1 and node – 2 respectively, The values of Z_1 an d Z_2 can be derived from the ratio of Vo and Vi, denoted as K. Thus it is not necessary to know the values of Vi and Vo to calculate the values of Z_1 and Z_2

The values of impedance Z_1 and Z_2

$Z_1 = Z / (1 - K)$; $Z_2 = Z \times K / (K - 1)$

30. What do you mean by faithful amplification?

During the process of raising the strength of the input signal if the shape of the output voltage is exactly same as that of the input signal, the amplification is called faithful amplification.

31. Define the various h-parameters for a common emitter transistor.

From the h – parameter equivalent circuit of the common emitter configuration.

$V_{be} = h_{ie} I_b + h_{re} V_{ce}$

$I_c = h_{fe} I_b + h_{oe} V_{ce}$

Where, $h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B} \,|\, V_{CE}$ constant

$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}} \,|\, I_B$ constant

$h_{fe} = \frac{\Delta I_C}{\Delta I_B} \,|\, V_{CE}$ constant

$h_{oe} = \frac{\Delta I_C}{\Delta V_C} \,|\, I_B$ constant

32. State the advantages of using h-parameters for analyzing transistor amplifiers.

i.) Real numbers at audio frequencies
ii.) Easy to measure
iii.) Can be obtained from the transistor static characteristics curves,
iv.) Convenient to use in circuit analysis and design,
v.) Most of the transistor manufacturers specify the h – parameters.

33. What is bandwidth of an amplifier.

The bandwidth of an amplifier is defined as the difference between the lower cut - off frequency and upper cut off frequency.

$BW = f_2 - f_1$

34. State the effect of coupling and bypass capacitors on the frequency response of amplifier.

Reactance of a capacitor is given by $X_c = 1 / 2\pi fc$. At medium and high frequencies, the factor f makes X_c very small, so that all coupling capacitors behave as short circuits. At low frequencies, X_c increases. This increase in X_c drops the signal voltage across the capacitor and reduces the circuit gain. As signal frequencies decrease, the capacitor reactance's increase and circuit gain continues to fall, reducing the output voltage.

35. State the effect of internal transistor capacitance on the frequency response of amplifier.

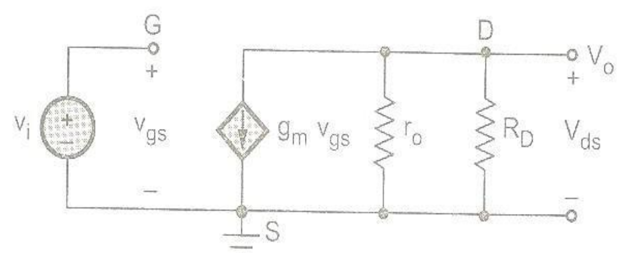
At high frequencies, the reactance of the junction capacitance are low. As frequency increases, the reactance of junction capacitances fall. When these reactance become small enough, they provide shunting effect as they are in parallel with junctions. This reduces the circuit gain and hence the output voltage.

36. Give the expression for $r_o$of NMOS transistor.

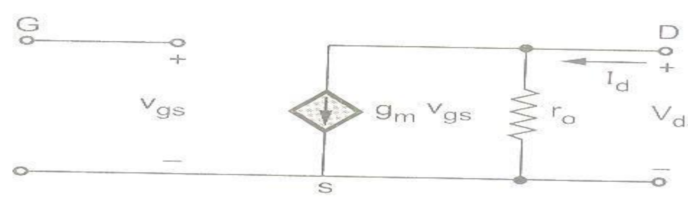
$r_o = (\partial i_D / \partial \mathbf{v}_{DS})^{-1} \big|_{v_{GS} = V_{GSQ} = \text{const.}}$

$r_o = [\lambda K [(v_{GSQ} - V_T)^2]^{-1} \approx [\lambda I_{DQ}]^{-1}$

37. Draw the small signal equivalent circuit of CS JFET (Nov/Dec2015).



Small signal equivalent circuit of common-source circuit with NMOS transistor model

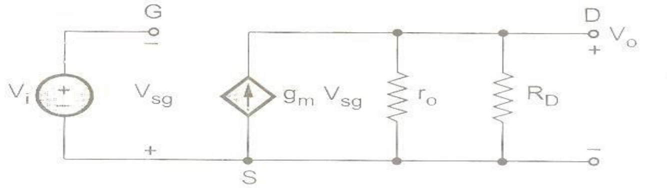


Expanded small signal equivalent circuit, including output resistance, for NMOS transistor

38. What is Gate capacitance in MOSFET.

Gate capacitance is a parallel – plate capacitance formed by a gate electrode with the channel, with the oxide layer acts as a capacitor dielectric. It is denoted as C_{ox}.

39. Draw the small signal equivalent circuit of PMOS transistor.



Small signal equivalent circuit of common source amplifier with PMOS transistor model

40. Explain the loading effect.

The small signal overall voltage gain is,

$$G_v = v_o / v_s = - g_m(r_o \| R_D)(R_i / R_i + R_{si}) = A_v (R_i / R_i + R_{si})$$

Since Rsi is not zero, the amplifier input signal v_i is less than the signal voltage, This is known as **loading effect**. It reduces the voltage gain of the amplifier.

41. What do you mean by drain diffusion and source diffusion capacitance?

Drain and Source capacitances are due to the reverse – biased pn junctions formed by the n^+ source region and the p – type substrate, and the n^+ drain region and the p- type substrate. These are denoted as **source diffusion capacitance** and **drain diffusion capacitance** respectively.

42. Give the expression of unity gain frequency (f_T)for MOSFET amplifier?

Unity gain frequency for MOSFET:

$f_T = g_m / 2\pi (C_{gs} + C_{gd})$

From the above expression we can say that f_T is proportional to gm and inversely proportional to the internal capacitances.

43. Compare different amplifiers.

COMMON SOURCE AMPLIFIER	Good voltage amplifier and better trans conductance amplifier	• Large Voltage gain • High input resistance • High output resistance
COMMON DRAIN AMPLIFIER	Good voltage buffer	• Voltage gain ≈ 1 • High input resistance • Low input resistance
COMMON GATE AMPLIFIERS	Good current buffer	• Current Gain ≈ 1 • Low input resistance • High output resistance

44. What is the need of coupling capacitors in amplifier design? (Aril/May 2019) (Nov / Dec 2015)

Coupling capacitors isolates the DC condition of one stage from the following stages.
It is used to couple output of one stage to another stage.

45. Differentiate between power transistor and signal transistor. (May / Jun 2016)

S.No	Power transistor	Small signal transistor
1	n^{-1} drift layer is present	110 n^{-1} drift layer
2	Secondary breakdown occurs	No secondary breakdown
3	Used in power circuits	Used in amplifying circuits

PART-B

BJT Small signal Model-Analysis of CE, CB, CC amplifiers

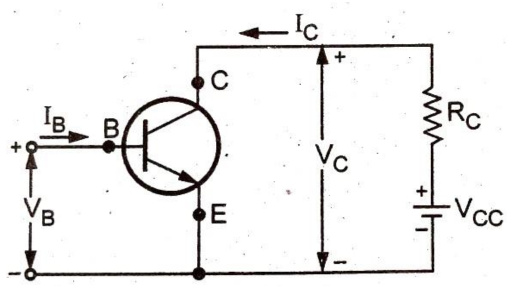
1. **Draw the small signal model of BJT device (OR) Draw the parameters equivalent circuit or small signal model of a transistor in CE, CB, CC configuration? (Apr/May 2018). (OR)**
Draw the hybrid model of BJT in CE, CC and CB configuration.

h – Parameter model for CE, CC and CB configuration

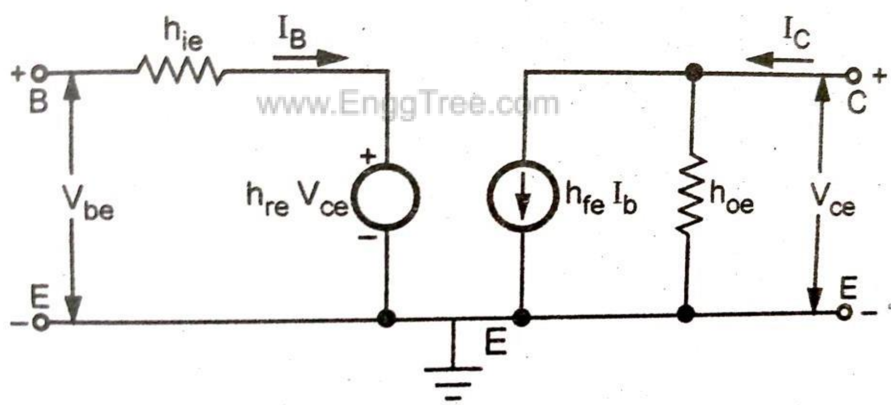
The variable I_b, I_c, V_b, and V_c represent total instantaneous current and voltage.

I_b – Input current; I_c – Output current; V_{be} – Input voltage; V_{ce} – Output voltage

CE Configuration



h– Parameter equivalent circuit



$V_{be} = h_{ie}I_b + h_{re}V_{ce}$ --- (1)

$I_c = h_{fe}I_b + h_{oe}V_{ce}$ --- (2)

Where, $h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B} \Big| V_{CE}$ – constant------(3)

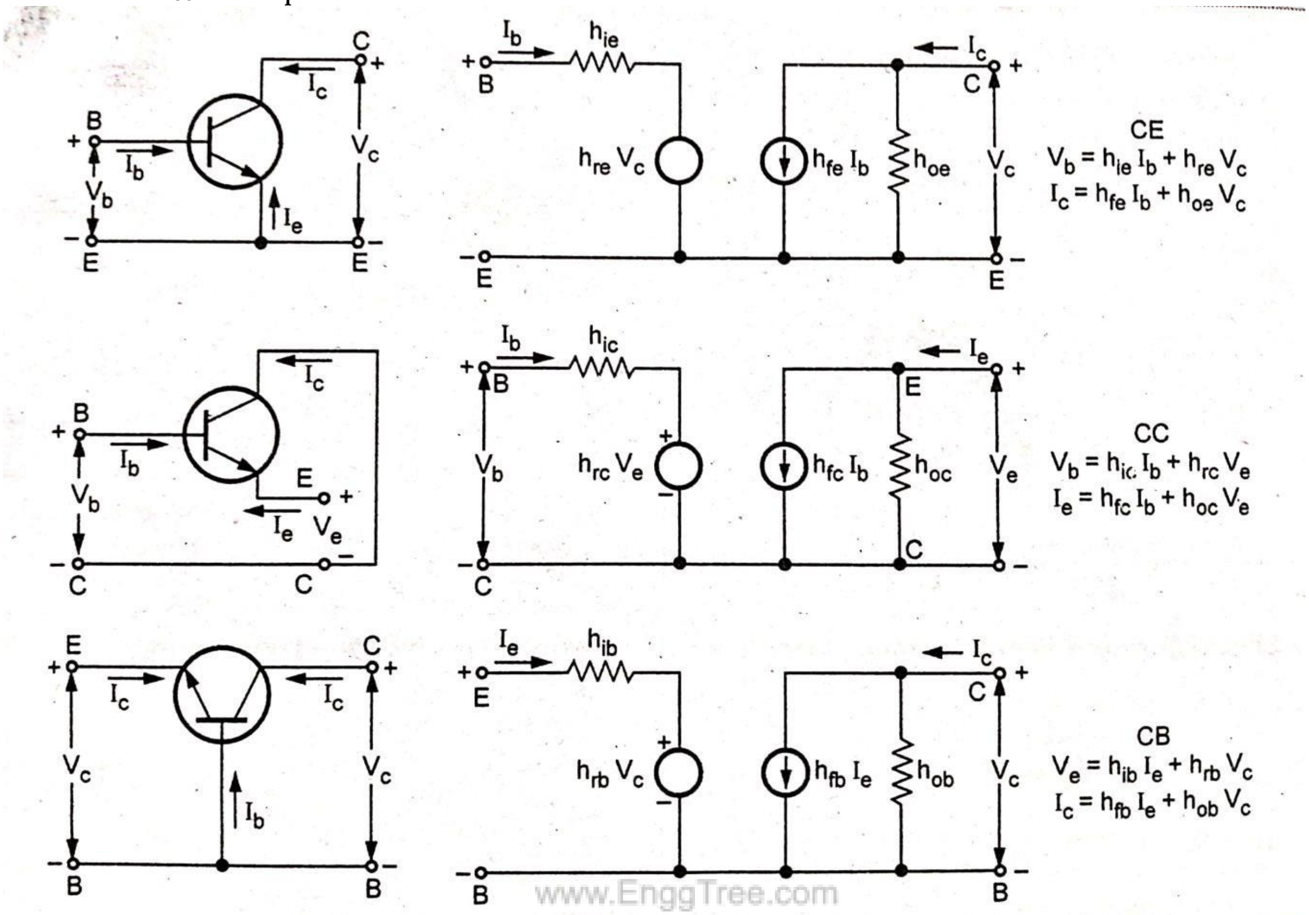
$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}} \Big| I_B$ – constant---- (4)

$h_{fe} = \frac{\Delta I_c}{\Delta I_B} \Big| V_{CE}$ – constant ----(5)

$h_{oe} = \frac{\Delta I_c}{\Delta V_C} \Big| I_B$ – constant -----(6)

h_{ie} – Input resistance;

h_{re} – Reverse voltage gain;
h_{fe} – Forward transfer gain;
h_{oe} – Output admittance

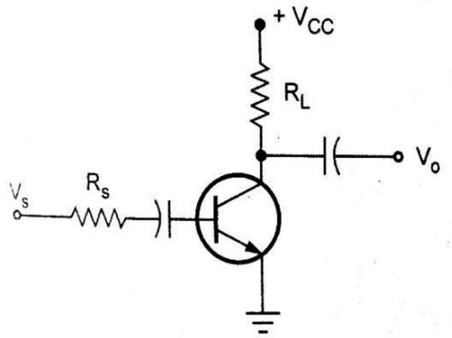


Relationship between h-parameters of different transistor configuration:

CE to CB conversion formulae	CE to CC conversion formulae
$h_{ib} = \frac{h_{ie}}{1 + h_{fe}}$	$h_{ic} = h_{ie}$ *
$h_{rb} = \frac{h_{ie} h_{oe}}{1 + h_{fe}} - h_{re}$	$h_{rc} = 1 - h_{re} \approx 1$ *
$h_{fb} = -\frac{h_{fe}}{1 + h_{fe}}$	$h_{fc} = -(1 + h_{fe})$ *
$h_{ob} = \frac{h_{oe}}{1 + h_{fe}}$	$h_{oc} = h_{oe}$ *

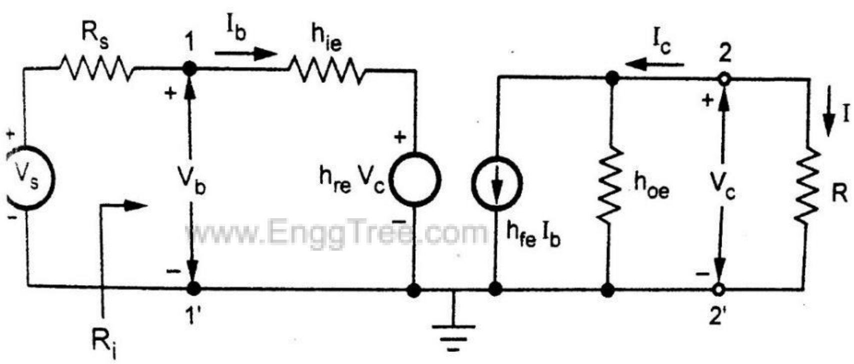
2. **(A) Derive the expressions for current gain (A_I), voltage gain(A_V), input resistance (R_i) and output resistance (R_O) for CE amplifier using h – parameter model.** ***(April/May 2015 & 18) (Nov / Dec' 2014& 16)***
Illustrate the steps involved in analyzing a BJT amplifier circuit using small signal model. (April/May 2019) (5 Marks)

Circuit diagram



(a) CE amplifier

h – Parameter model



(b) CE amplifier in its h-parameter model

Current gain $[A_I]$ $A_I = \frac{I_L}{I_b}$

$I_C = h_{fe}I_b + h_{oe}V_c;\; I_C = h_{fe}I_b + h_{oe}(-I_cR_L);$ $\{since, V_c = -I_cR_L\}$

$I_C + h_{oe}R_LI_c = h_{fe}I_b; I_C(1 + h_{oe}R_L) = h_{fe}I_b$

$$\frac{I_C}{I_b} = \frac{h_{fe}}{1 + h_{oe}R_L}$$

$$A_I = \frac{-I_C}{I_b} = -\frac{h_{fe}}{1 + h_{oe}R_L}$$

Input Resistance $(R_i) R_i = \frac{V_b}{I_b}$

$V_b = h_{ie}I_b + h_{re}V_C$

$V_C = -I_CR_L; V_C = A_II_bR_L$

Now $R_i = \frac{V_b}{I_b} = \frac{h_{ie}I_b + (A_I I_b R_L)}{I_b} = h_{ie} + h_{re} A_I R_L$

Substituting, $A_I = \frac{-h_{Fe}}{1+h_{oe}R_L}$ to the above equation

$$R_i = h_{ie} + h_{re}\left(\frac{-h_{fe}}{1 + h_{oe}R_L}\right) \times R_L$$

$$R_i = h_{ie} - \frac{h_{re}h_{fe}R_L}{1 + h_{oe}R_L}$$

Voltage gain ($\mathbf{A_V}$) $A_V = \frac{V_c}{V_b} = \frac{A_I I_b R_L}{V_b} \therefore \frac{I_b}{V_b} = \frac{1}{R_i}$

$$A_V = \frac{A_I R_L}{R_i}$$

Output admittance ($\mathbf{Y_o}$) $Y_o = \frac{I_c}{V_c}$ with $V_s = 0$

$I_c = h_{fe}I_b + h_{oe}V_c$ (divide this equation by V_C)

$$\frac{I_c}{V_c} = \frac{h_{fe}I_b + h_{oe}V_c}{V_c}$$

$$Y_o = \frac{h_{fe}I_b}{V_c} + h_{oe}$$

From h parameter circuit with $\mathbf{V_s = 0}$

$R_sI_b + h_{ie}I_b + h_{re}V_c = 0$ *(Apply KVL)*

$(R_s + h_{ie})I_b = -h_{re}V_c$

$$\frac{I_b}{V_c} = \frac{-h_{re}}{R_s + h_{ie}}$$

Substitute, $\frac{Ib}{V_c} = \frac{-h_{re}}{R_s+h_{ie}}$ *in* $Y_o = \frac{h_{Fe}I_b}{V_c} + h_{oe}$

$$Y_o = \frac{I_c}{V_c} = h_{fe}\left(\frac{-h_{re}}{R_s + h_{ie}}\right) + h_{oe}$$

$Y_o = h_{oe} - \frac{h_{Fe}h_{re}}{R_s+h_{ie}}$ and $R_o = \frac{1}{Y_o}$

(B) Draw the circuit of CE amplifier with DC sources eliminated and deduce the small signal model for amplifier operation. (April/May 2019) (8 Marks) (OR) **Approximate analysis of CE amplifier using simplified Hybrid Model.**

Analysis of CE Amplifier using simplified Hybrid Model:

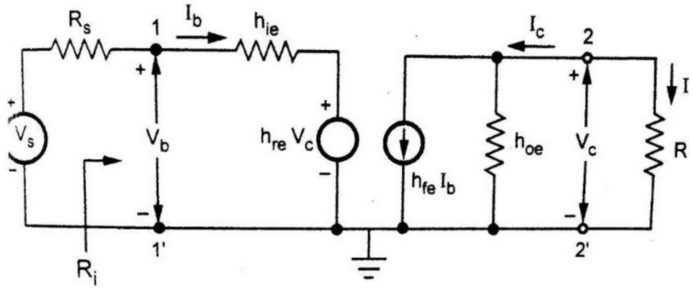


Fig. Simplified CE model

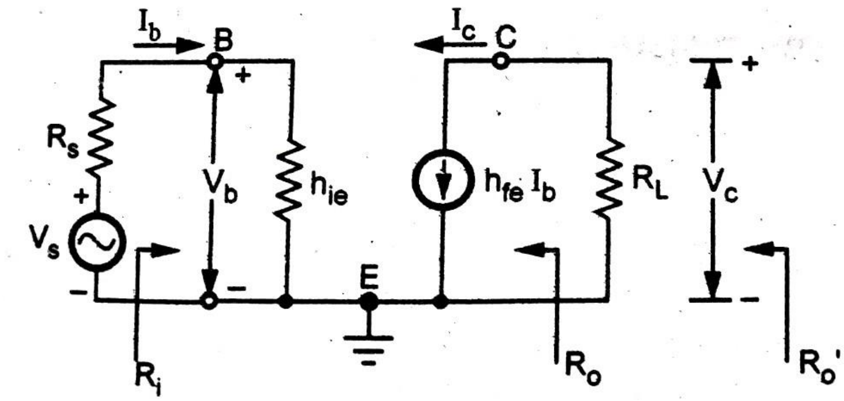


Fig. Approximate CE model

Current gain $[A_I]$ $A_I = \frac{I_L}{I_b}$

$$A_I = \frac{-I_C}{I_b} = -h_{fe}$$

Input Resistance (R_i) $R_i = \frac{V_b}{I_b}$

$$R_i = h_{ie}$$

Voltage gain (A_V) $A_V = \frac{V_c}{V_b} = \frac{A_I I_b R_L}{V_b} \therefore \frac{I_b}{V_b} = \frac{1}{R_i}$

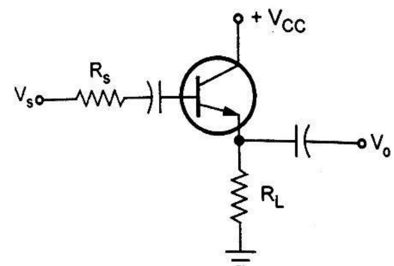
$$A_V = \frac{A_I R_L}{R_i}$$

Output admittance (Y_o) $Y_o = 0$

$$R_o = 1/Y = \infty$$

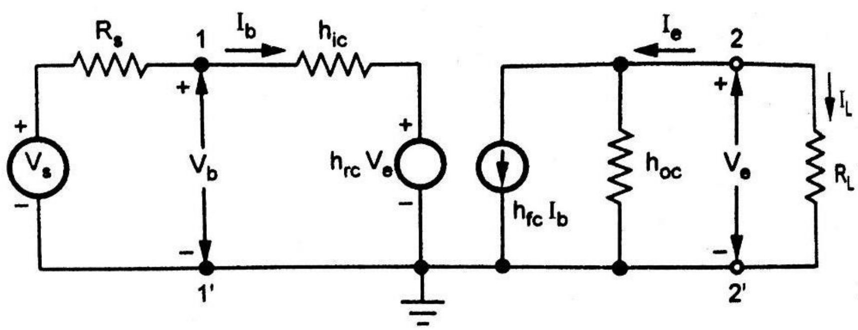
3. (A) Derive the expressions for current gain, voltage gain, input impedance and output impedance for an Emitter Follower (common collector) circuit.

Circuit diagram



(a) CC amplifier

h parameter equivalent circuit



(b) CC amplifier in its h-parameter model

Current gain (A_I) $A_I = \frac{I_L}{I_b} = \frac{-I_e}{I_b}$

Apply KCL

$I_e = h_{fc}I_b + h_{oc}V_e \quad = h_{fc}I_b + h_{oc}(-I_eR_L) \qquad (since, V_e = -I_eR_L)$

$I_e + I_eR_Lh_{oc} = h_{fc}I_b; I_e(1 + h_{oc}R_L) = h_{fc}I_b; \frac{I_e}{I_b} = \frac{h_{fc}}{1 + h_{oc}R_L}$

$$A_i = \frac{I_e}{I_b} = \frac{-I_L}{I_b} = \frac{-h_{fc}}{1 + h_{oc}R_L}$$

Input Resistance $(\mathbf{R_i})R_i = \frac{V_b}{I_b}$

Apply KVL

$V_b = h_{ic}I_b + h_{rc}V_e(V_e = -I_eR_L)$

$V_e = A_II_bR_L \qquad \{A_I = \frac{-I_e}{I_b}\}$

Now

$R_i = \frac{h_{ic}I_b + h_{re}(A_II_bR_L)}{I_b}; \qquad R_i = h_{ic} + h_{re}A_IR_L$

$R_i = h_{ic} - h_{rc}\left(\frac{h_{Fc}R_L}{1+h_{oc}R_L}\right) \qquad \{A_I = \frac{-h_{Fc}}{1+h_{oc}R_L}\}$

Voltage gain (A_V) $A_V = \frac{V_e}{V_b}$ $\{\because V_e = -I_e R_L;\ I_e = A_I I_b;\quad V_b = I_b\ R_i\}$

$$A_V = \frac{A_I I_b R_L}{V_b} \Rightarrow \frac{A_I I_b R_L}{I_b R_i} \qquad \{\because \frac{I_b}{V_b} = \frac{1}{R_i}\}$$

$$A_V = \frac{A_I R_L}{R_i}$$

Output admittance (Y_0) $Y_0 = \frac{I_2}{V_2}$ with $V_s = 0$

$$Y_O = \frac{I_e}{V_e} \text{ with } V_s = 0$$

$$I_e = h_{fc}\, I_b + h_{oc}\, V_e$$

Dividing the above equation by V_e , $\frac{I_e}{V_e} = \frac{h_{fc} I_b}{V_e} + h_{oc} \quad ---(1)$

From circuit $V_s = 0$

Apply KVL

$$R_S I_b + h_{ic}\, I_b + h_{rc}\, V_e = 0$$

$$(R_S + h_{ic}) I_b = -h_{rc}\, V_e$$

$$\frac{I_b}{V_e} = \frac{-h_{rc}}{R_s + h_{ic}} \quad ---(2)$$

Sub equation (2) in (1)

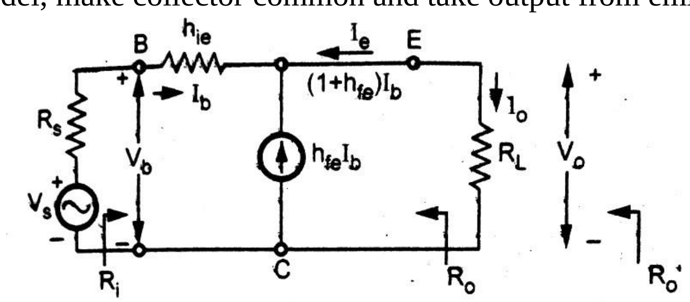
$$\frac{I_e}{V_e} = h_{fc}\left(\frac{-h_{rc}}{R_s + h_{ic}}\right) + h_{oc}$$

$$y_o = \frac{I_e}{V_e} = h_{oc} - \frac{h_{fc}\, h_{rc}}{R_s + h_{ic}} \quad \textit{and } R_o = \frac{1}{y_o}$$

(B) Draw the circuit of CC amplifier with DC sources eliminated and deduce the small signal model for amplifier operation. (April/May 2019) (8 Marks) (OR) **Approximate analysis of CC amplifier using simplified Hybrid Model.**

In simplified CE model, the input is applied to base and output is taken from collector, and emitter is common between input and output. The same simplified model can be modified to get simplified CC model.

For simplified CC model, make collector common and take output from emitter.



The $h_{fb}I_b$ current direction is now exactly opposite that of CE model because the current $h_{fc}I_b$ always points towards emitter.

Current gain (A_I) $A_I = \frac{I_L}{I_b} = \frac{-I_e}{I_b}$

$$A_i = 1 + h_{fe}$$

Input Resistance $(\mathbf{R_i})$ $R_i = \frac{V_b}{I_b}$

Apply KVL

$V_b = h_{ie}I_b + I_O R_L$; (divide both sides by I_b)

$\{A_I = \frac{-I_e}{I_b} = \frac{-I_O}{I_b}\}$

Now

$R_i = \frac{V_b}{I_b} = h_{ie} + (1 + I_O h_{fe})R_L$;

Voltage gain (A_V) $A_V = \frac{V_e}{V_b}$

$A_V = \frac{A_I I_b R_L}{V_b} \Rightarrow \frac{A_I I_b R_L}{I_b R_i}$ $\{\because \frac{I_b}{V_b} = \frac{1}{R_i}\}$

$A_V = \frac{A_I R_L}{R_i}$

Substituting values of A_I and R_i *we get*, $A_V = \frac{A_I I_b R_L}{V_b} \Rightarrow \frac{A_I I_b R_L}{I_b R_i}$

Output admittance $(\mathbf{Y_0})$ $Y_0 = \frac{I_2}{V_2}$ with $V_s = 0$

$Y_O = \frac{I_e}{V_e}$ with $V_s = 0$

$I_e = h_{fc} I_b + h_{oc} V_e$

Dividing the above equation by V_e, $\frac{I_e}{V_e} = \frac{h_{fc}I_b}{V_e} + h_{oc}$ $---(1)$

From circuit $V_s = 0$

Apply KVL

$R_S I_b + h_{ic} I_b + h_{rc} V_e = 0$

$(R_S + h_{ic})I_b = -h_{rc} V_e$

$\frac{I_b}{V_e} = \frac{-h_{rc}}{R_s + h_{ic}} --- (2)$

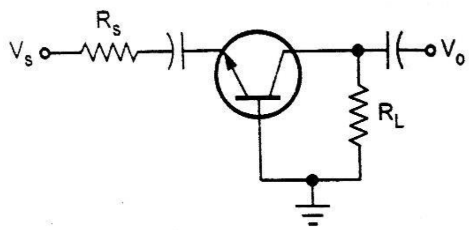
Sub equation (2) in (1)

$\frac{I_e}{V_e} = h_{fc} (\frac{-h_{rc}}{R_s + h_{ic}}) + h_{oc}$

$y_o = \frac{I_e}{V_e} = h_{oc} - \frac{h_{fc}\, h_{rc}}{R_s + h_{ic}}$ *and* $R_o = \frac{1}{y_o}$

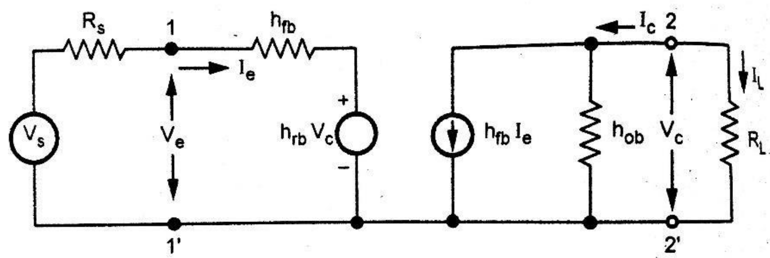
4. Derive the expression for A_i, A_v, R_c and R_o for CB amplifier using h parameter model. ***(April/May 2016)***

Circuit diagram



(a) CB amplifier

h parameter model



(b) h-parameter equivalent circuit for CB amplifier

Current gain (A_I) $A_I = \frac{I_L}{I_e} = \frac{-I_c}{I_e}$

$$I_c = h_{fb}I_e + h_{ob}\, V_c$$

$$h_{fb}I_e + h_{ob}(-I_cR_L) \qquad \therefore V_c = -I_cR_L$$

$$I_c + h_{ob}\, I_cR_L = h_{fb}I_e$$

$$(1 + h_{ob}\, R_L)\, I_c = h_{fb}I_e$$

$$A_I = \frac{I_c}{I_e} = -\frac{h_{fb}}{1 + h_{ob}\, R_L} \qquad \Rightarrow \frac{-I_L}{I_e} = -\frac{h_{fb}}{1 + h_{ob}\, R_L}$$

Input Resistance R_i $R_i = \frac{V_e}{I_e}$

$$V_e = h_{ib}I_e + h_{rb}\, V_c$$

$$V_c = -R_LI_c$$

$$= A_II_eR_L$$

$$R_i = \frac{V_e}{I_e} = \frac{h_{ib}I_e + h_{rb}A_II_eR_L}{I_e}$$

$$R_i = h_{ib} + h_{rb}A_IR_L$$

Voltage gain (A_V) $A_V = \frac{V_c}{V_e} = \frac{A_II_eR_L}{V_e}$

$$= \frac{A_I R_L}{R_c} \qquad \left| \; \frac{I_e}{V_e} = \frac{1}{R_i} \right.$$

Output admittance(Y_0) $Y_0 = \frac{I_c}{V_c}$ with $V_s = 0$

$$I_c = h_{fb} I_e + h_{ob} V_c$$

$$\div V_c \quad \frac{I_c}{V_c} = \frac{h_{fb} I_e}{V_c} + h_{ob} \quad --- (1)$$

When $V_s = 0$

$$R_s I_e + h_{ib} I_e + h_{rb} V_c = 0$$

$$(R_s + h_{ib}) I_e = -h_{rb} V_c$$

$$\frac{I_e}{V_c} = -\frac{h_{rb}}{R_s + h_{ib}} \quad --- (2)$$

Sub (2) in (1)

$$\frac{I_c}{V_c} = h_{fb}\left(\frac{-h_{rb}}{R_s + h_{ib}}\right) + h_{ob}$$

$$y_0 = \frac{I_c}{V_c} = h_{ob} - \frac{h_{fb} \cdot h_{rb}}{R_s + h_{ib}}$$

$$R_o = \frac{1}{y_0}$$

5. **Explain the frequency response operation of BJT amplifier with suitable circuit diagram.**

From the fig 9.1, the capacitors C_S, C_C and C_E will determine the low-frequency response.

C_s is normally connected between the applied source and active device. In fig 9.2The total resistance is now $R_S + R_i$, the cutoff frequency is established as

$$f_{LS} = \frac{1}{2\Pi (R_S + R_i) C_S}$$

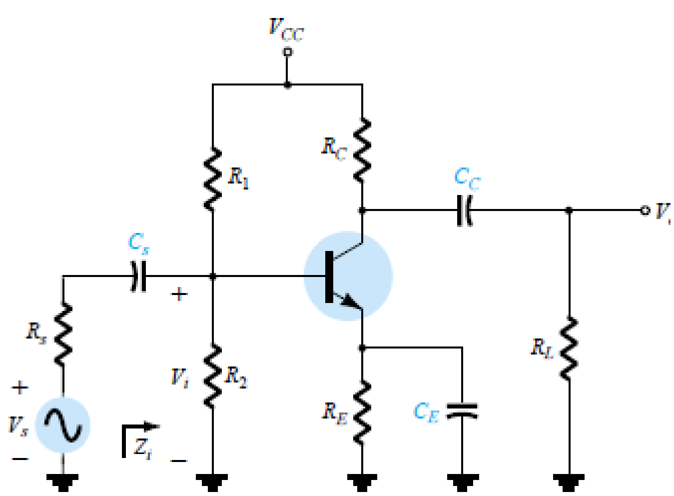


Fig Loaded BJT amplifier with capacitors that affect the low- frequency response

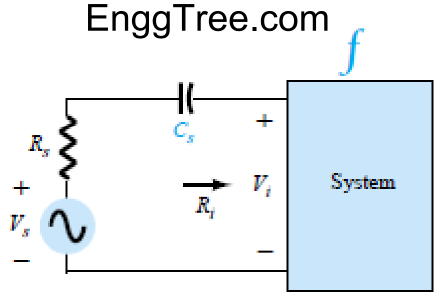


Fig Determining the effect of C_s on the low frequency response

At mid or high frequency, the reactance of the capacitor will be small to permit short circuit approximation for the element. the voltage V_i related to V_S by

$$V_i|_{mid} = \frac{R_i \; V_S}{R_i + R_S}$$

The value of R_i is determined by $R_i = R_1 \| R_2 \| \beta r_e$

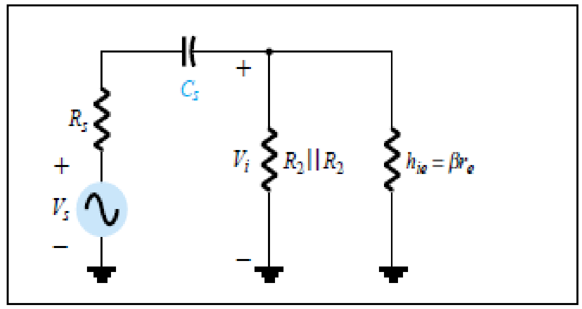


Fig Localized ac equivalent for C_s

The voltage V_i applied to the input of the active device can be calculated using the voltage divider rule: $V_i = \frac{R_i \; V_S}{R_S + R_i - jX_{Cs}}$

Since the coupling capacitor is normally connected between the output of the active device and the applied load, the R-C configuration that determines the low cutoff frequency due to C_C.

From fig 9.4 the total series resistance is now $R_0 + R_L$ and the cutoff frequency is determined by,

$$f_{LC} = \frac{1}{2M(R_0 + R_L)C_C}$$

The resulting value for R_0 , $R_0 = R_C \| r_0$

To determine f_{LE}, C_E must be determined from

$$f_{LE} = \frac{1}{2MR_e C_E}$$

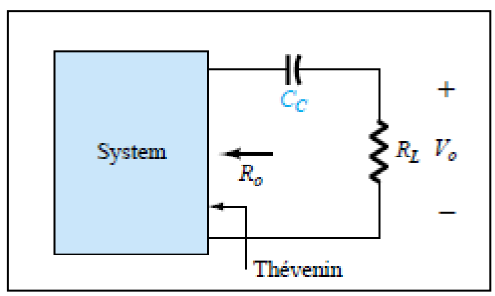


Fig determining the effect of C_c on the low freq

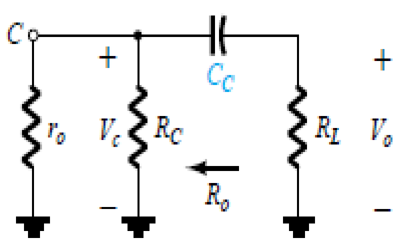


Fig Localized ac equivalent for C_c with V_i=0 V

The value of R_e is determined by $R_e = R_E \| (\frac{RS'}{\beta} + r_e)$.where $R_S' = R_S \| R_1 \| R_2$

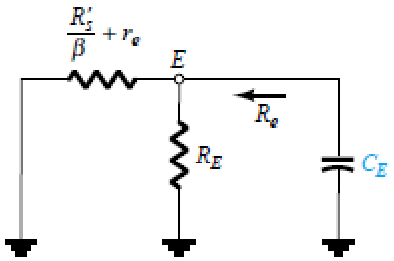


Fig .9.6 Localized ac equivalent of C_E

The effect of C_E on the gain is given by,

$$A_V = - R_C / r_e + R_E$$

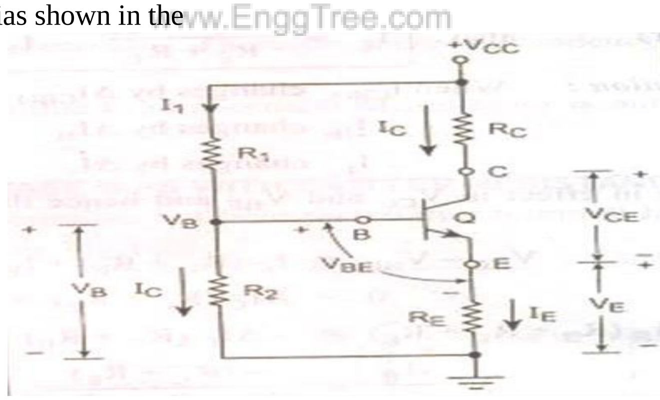
The maximum gain is available where R_E is 0Ω. At low frequency with bypass capacitor C_E in open circuit.

As the frequency increases, the reactance of the capacitor C_E will decrease, reducing the parallel impedance of R_E and C_E until R_E shorted out by C_E.

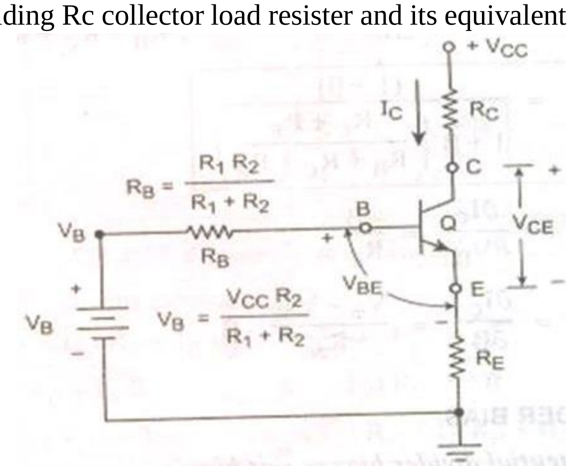
At the midband frequency level, the Short circuit equivalents for the capacitors can be inserted. The highest low frequency cutoff determined by C_S, C_C or C_E.
If there are two or more high cutoff frequencies, the effect will be to raise the lower cutoff frequency and reduce the resulting bandwidth of the system. there is an interaction between the capacitive elements that can affect the resulting low cutoff frequency.

6. Discuss the factors involved in the selection of I_C, R_C and RE for a single stage common emitter BJT amplifier circuit, using voltage divider bias (Nov/Dec2015)

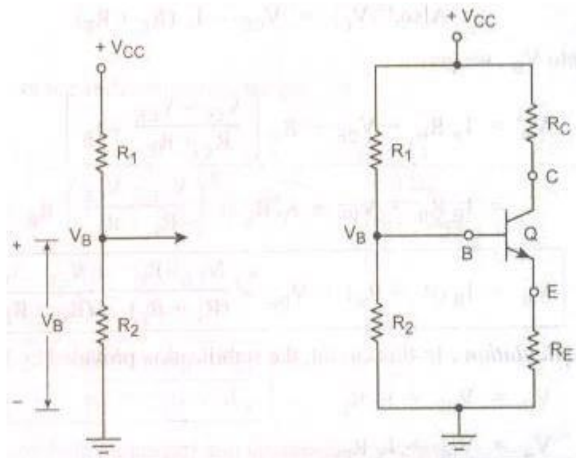
It is also called potential divider bias or self-bias.
In all D.C bias discussed in the above sections clearly states that the values of D.C bias currents and voltage of collector depends on the currents gain$\beta(\beta = \frac{IC}{IB})$. But we know it is purely a temperature sensitive one particularly in silicon type. Hence the nominal value of β is not well defined.
So it is not desirable to provide a D.C bias circuit which is independent of the transistor current gain (β). This is avoided by potential or voltage divider bias shown in the



Here R1 and R2 forms potential dividing Rc collector load resister and its equivalent thevinins circuits is as follows;



This method is widely used since its provides a stable Q-point.
In this method two resistors R1 and R2 connected across the supply voltage Vcc and it provide biasing.
Emitter resistance Re provides bias to BE junction. This causes the base current and hence collector current flows in zero signal condition.
Applying KVL law to BE junction circuit we get fig.



V_B is the voltage across R2 which is given by $V_B = VCC*(R2/ (R1+R2))$
Jut by taking this value as a source voltage and $R_B = R1 \| R2$

$$R_B = \frac{R1R2}{R1 + R2}$$

We can draw the thevinins equivalent circuit which is shown in fig
Then as per KVL law,
$V_B - I_BR_B - V_{BE} - I_ER_E = 0$
$V_B - I_BR_B - V_{BE} - (I_C+I_B) R_E = 0$ $\qquad (I_E = I_B + I_C)$

$V_B = I_BR_B + V_{BE} + (I_C + I_B) R_E$
Then apply KVL to output side we get
$V_{CC} – I_CR_C – I_E R_E – V_{CE} = 0$ $\qquad$ But $I_C=I_E$
$V_{CC} – I_CR_C – I_C R_E – V_{CE} = 0$
$V_{CC} – I_C (R_C + R_E) – V_{CE} = 0$
$I_C (R_C + R_E) = V_{CC} - V_{CE}$
$I_C = V_{CC}- V_{CE} / (R_C + R_E)$
Also $\qquad V_{CE} = V_{CC}- I_C / (R_C + R_E)$
Then put I_c into V_B we get
$V_B = I_B R_B + V_{BE} + R_E [V_{CC}- V_{CE} / (R_C + R_E)+I_B]$
$\quad = I_B R_B + V_{BE} + I_B R_E +[V_{CC}- V_{CE} / (R_C + R_E)]$
$V_B = I_B(R_B+ R_E)+ V_{BE} +[V_{CC}* V_{CE} / (R_C + R_E)]- [V_{CE}* R_E / (R_C + R_E)]$

Gain and frequency response

7. Explain the frequency response of an amplifier with suitable characteristics.

The plot between the gain of the amplifier and frequency of the signal is known as frequency response of the amplifier. The frequency covers a wide range from 0Hz to very high frequencies(> 100MHz).

Decibels: The decibel (dB) is a measure of the difference in magnitude between two power levels. The power gain in decibel is given by,

$$G_{dB} = 10 \log_{10} \frac{P_2}{P_1} \text{ dB}$$

Where P_2 = specified terminal power; P_1 = reference power

If the power P_2 is output power (P_0) and P_1 is input power (P_i) of an amplifier. Then the power gain is given by,

$$G_{dB} = 10 \log_{10} \frac{P_0}{P_i}$$

If V_0 and V_i are output and input voltage of an amplifier then voltage gain, $G_{dB} = 20 \log_{10} \frac{V_0}{V_i}$

The frequency response is divided into three region 1) Low frequency region 2) Mid frequency region 3) High frequency region.

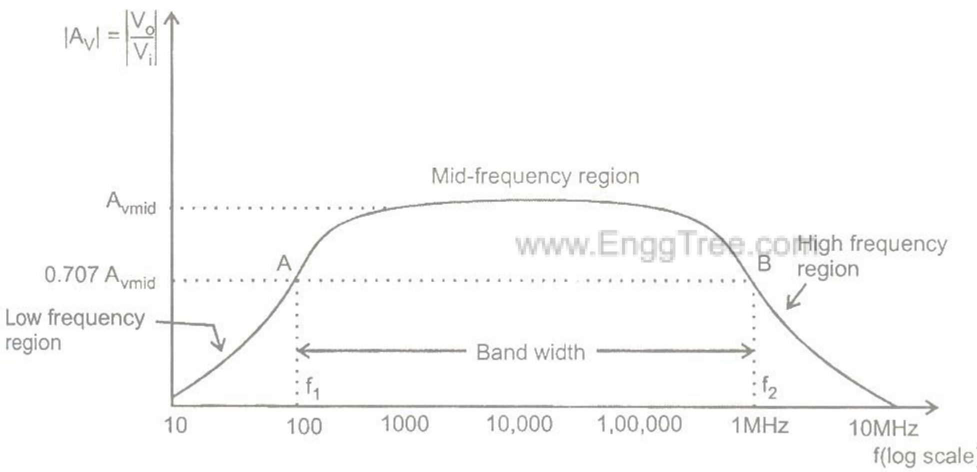


Fig: Frequency response of an amplifier

1) **Mid frequency region:** The gain of the amplifier is maximum A_{Vmid} intersecting the frequency response at point A and B. The corresponding frequencies f_1 ans f_2 are generally called corner, cutoff or half power frequencies. If the maximum voltage gain in mid-band is $A_{Vmid} = V_0 / V_i$ then the gain at half power frequencies is $A_{Vmid} / \sqrt{2}$

   The output power in mid-band is, $P_{o(mid)} = V_0^2 / R_0 = (A_{Vmid} V_i)2 / R_0$

   The power at half power frequency is, $P_{o(HPF)} = V_0^2 / R_0 = (A_{Vmid} V_i / \sqrt{2})^2 / R_0$
   $= P_{0(mid)} / 2$

2) **Cutoff Frequency:** The frequency at which the voltage gain is equal to 0.707 times of its maximum value is called cutoff frequency.

3) **Bandwidth:** The bandwidth of the amplifier is defined as the difference between the two half power frequencies f_1 and f_2

   Bandwidth = $f_2 - f_1$

   Where f_1= the lower cutoff frequency
   f_2=the upper cutoff frequency

4) **Low frequency region:** In midband frequencies the coupling and bypass capacitor are replaced by short circuits.

Capacitive reactance $X_c = \frac{1}{2MfC}$

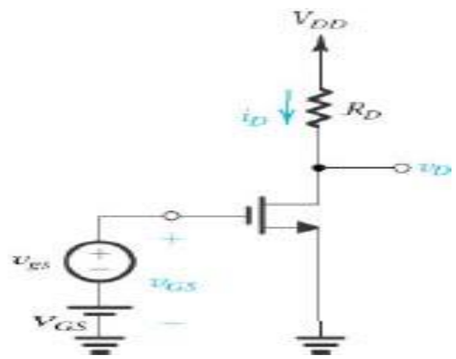
At Low frequency, the coupling and bypass capacitor are increased. Hence the voltage gain decreases.

5) **High frequency region:** Here the internal capacitance across the junction affects the performance of the amplifier.
The capacitance, $C_{b'e}$ = feedback path from bias to emitter
C_{ce} = feedback path from collector to emitter
These capacitors divert the signal to ground.
$C_{b'c}$ = feedback path from base to collector
This provides a bypass path for the input ac signal.

MOSFET-Small Signal Model

8. Draw and explain the small signal model of MOSFET.

To operate as an small signal amplifier,we bias the MOSFET in saturation region.



- The DC bias Point
- The signal current in the drain
- The voltage gain

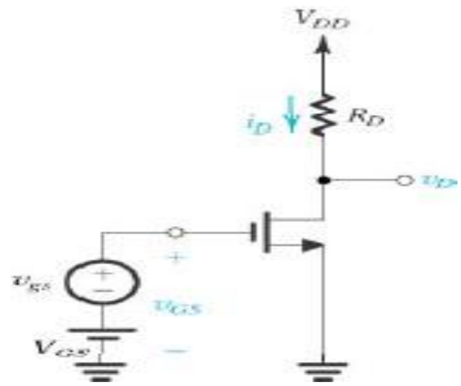
The DC bias Point: I_D - ½ $K_n'(W/L)(V_{GS} - V_t)^2$

$V_D = V_{DD} - I_D R_D$

$V_D \gg V_{GS} - V_t$

The required signal depends on V_D, which is sufficiently greater than ($V_{GS} - V_t$).

The Voltage Gain:



$V_D = V_{DD} - I_D R_D$

$V_D = V_{DD} - (I_D + i_d)R_D$

$V_D = V_{DD} - I_D R_D - i_d R_D$

$V_d = - i_d R_D = - g_m v_{gs} R_D$

$A_v = V_d / V_{gs} = - g_m R_D$

In the small signal analysis, signal are superimposed on the DC quantities,

The drain current, $i_D = I_D + i_d$.

The AC drain current i_d is related to v_{gs} is so called transistor Trans conductance (g_m).

$$g_m \equiv i_d / v_{gs} = ½ K_n (W / L) (V_{GS} – V_t) [S]$$

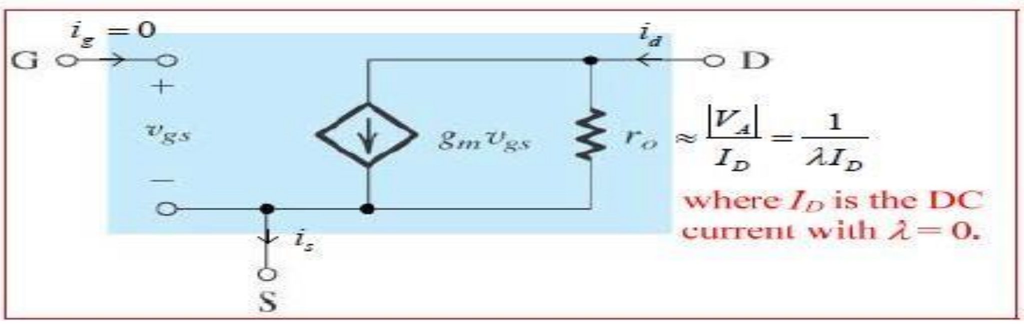
Sometimes expressed in terms of the overdrive voltage, $V_{OV} = V_{GS} – V_t$

$$g_m = K_n'(W / L) V_{OV} [S]$$

This g_m depends on the bias. The Trans conductance g_m equals the slope of i_{D}- v_{gs} characteristic.
Similarly drain voltage, $V_D = V_D + V_d$

In saturation mode, MOSFET acts a voltage controlled current source, The control voltage V_{gs} and output current i_D give rise to small signal Π-model.

For Operation in the saturation region $V_{GD} \le V_t$ ==> $V_{GS} – V_{DS} \le V_t$
Where the total drain to source voltage is $V_{DS} = V_{DS} + v_d$



- $i_g = 0$ and v_{gs}→ infinite input resistance
- r_0 models the finite output resistance in the range from ≈ 10KΩ to 1MΩ and depends on bias current I_D.

$$g_m = K_n'(W / L) (V_{GS} – V_t)$$

it can be, $g_m = I_D / (V_{GS} - V_t)/2$

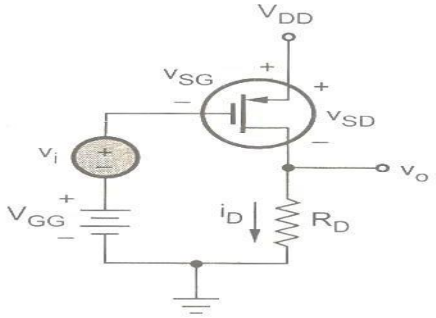
Similar to $g_m = I_C / V_T$ for BJT. Hence the bias current g_m is much larger for than for MOSFET.

MOSFET have these advantages over BJT:

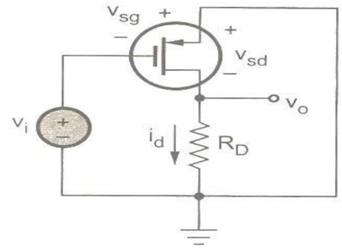
- ✓ High input resistance.
- ✓ Small physical size.
- ✓ Low power dissipation.
- ✓ Relative ease of fabrication.

Becomes amplifiers combines the advantages of BJT and MOSFET, They provide very large input resistance from MOSFET and a large output impedance from the BJT.

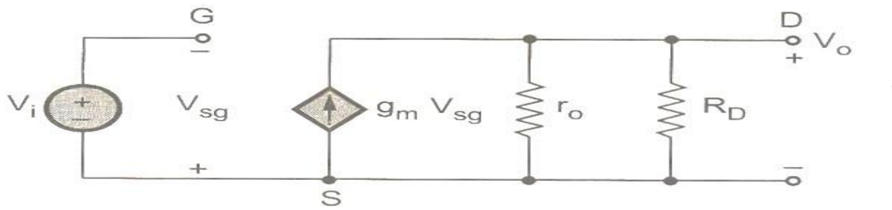
9. Explain Small signal model of P Channel MOSFET.



(a) Common source circuit with PMOS transistor



(b) Corresponding a.c. equivalent circuit



Small signal equivalent circuit of common source amplifier with PMOS transistor model

The above diagram shows the common source circuit with p-channel MOSFET and its A.C equivalent circuit. The A.C equivalent circuit seen for n-channel MOSFET also applies to the p-channel MOSFET; however, there is a change in current directions and voltage polarities compared to the circuit containing the n-channel MOSFET. The above diagram shows the small signal equivalent circuit of the p-channel MOSFET amplifier.

10. Explain the Common – Source (CS) Configuration. (April/May 2019) (Nov/Dec 2017)

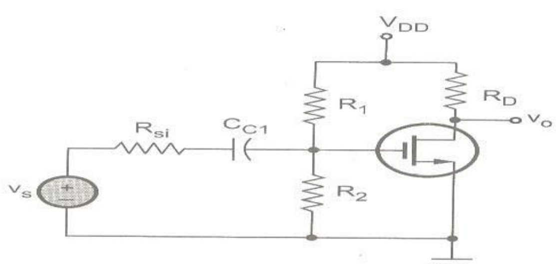
The diagram shows the common source circuit with voltage divider biasing and coupling capacitor. The MOSFET is biased near the middle of the saturation region by R1 and R2 resistors to work as an amplifier.

Assume that,the signal frequency is sufficiently large for the coupling capacitor to act essentially as a short circuit. The signal source is represented by a Thevenin equivalent circuit, in which the signal voltage source vs, is in series with an equivalent source resistance Rsi.

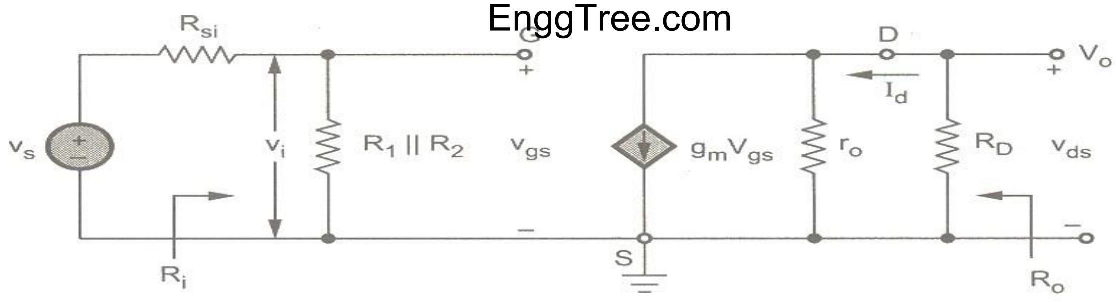
Here R_{si} should me much less than the amplifier input resistance,

$R_i = R_1 \parallel R_2$ in order to minimize loading effects.

The following diagram shows the resulting small- signal equivalent circuit.



Common-source circuit with voltage divider biasing and coupling



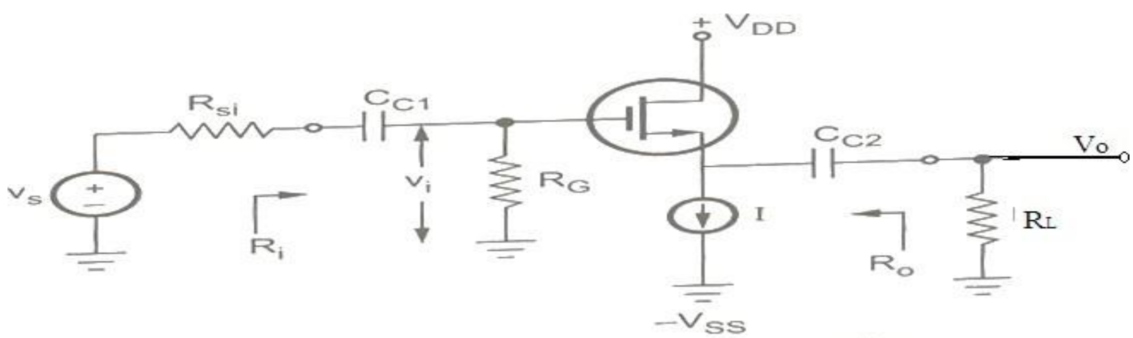
Small-signal equivalent circuit

$v_o = -g_m v_{gs} (r_o \| R_D)$
$v_i = v_{gs}$
$A_v = v_o / v_i = -g_m v_{gs} (r_o \| R_D) / v_{gs} = -g_m(r_o \| R_D)$
The input gate to source voltage is
$v_i = (R_i / R_i + R_{si})\, v_s$
So the small signal overall voltage gain is,

$G_v = v_o / v_s = -g_m(r_o \| R_D)(R_i / R_i + R_{si}) = A_v (R_i / R_i + R_{si})$

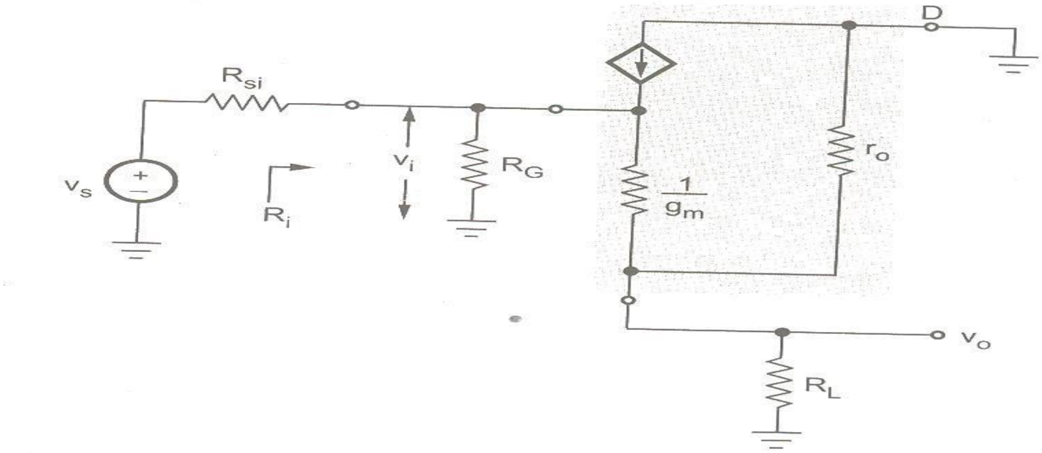
Since Rsi is not zero, the amplifier input signal v_i is less than the signal voltage, This is known as **loading effect**. It reduces the voltage gain of the amplifier.
The input resistance is $R_{is} = R_1 \| R_2$
The output resistance is $R_o = R_D \| r_o$
We can also relate the A.C drain current to the A.C drain to source voltage, as
$V_{ds} = -I_d (R_D)$

11. Analysis of Common – Drain (CD) or Source follower Amplifier.(Nov/Dec 2016)(May 2017)



Common drain amplifier

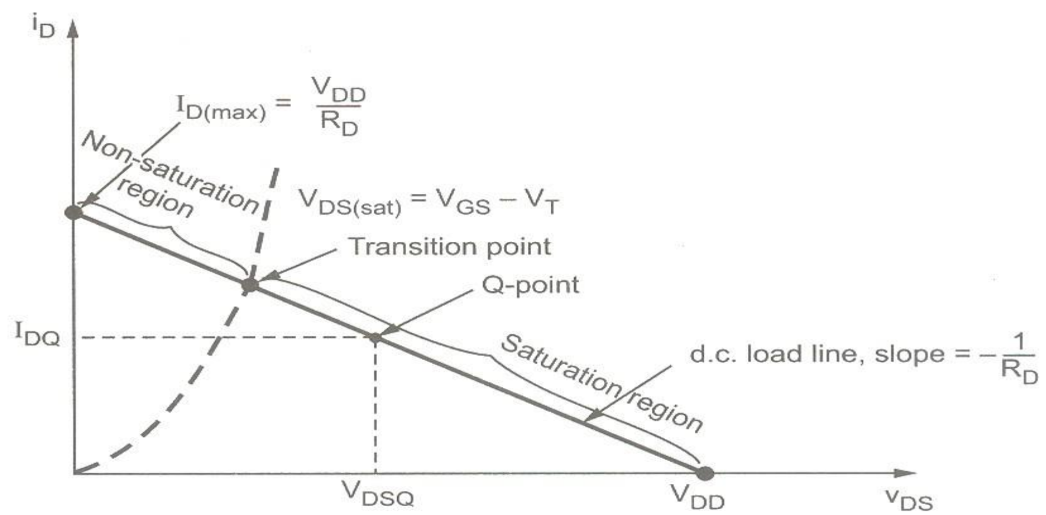
The above diagram shows the common – drain amplifier circuit. It is also known as grounded drain amplifier.
In this amplifier circuit, drain is used as a signal ground and hence RD is not needed.
The input signal is coupled to via Cc1 to the MOSFET gate and the output signal at the output signal at the MOSFET source is coupled via Cc2 to a load resistance RL.
Since RL is in effect connected in series with the source terminal of the MOSFET, it is more convenient to use the MOSFET's T model for the analysis. This is shown in the following diagram.
$R_i = R_G$
$v_i = v_s x R_i / (R_i + R_{si}) = v_s x R_G / (R_G + R_{si})$
From the following diagram it can be seen that the load resistance RL is in parallel with ro and resistance 1/gm in series with $R_L \| r_o$.



Small signal equivalent circuit for CD amplifier

The input voltage v_i appears across the total resistance and hence by applying the voltage divider rule, we have
$v_o = v_i x (R_L \| r_o) / (1/g_m) + (R_L \| r_o)$
$A_v = v_o / v_i = (R_L \| r_o) / (1/g_m) + (R_L \| r_o)$

The open circuit voltage gain A_{vo} (RL = Infinity) is given as
$A_v = r_o /(1 / g_m) + r_o$
Since r_o>> 1 / gm, the open circuit voltage gain tends to unity; however, it is always less than unity.
Usually, R_L<< r_o and hence the voltage gain given by above expression Av becomes
$A_v = v_o / v_i = R_L / (1 / g_m) + R_L$ (R_L<< r_o)
$A_{vs} = G_v = v_o / v_s = v_o / v_i X v_i / v_s$
$= (R_L \| r_o) / (1 / g_m) + (R_L \| r_o) X R_G / (R_G + R_{si})$
The output resistance is given by
$R_o = 1 / g_m \| r_o = 1 / g_m$.

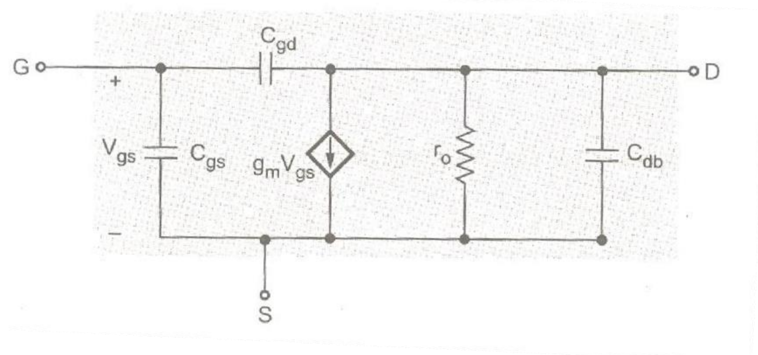


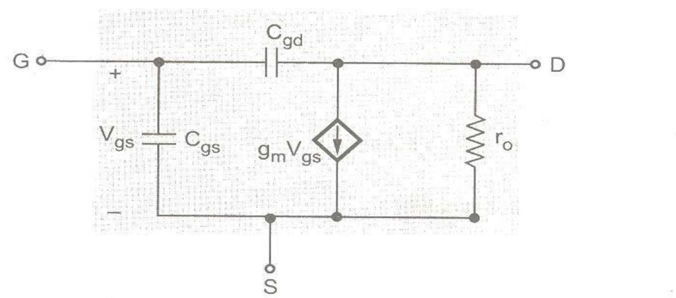
D.C. load line and transition point separating saturation and non-saturatio regions

The above diagram shows the D.C load line, the transition point, and the Q- point, which is in the saturation region.

12. Explain High – Frequency MOSFET Model.

Following diagram shows the high frequency equivalent circuit model for MOSFET. In this model, capacitance C_{db} can be neglected to simplify the analysis. The resulted model is shown

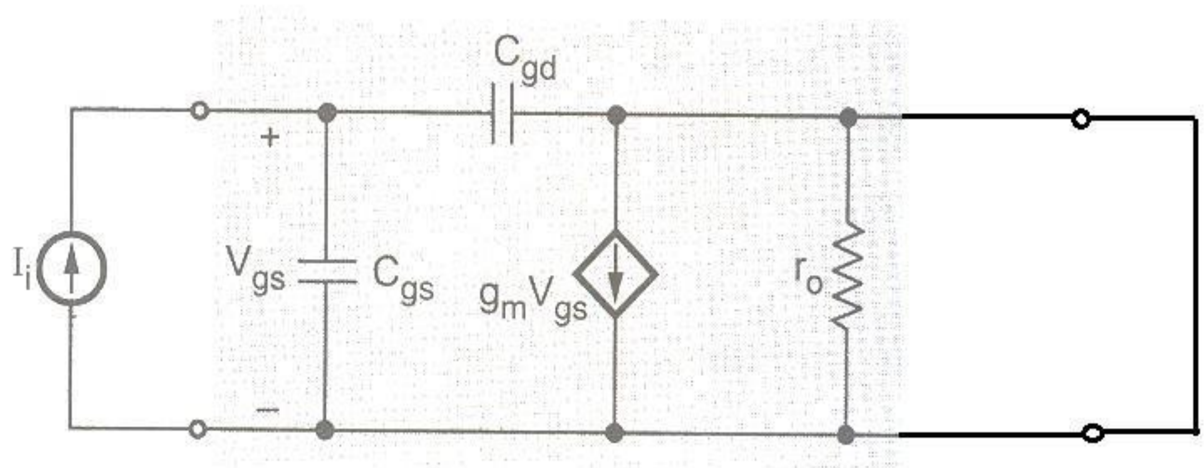




High frequency equivalent circuit neglecting C_{db}

13. Calculate the current gain of high frequency model. (OR)
Derive an expression for MOSFET unity gain frequency(f_T). (April/May 2019)

The f_T is the frequency at which the short – circuit current gain of the CS MOSFET amplifier becomes unity.



The above diagram shows the modified high – frequency equivalent circuit to determine the short – circuit current gain. Here, the input is fed with a current – source signal Ii and the output terminals are shorted.

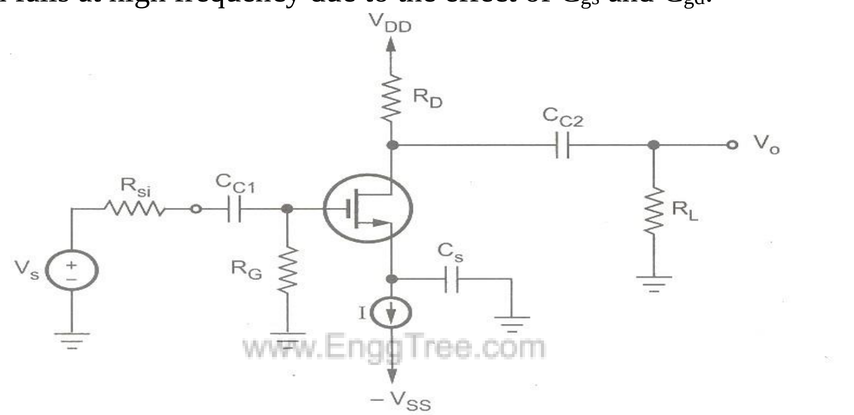
The short circuit current Io is given by

$I_o = g_m V_{gs} - s C_{gd} V_{gs}$

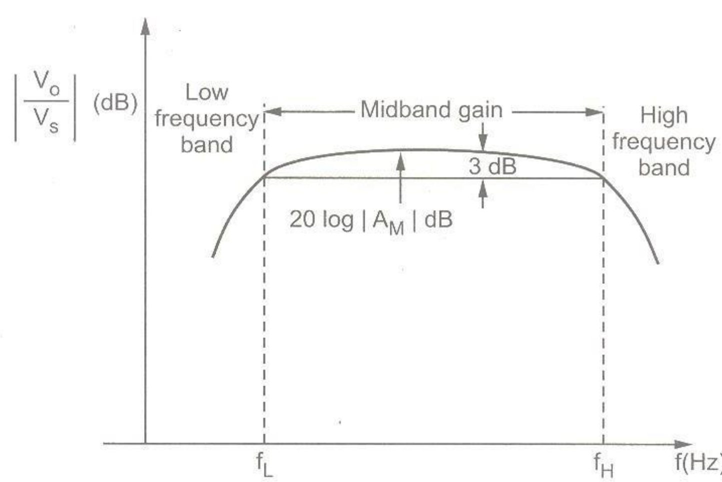
The second term in the above equation is very small and can be neglected at the frequencies of interest and thus
$I_o = g_m V_{gs}$
The Vgs in terms of Ii can be given by
$V_{gs} = I_i / s (C_{gs} + C_{gd})$
Substituting the values of I_i and I_o from the above equations we have
$I_o / I_i = g_m V_{gs} / V_{gs}.s(C_{gs} + C_{gd}) = g_m / s(C_{gs} + C_{gd})$
For physical frequencies s=jω. From above equation it can be seen that the magnitude of the current becomes unity at the frequency.
$\omega_T = g_m / C_{gs} + C_{gd}$
$f_T = g_m / 2\pi (C_{gs} + C_{gd})$
From the above expression we can say that f_T is proportional togm and inversely proportional to the internal capacitances.

14. Explain Frequency response of CS Amplifier. (Apr/May 2018) *(OR)* With neat circuit diagram, perform ac analysis for common source using equivalent circuit NMOSFET AMPLIFIER (NOV/DEC2015)

The following diagram shows the CS MOSFET amplifier. Its gain falls at low frequency due to the effect of C_{c1} and C_s and C_{c2}. Its gain falls at high frequency due to the effect of C_{gs} and C_{gd}.



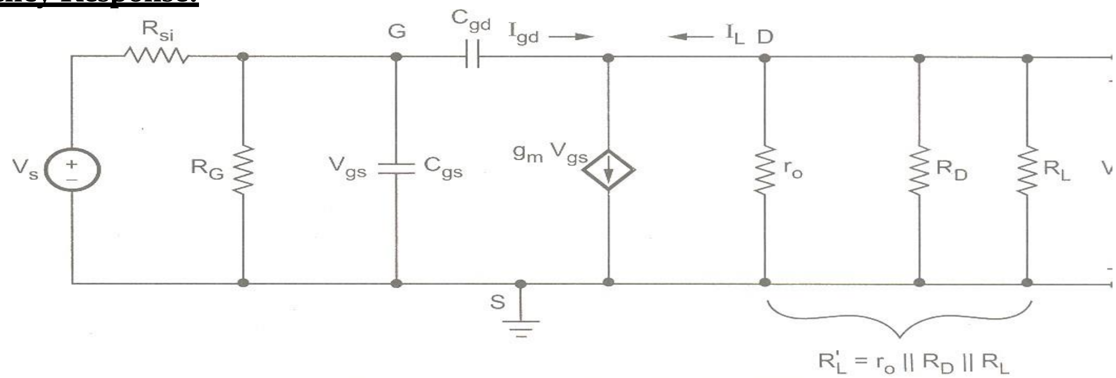
CS MOSFET amplifier



Frequency response of CS MOSFET amplifier

Above diagram shows frequency response of CS MOSFET amplifier.

High Frequency Response:



Equivalent circuit for CS MOSFET amplifier

The above diagram shows equivalent circuit for CS MOSFET amplifier.

Let us consider the output node. The load current is $g_m V_{gs} - I_{gd}$, where $g_m V_{gs}$ is the output current of the MOSFET and I_{gd} is the current supplied through the very small capacitance C_{gd}.

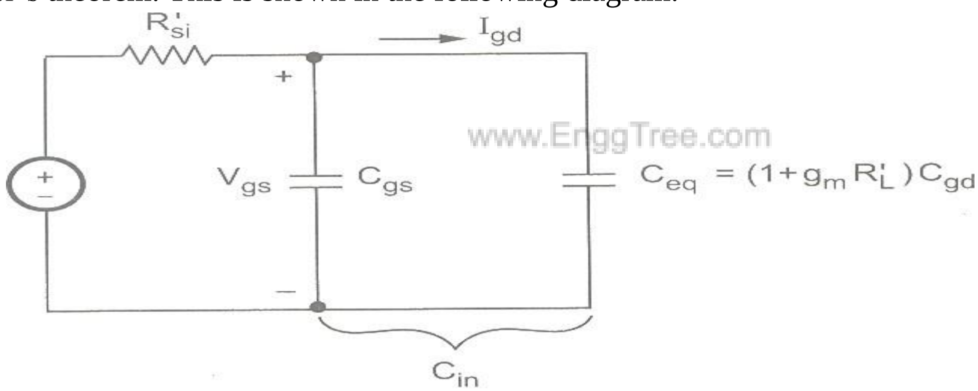
At frequencies in the vicinity of f_H, the I_{gd} is very small and can be neglected.

Hence we can write

$V_o \approx - I_L R_L = - g_m V_{gs} R_L`$

Where $R_L = r_o \parallel R_d \parallel R_L`$

Now consider the input node. We can replace Cgd at the input side with the equivalent capacitance Ceq using Miller's theorem. This is shown in the following diagram.



Input node

By Miller's theorem, equivalent capacitance is given by,

$C_{eq} = (1 + A_v)C = (1 + A_v)C_{gd}$

Since input voltage Vgs, we have

$A_v = V_o / V_i = -g_m V_{gs} R_L` / V_{gs} = - g_m R_L`$

$C_{eq} = (1 + g_m R_L`)$ = Total input capacitance Cin can be given by,

$C_{in} = C_{gs} + C_{eq} = C_{gs} + (1 + g_m R_L`)C_{gd}$

The total resistance is given by,

$R_{si}` = R_{si} \parallel R_G$

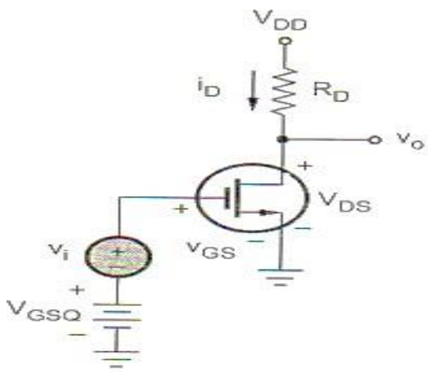
By considering input circuit as a simple- time constant circuit we have

$\tau = RC = R_{si}` C_{in}$

$\omega_H = \omega_o = 1/ \tau = 1 / R_{si}`C_{in}$

$f_H = 1 / 2\pi R_{si}`C_{in}$

15. Explain small signal model of MOSFET.



NMOS common-source circuit with time varying signal source in series with gate d.c. source

From the above diagram, we see that the output voltage is

$v_{ds} = V_o = V_{DD} – i_D R_D$

$v_o = V_{DD} - (I_{DQ} + i_d) R_D \quad = (V_{DD} – I_{DQ} R_D) – i_d R_D$

The output voltage is also a combination of D.C and A.C values. The time – varying output signal is the time – varying drain to source voltage, or

$Vo = Vds = – i_d R_D$

We have,

$i_d = g_m V_{gs}$

In summary, the following relationships exist between the time varying signals for the circuit. The equations are given in terms of the instantaneous A.C values as well as the phasors. We have,

$v_{gs} = v_i$

(or)

$V_{gs} = V_i$ and

$I_d = g_m v_{gs}$

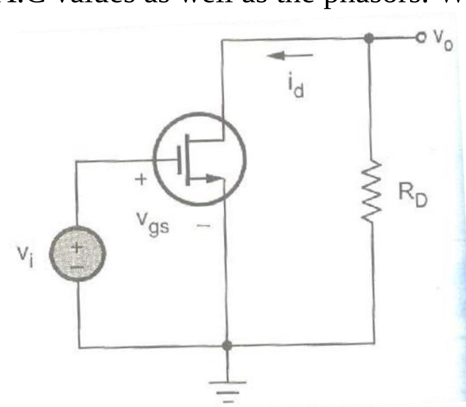
(or)

$I_d = g_m V_{gs}$ also

$v_{ds} = - i_d R_D$

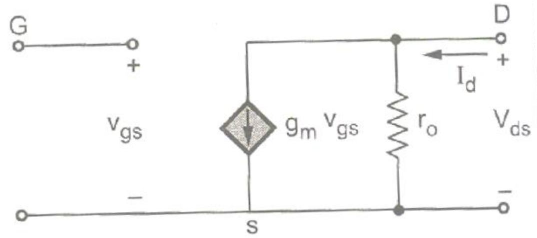
(or)

$V_{ds} = - I_d R_D$

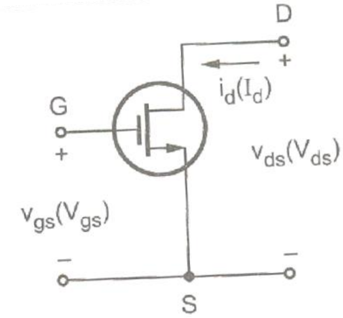


The above diagram shows the A.C equivalent circuit. Here, the D.C sources are made zero.

From the equivalent circuit for the NMOS amplifier circuit, we can draw a small signal equivalent circuit for the MOSFET.



Expanded small signal equivalent circuit, including output resistance, for NMOS transistor



Common-source NMOS transistor with small signal parameters

The above diagram shows the small signal low frequency A.C equivalent circuit for n – channel MOSFET.

The relation of I_d by V_{gs} is included as a current source gm vgs connected from drain to source.
The input impedance is represented by the open circuit at its input terminals, since gate current IG is zero.
We know that the circuit has the finite output resistance of a MOSFET biased in the saturation region because of the nonzero slope in the I_D versus V_{DS} curve.

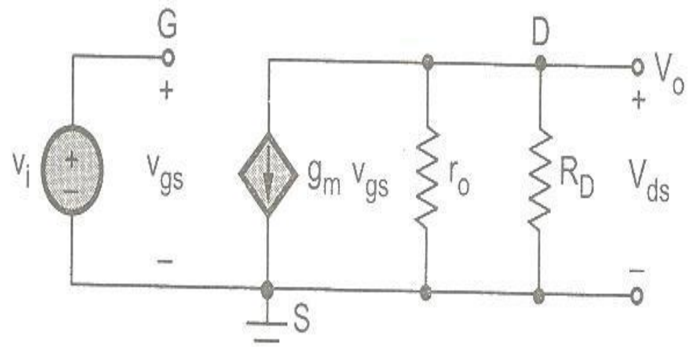
We also know that,
$i_D = K\ [(v_{CS} - V_T)^2(1+\lambda v_{DS})]$

where λ is the channel length modulation parameter and is a positive quantity. The small signal output resistance, is defined as,

$$r_o = (\partial i_D / \partial \mathbf{v}_{DS})^{-1} \big|\ v_{GS} = V_{GSQ} = \text{const.}$$

$$r_o = [\lambda\ K\ [(v_{GSQ} - V_T)^2\ ]^{-1} \approx [\lambda\ I_{DQ}]^{-1}$$

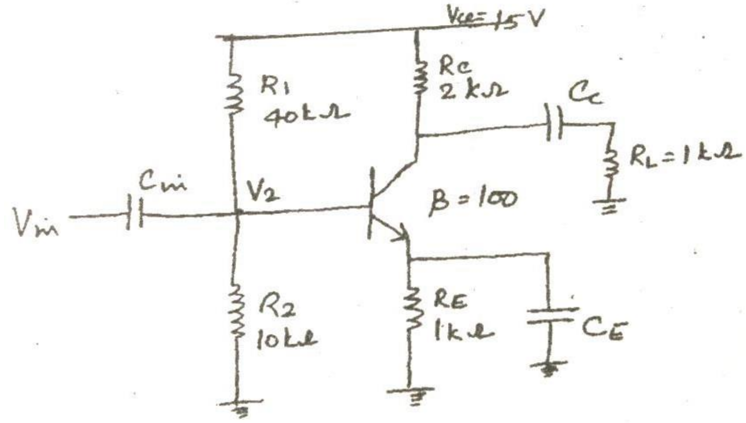
This small signal output resistance is also a function of the Q – point parameters. The following diagram shows the small signal equivalent circuit of common – source circuit.



Small signal equivalent circuit of common-source circuit with NMOS transistor model

Problems

1. **For the circuit below, find (i) dc bias levels (ii) dc voltage across the capacitors (iii) ac emitter resistance (iv) voltage gain (v) state of the transistor. (Nov/Dec 2018)**



Solution:

Given that,

Emitter resistance, R_E=1 KΩ
Collector resistance, R_C=2 KΩ
Load resistance, R_L=1 KΩ
Collector input voltage, V_{CC}=15V
Amplification factor, ß=100
Input resistance, R_1=40 KΩ and R_2=10 KΩ
Voltage gain, A_V= ?
AC emitter resistance, r_e= ?

i. DC bias levels: DC bias levels of CE amplifier determined by calculating various dc voltages and dc currents.
DC voltage, V_2 across resistor, R_2 is

$$V_2 = \frac{V_{CC}}{R_1 + R_2} X R_2$$

Substituting the corresponding values, V_2 is obtained as,

$$V_2 = \frac{15}{40 + 10} X\, 10$$

V_2= 3 V

DC emitter voltage, V_E across emitter resistor, R_E is,

$V_E = V_2 - 2V_{BE}$
= 3 V- 0.7 V
= 2.3 V

DC emitter voltage, V_E= 2.3 V

DC emitter current, I_E is given by,

$$I_E = \frac{V_E}{R_E}$$

$$I_E = \frac{2.3\, V}{1\, K\Omega} = 2.3\, mA$$

DC Collector voltage, V_C is determined as, $V_C = V_{CC} - I_C R_C$

V_C=15 V - 2.3 X 2 KΩ since $[I_E = I_C]$

V_C = 10.4 V

DC base current, I_B is obtained as,

Using the relation I_C = ß I_B

$$I_B = \frac{I_C}{ß} = \frac{2.3\, mA}{100} = 0.023\, mA$$

ii. **DC voltages across the capacitors:** From the above calculations, DC voltages across capacitors in the circuit is obtained as,

DC voltage across capacitor, C_{in} is, $V_2 = 3$ V

DC voltage across emitter capacitor, C_E is , $V_E = 2.3$ V

DC voltage across collector capacitor, C_C is $V_C = 1.4$ V

iii. **AC Emitter Resistance:** The ac emitter resistance, r_e' is given by, $[I_E = 2.3 \text{ mA}]$

$$r'_e = \frac{25 \text{ mV}}{I_E} = \frac{25 \text{ mV}}{2.3 \text{ mA}} = 10.9\ \Omega$$

iv. **Voltage Gain(A_V):** The voltage gain A_V of CE amplifier is defined by,

$$A_V = \frac{r_c}{r'_e}$$

Here, total ac collector resistance, r_c is determined by, $r_e = R_c \parallel R_L$

$$r_c = \frac{R_C R_L}{R_C + R_L} = \frac{2 X 1}{2+1}\ 10.9\Omega = 0.667\ K\Omega$$

Substituting r_c value in A_V, implies,

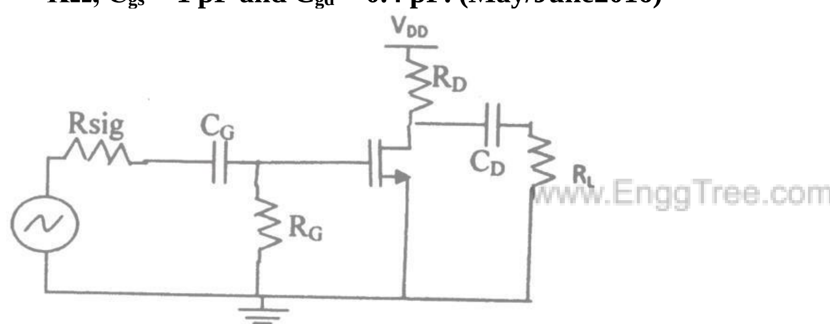
$$A_V = \frac{0.667\ K\Omega}{10.9\ \Omega}$$

Voltage gain, $A_V = 61.2$

v. **State of transistor:** From the above calculation it can be determined that the transistor is in active state.

Since $V_C > V_E$

2. **Determine the mid band gain, the upper 3 dB frequency f_H of a CS amplifier fed with a signal source having an internal resistance $R_{sig} = 100$ KΩ. The amplifier has RG = 4.7 MΩ, $R_D = R_L = 15$ KΩ gm = 1 mA/V, $r_o = 150$ KΩ, $C_{gs} = 1$ pF and $C_{gd} = 0.4$ pF. (May/June2016)**



Solution: $A_M = \frac{R_G}{R_G + R_{Sig}} g_m R'_L$

Where $R'_L = r_0 \| R_D \| R_L = 150 \| 15 \| 15 = 7.14\text{K}\Omega$

$$g_m R'_L = 1 \times 7.14 = 7.14 V/V$$

Thus $A_M = -\frac{4.7}{4.7+0.1} \times 7.14 = -7V/V$

The equivalent capacitance C_{eq} is found as

$$C_{eq} = (1 + g_m R'_L) C_{gd} = (1 + 7.14) \times 0.4 = 3.26pF$$

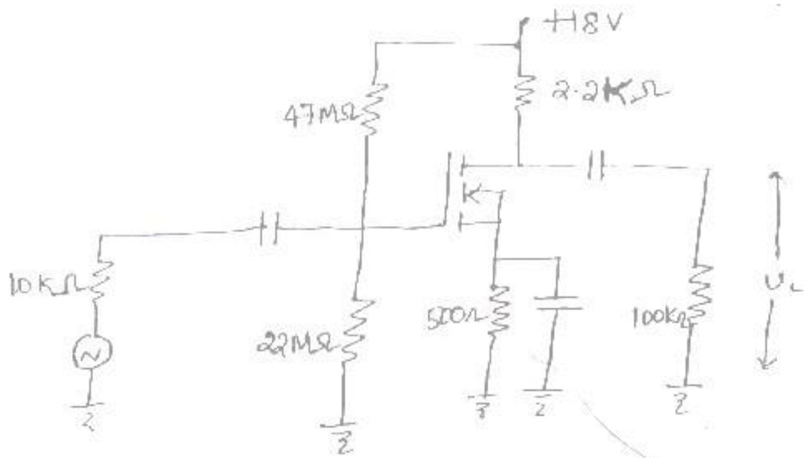
The total input capacitance C_{in} can be now obtained as

$$C_{in} = C_{gd} + C_{eq} = 1 + 3.26 = 4.26\ pF$$

The upper 3 dB frequency f_H is found from

$$f_H = \frac{1}{2\pi C_{in}(R_{sig} \| R_G)} = \frac{1}{2\pi \times 4.26 \times 1^{-12} (0.1 \| 4.7) \times 10^6} = 382\ kHz$$

3. The MOSFET shown fig has the following parameter V_T = 2V, $Q = 0.5 \times 10^{-3}$, r_d = 75KΩ. It is biased at at I_D = 1.9m A. (Nov/Dec2017)



a) Verify that the MOSFET is biased in its active region.
b) Find the input resistance.
c) Draw the small single equivalent circuit and find the voltage gain VL/VS.

Solution:

a) $V_{DS} = V_{DD} - I_D(R_D + R_S)$ = 18 – (1.9mA)(2.2 * 103 + 500) = 12.87V

$$V_G = \left(\frac{22 * 10^6}{47 * 10^6 + 22 * 10^6}\right) 18 = 5.74V$$

Using equation 7.25 to find V_{GS}, we have

V_{GS} = 5.74-(1.9)(5) = 4.79V

$$|V_{GS} - V_T| = |4.79 - 2| = 2.79V$$

Therefore condition 8.30 is satisfied;

$$12.87 = |V_{DS}| > |V_{GS} - V_T| = 2.79$$

And we conclude that the MOSFET is biased in its active region.

b)

$$r_{in} = R_1 \| R_2 = (47M\Omega \| (22M\Omega) = 15M\Omega$$

c) From equation 8.31,

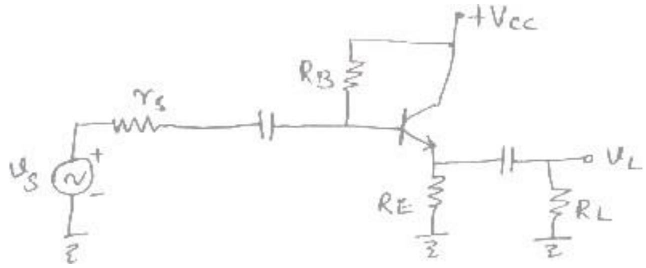
$g_m = 0.5 * 10^{-3}(4.79 - 2) = 1.4 * 10^{-3}$ S

The small single equivalent circuit is shown in fig 8.33 from equation 8.33

$$\frac{v_L}{v_s} = \left(\frac{15 * 10^6}{10 * 10^3 + 15 * 10^6}\right) * (-1.4 * 10^{-3})[(75 * 10^3 \| (2.2 * 1^3 \| (100 * 10^3)]$$

$= (0.999)(-1.4*10^{-3})(2.09*10^3) = -2.92$

4. A CC amplifier shown in below figure has V_{CC} = 15V, R_B = 75KΩ and R_E = 910 Ω the Q of the silicon transistors is 100 and the load resistor is 600 Ω find r_{in} and A_V. (Nov/Dec 2015)



Given:

V_{CC} = 15V, R_B = 75KΩ, R_E = 910 Ω, $\beta = 100$, *RL = 600* Ω

To Find: r_{in} and A_V

Formulae used $I_B = \frac{V_{CC}-0.7}{R_B+(\beta+1)R_E}$, $I_E = (1+\beta)I_B$, $r_E = \frac{0.026}{I_E}$

$$r_{in}(stage) = (\beta+1)(r_e + r_L)\|R_B$$

$$V_L = R_E\|R_L$$

$$r_{in}(stage) = (\beta+1)(r_e + R_E)$$

$$r_o(stage) = R_E\|r_e \qquad (r_s = 0)$$

$$A_r = \frac{V_L}{V_S} = \frac{R_E}{r_E + R_E}\ (output\ open)$$

Calculation:

$$I_B = \frac{V_{CC}-0.7}{R_B+(\beta+1)R_E} = \frac{15-0.7}{75000+(100+1)910} = \frac{15-0.7}{75000+101*910} = \frac{143}{166910}$$

$$= 8.5674 \times 10^{-4}A$$

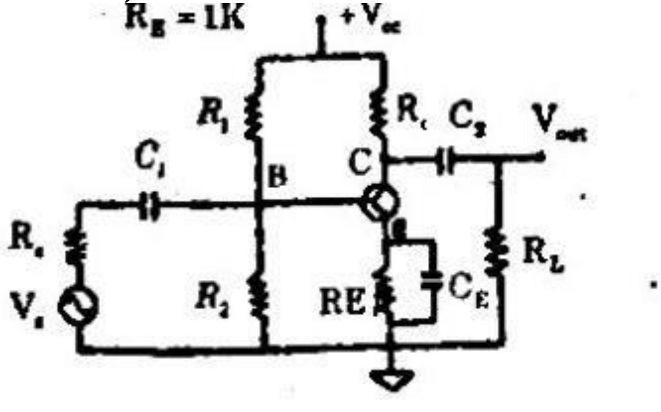
$$I_E = (1+\beta)I_B = (101) \times 8.5674 \times 10^{-4} = 0.08653A$$

$$r_E = \frac{0.026}{I_E} = \frac{0.026}{0.08653} = 0.300$$

$$r_{in}(stage) = (\beta+1)(r_e + R_E) = (101) \times (0.300 + 910) = 91940.3\ ohms$$

$$A_V = \frac{V_L}{V_S} = \frac{R_E}{r_E + R_E} = \frac{910}{910 + 0.300} = 0.999$$

5. Evaluate the A_I, A_V, R_i, R_o, A_{is}, A_{vs} of a single stage CE amplifier with R_s=1 KΩ R_1=22KΩ, R_2=10KΩ, R_c=2KΩ, R_L=2KΩ, h_{fe}=50,h_{ie}=1.1KΩ, h_{oe}=25μA/V and h_{re}=2.5X10^{-4} (Nov/Dec 2016)



Given

R_s=1 KΩ R_1=22KΩ,R_2=10KΩR_c=2KΩ,R_L=2KΩ,h_{fe}=50,h_{ie}=1.1KΩ,h_{oe}=25μA/V and h_{re}=2.5X10^{-4}.

i)Current gain

$$A_i = -h_{fe} = -50$$

ii) Input impedance $R_i = h_{ie} = 1.1\ k\Omega$

$$R_i = h_{ie} \| R_1 \| R_2$$
$$= 1.1 \times 10^3 \| 22 \times 10^3 \| 10k\Omega$$
$$= 1.1 \times 10^3 \| [\frac{22 \times 10 \times 10^6}{32 \times 10^3}]$$
$$= 1.1 \times 10^3 \| [\frac{220 \times 10^3}{32}]$$

$$= 1.1 \| 6.87k$$
$$= \frac{1.1 \times 6.87 \times 10^6}{(1.1 + 6.87)10^3} = \frac{7.56 \times 10^6}{7.975 \times 10^3} = 0.947 \times 10^3 = 947\ \Omega$$

iii)Voltage gain

$$A_v = \frac{A_I R_L'}{R_i} = \frac{-50 \times (R_c \| R_L)}{R_i} = \frac{-50(2k \| 2k)}{1.1k} = -45.45$$

Output voltage

$$R_0 = \frac{1}{y_0} = \infty$$
$$R_0' = R_0 \| R_L' = \infty \| 2k \| 2k = 1k$$

Over all voltage gain

$$A_{vs} = A_V \times \frac{V_{in}}{V_s}$$
$$A_{vs} = \frac{V_o}{V_s} = \frac{V_o}{V_b} \times \frac{V_b}{V_s}$$

$$where\ \frac{V_o}{V_b} = Av\ and \qquad \frac{V_b}{V_s} = \frac{R_1}{R_1 + R_3}$$

$$A_{vs} = \frac{AvR_i'}{R_i' + R_s} = \frac{-45.45 \times 947}{947 + 1k} = \frac{-45.45 \times 947}{1947} = -22.106$$

Overall current gain

$$A_{is} = \frac{I_L}{I_S} = \frac{I_L}{I_C} \times \frac{I_C}{I_b} \times \frac{I_b}{I_S}$$

$$\frac{I_L}{I_C} = \frac{R_c}{R_c + R_L} = \frac{-2k}{2k + 2k} = \frac{-2k}{4k} = -0.5$$

$$\frac{I_C}{I_b} = h_{fe} = 50$$

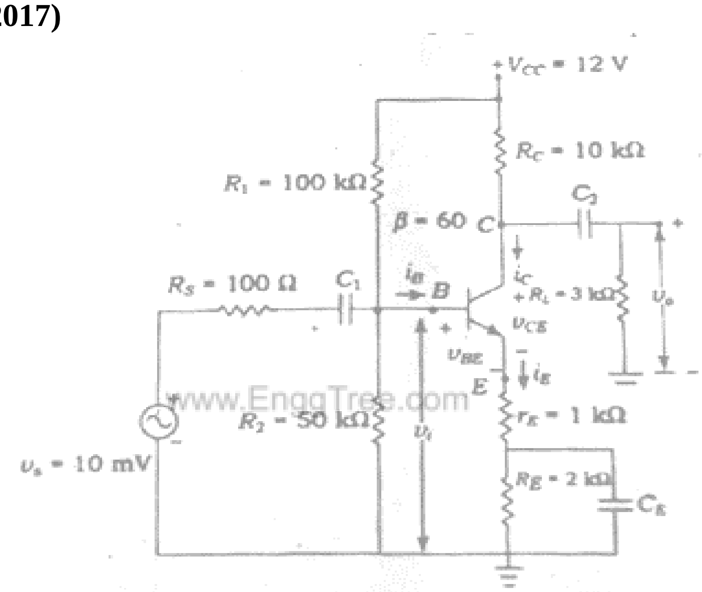
$$\frac{I_b}{I_S} = \frac{R_B}{R_B + R_i} = \frac{22\|10}{22\|10 + 1.1k} = \frac{6.87k}{6.87k + 1.1k} = \frac{6.87}{7.97} = 0.86$$

$A_I = \frac{I_L}{I_S}$

$= -0.5 \times 50 \times 0.86$

$A_{IS} = -21.54$

6. Fig shows a common emitter amplifier. Determine the input resistance, ac load resistance, voltage gain and output voltage?(May 2017)



Given:

$V_{CC} = 12\,V, R_C = 10\,k\Omega, R_\alpha = 3\,k\Omega, \beta = 60, R_1 = 100\,k\Omega, R_2 = 50\,k\Omega, r_E = 1\,k\Omega, R_{E1} = 2\,k\Omega, R_S = 100\,\Omega,$

$$V_s = 10\,mV$$

Input resistance looking directly into the base.

$$V_{th} = V_{CC}\left(\frac{R_2}{R_1 + R_2}\right) = 12\left(\frac{50 \times 10^3}{100 \times 10^3 + 50 \times 10^3}\right)$$

$$= 12\left(\frac{50}{150}\right) = \frac{12}{3} = 4\,V$$

$$R_{th} = R_1 \| R_2$$

$$= \frac{100 \times 50 \times 10^3 \times 10^3}{10^3 \times 100 + 50 \times 10^3} = \frac{100 \times 50 \times 10^3}{10^3(150)}$$

$$= \frac{500 \times 10^3}{15} = \frac{100 \times 10^3}{3} = 33.3 \times 10^3\Omega = 33.3\,k\Omega$$

$$Emitter\ resistance\ (R_E)$$

$$R_E = R_{E1} + R_E = 1k\Omega + 2k\Omega = 3k\Omega$$

$$I_E = \frac{V_{th} - V_{BE}}{R_E + \frac{R_{th}}{\beta}}$$

$$= \frac{4 - 0.7}{3 \times 10^3 + \frac{33.3 \times 10^3}{60}}$$

$$I_E = \frac{3.3}{3555.55} = 0.000928 = .92mA$$

A.C resistance

$$r_e^1 = \frac{25}{I_E(mA)} = \frac{25}{0.92}$$

Input resistance

$$R_i = \beta(r_E + r_e^1) = 27\Omega$$

$$= 60(1 \times 10^3 + 27)$$

$$= 61620\ \Omega$$

$$= 61.6\ k\Omega$$

Input resistance of the stage

$$R_{is} = (R_1 \| R_2) \| \quad [\beta(r_E + r_e^1)]$$

$$= \frac{33.33 \times 61.6 \times 10^3 \times 10^3}{33.33 \times 10^3 + 61.6 \times 10^3}$$

$$= \frac{2053.12 \times 10^3}{94.93}$$

$$= 21.62\ k\ \Omega$$

A.C load resistance

$$r_2 = R_c \| R_L$$

$$= 10k \| 3k$$

$$= \frac{10 \times 3 \times 10^6}{13 \times 10^3} = \frac{30}{13} \times 10^3 = 2.3\ k\Omega$$

$$A_v = \frac{r_L}{r_E + \gamma_e^1} = \frac{2307}{1 \times 10^3 + 27} = 2.246$$

Overall voltage gain

W.K.T the ratio of base to source voltage

$$\frac{V_{in}}{V_s} = \frac{R_{iS}}{R_S + R_{iS}} = \frac{21.62 \times 10^3}{100 + 21.62 \times 10^3} = \frac{21.62 \times 10^3}{21720} = 0.99$$

$$\therefore over\ all\ voltage\ gain$$

$$A_{vs} = A_V \times \frac{V_{in}}{V_s} = 2.246 \times 0.99 = 2.235$$

Output voltage

$$V_O = A_{VS} \times V_S = 2.235 \times 10\ mV$$

$$V_O = 22.35\ mV$$

7. An NPN common emitter amplifier circuit has the following parameters: h_{fe}=50, h_{ie}=1KΩ and R_c=3KΩ. Find the voltage gain of the amplifier. (April/May 2019)

$$A_V = \frac{A_I R_L}{R_i}; \qquad A_I = -h_{fe}; \qquad R_i = h_{ie}; R_L = R_C;$$

$$A_V = \frac{-50 \ X \ 3 \ X \ 10^3}{1 \ X \ 10^3}; \qquad A_I = -50; \qquad R_i = 1K; R_L = 3K;$$

$$\boldsymbol{A_V = -150}$$

8. A common emitter amplifier has an input resistance 2.5 kΩ and voltage gain of 200.If the input signal voltage is 5mV. Find the base current of the amplifier. (May 2017) (Nov/Dec 2017)

W.K.T

i_b-base current, R_i=2.5 kΩ, V_s=5mV

$2.5X10^{-3} = \frac{V_s}{i_b} = 5x10^{-3}/i_b \therefore i_b = 2 \times 10^{-6} A = 2\mu A$

9. For a certain D-MOSFET, I_{DSS}=10 mA and $V_{GS(off)}$= -8 V. check if it is an n-channel or p-channel device? Justify your answer. (Nov/Dec 2018)

Given that,

For a D-MOSFET,

Saturation currents, I_{DSS}=10 Ma

Gate to source cut-off voltage, $V_{GS\ (off)}$= -8V

Since the D-MOSFET has negative $V_{GS\ (off)}$. The device is n-channel D-MOSFET.

1. Derive the expression for current gain, input impedance and voltage gain of a CE transistor Amplifier. (Nov/Dec 2016) (Apr/May 2018)

The ac equivalent circuit can be obtained by replacing all the capacitors and voltage sources by a short circuit.

Characteristics of CE amplifier:

A. Without Emitter Resistor

(1) It has good voltage gain with phase inversion i.e., the output voltage is 180° out of phase with input.
(2) It also has good current gain, power gain and relatively high input and output impedance.

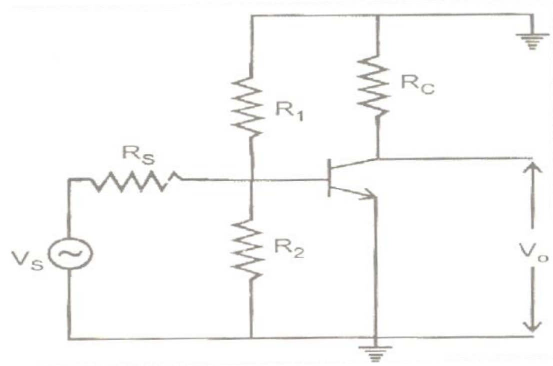


Fig. ac equivalent circuit of CE amplifier

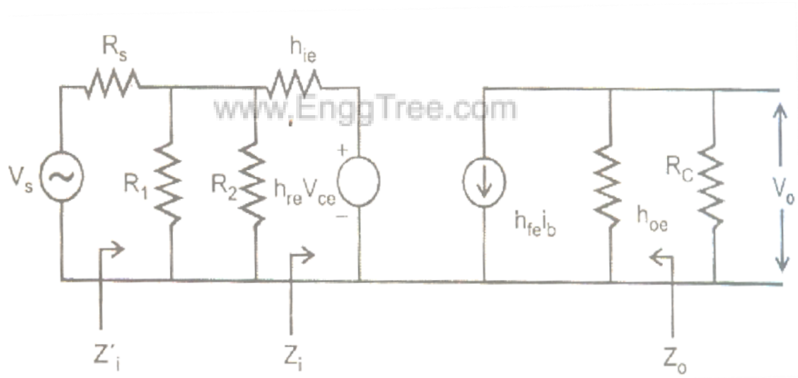


Fig. h-parameter model of CE amplifier

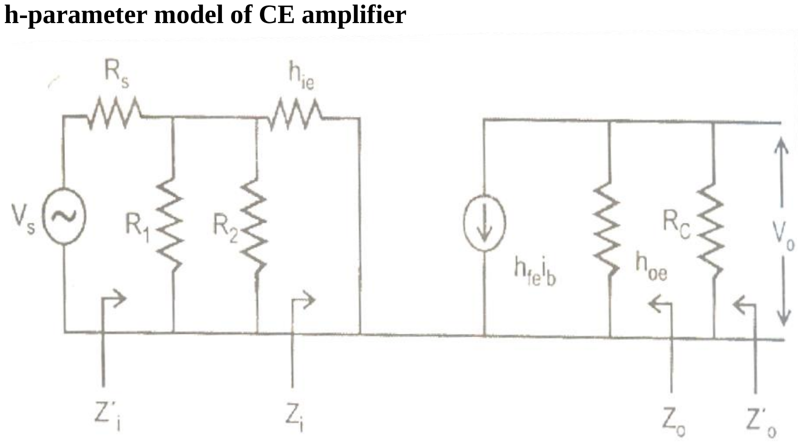
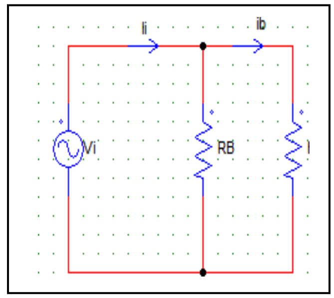


Fig Approximate hybrid model of CE amplifier

Assume h_{re}=0,

The input impedance: h_{ie} seen to be in series with $h_{re}V_0$.For CE circuit, h_{re} is normally a very small quantity. So that the voltage $h_{re}V_0$ fed back from the output to the input circuit is much smaller than the voltage drop across h_{ie}.

$$Z_i' = R_B \,||\, h_{ie} \qquad \text{where } R_B = R_1 \,||\, R_2$$



The output impedance: The output voltage variation have liitle effect upon the input of CE circuit, only the output half of the circuit need to be considered in determining the output impedance.

$$Z_0' = R_C \frac{1}{h_{oe}}$$

The voltage gain: $A_V = V_0 / V_i$

W.K.T $\quad V_0 = -i_c R_c \qquad V_i = i_b h_{ie}$

Where $h_{re} V_0$ is assumed short circuited.

$$i_c = h_{fe} i_b$$

$$A_V = -(h_{fe} R_C) / h_{ie}$$

Current Gain:

$$A_I = I_0 / I_i = i_c / I_i$$

$$= \frac{-i_c}{i_b} \cdot \frac{i_b}{I_i} = -h_{fe} \frac{i_b}{I_i} \qquad \frac{i_b}{I_i} = R_B / (h_{ie} + R_B)$$

$$= -h_{fe} R_B / (h_{ie} + R_B)$$

B. With emitter resistor:

A common emitter amplifier with emitter resistor Re provides feedback and voltage gain stabilized in a CE amplifier But it reduces the gain.

To obtain h-parameter model of the circuit, we replace the transistor by its h-parameter model.

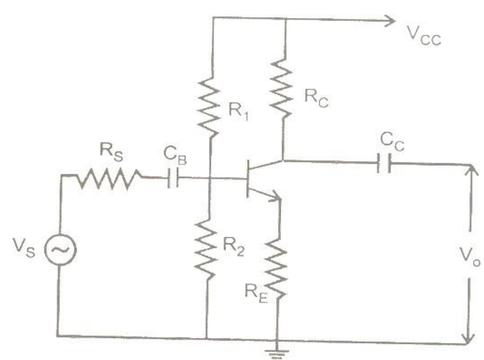


Fig. CE amplifier with Emitter resistor

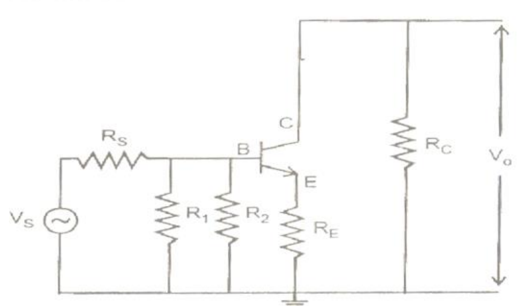


Fig. AC equivalent circuit of CE amplifier with Emitter resistor

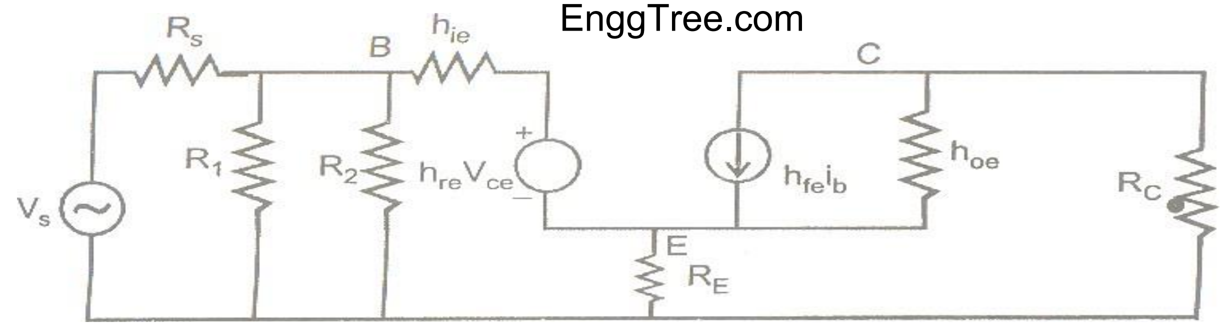


Fig .h-parameter model of a CE amplifier with emitter resistor

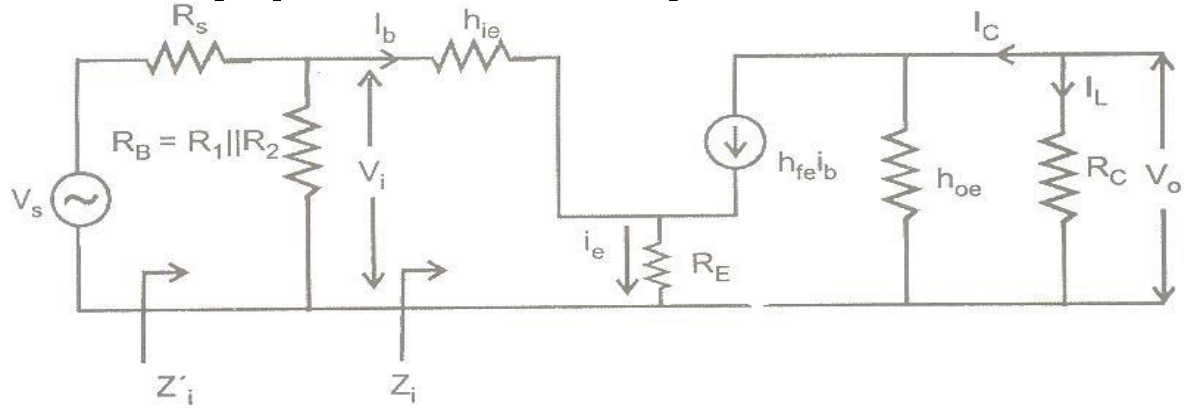


Fig .Approximate Model

Assuming h_{re} is very low, **The input impedance**

$Z_i' = R_B \| Zi$

$Z_i = V_i / I_i = V_i / i_b$ ------------------1

$V_i = h_{ie}\, i_b + i_e\, R_E$ W.K.T $(i_e = i_b + i_c)$

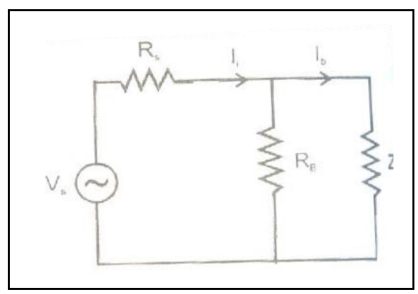
$i_e = i_b + h_{fe}\, i_b = (1+h_{fe}) i_b$ ------------2

sub eq(2) in eq(1), $V_i = i_b\, (h_{ie} + (1+h_{fe})\, R_E)$

$Z_i = V_i / i_b = h_{ie} + (1+ h_{fe})\, R_E$ -------- 3

$Z_i = R_B \|$ Zi

$= R_b \| (h_{ie} + (1+h_{fe}) R_E)$-------------- 4



Voltage Gain: $A_v = V_0 / V_i$ -----------------5

$Vo = I_L\, R_C$

$= -\, i_c\, R_c$ where$(i_c = h_{fe}\, i_b)$

$= -h_{fe}\, i_b\, R_c$

$V_i = I_i\, Z_i$

$= i_b\, (h_{ie} + (1+h_{fe})\, R_E)$ -----------------6

Sub eq(6) and eq(6) in eq(4)

$A_V = V_0 / V_i = -\, h_{fe}\, R_C\, i_b / (h_{ie} + (1+h_{fe})\, R_E)\, i_b$

$= -\, h_{fe}\, R_C / h_{ie}\, (1+h_{fe})\, R_E$-----------------------7

Since $(1+h_{fe})R_E >> h_{ie}$ $A_v = -\, h_{fe}\, Rc / (1+h_{fe})R_E$ ------------------------8

Since $h_{fe} >> 1$ $A_v = -\, R_C / R_E$ -------------------------- 9

Output impedance: $Z_0 = R_C$-------------- 10

Current gain: The current gain is defined as the ratio of output current to input current

$A_I = I_0 / I_i = I_0 / i_b \cdot i_b / I_i$

$I_0 = - i_c$

$A_I = - h_{fe} \; i_b / I_i$ 11

using voltage divider rule, $I_b / I_i = R_B / R_B + Z_i$

$A_I = - h_{fe} R_B / R_B + Z_i$--------------------12

Application:

It is used as voltage amplifier, among the three basic amplifier configuration CE amplifier most frequently used.

2. Derive the expression for current gain, input impedance and voltage gain of a CC transistor Amplifier.

This circuit is also known as emitter follower amplifier because its voltage gain is close to unity. Hence a change in base voltage appears as an equal change across the load.

Characteristics of CC amplifier:

(1) CC amplifier provide current gain and power gain. but no voltage gain.
(2) It has high input impedance and very low output impedance.

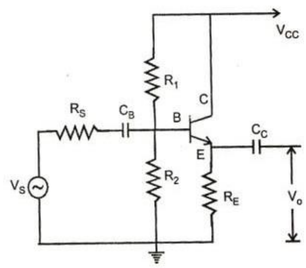


Fig . Common collector amplifier

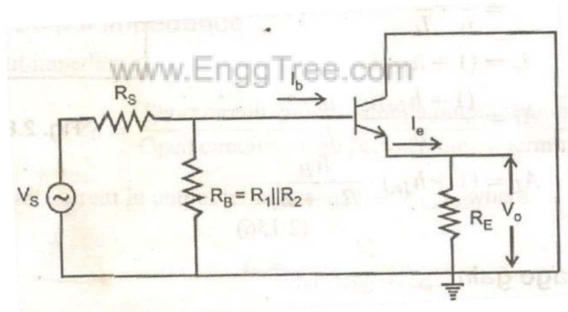


Fig . ac equivalent of CC amplifier

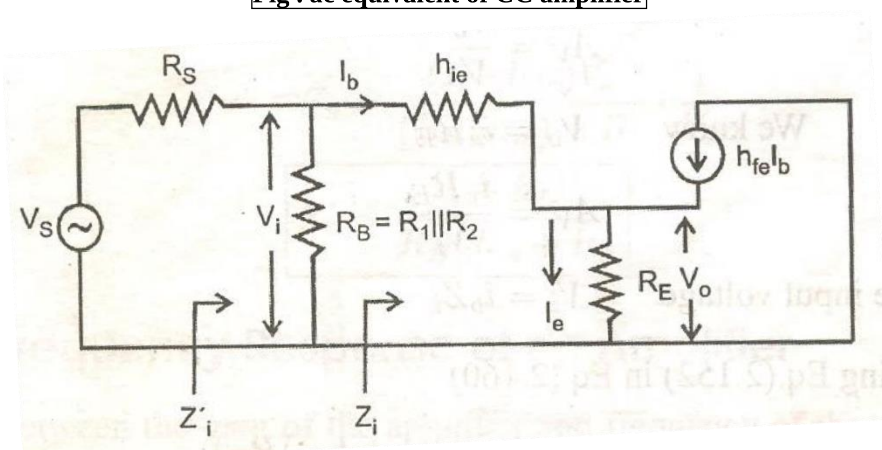


Fig .h-parameter model of a CC amplifier

The input impedance: $Z_i' = Zi \parallel R_B$--------------------1

$Z_i = V_i / i_b$

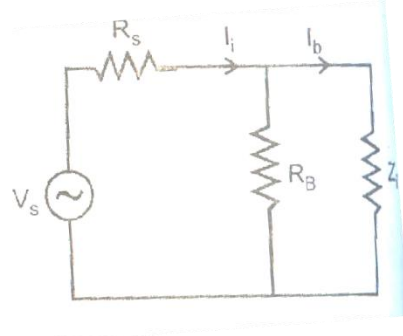
$V_i = h_{ie}\, i_b + I_e\, R_E$-------2 W.K.T $i_e = (1+h_{fe})i_b$

sub eq(2) in eq(1), $V_i = i_b(h_{ie} + (1+h_{fe})\, R_E)$

$Z_i = V_i / i_b = h_{ie} + (1+ h_{fe})\, R_E$ ---------3

$Z_i' = R_B \parallel Zi$

Current gain: The current gain is defined as the ratio of output current to input current



$A_I = i_e / I_i = I_e / i_b \,.\, i_b / I_i$ W.K.T $i_e = (1+h_{fe})i_b$

$A_I = - (1+h_{fe})i_b / i_b \,.\, i_b / I_i$

$A_I = - (1+h_{fe}).R_B / R_B+Z_i.$

Voltage Gain: $A_v = V_0 / V_i$----------------- 4

$Vo = i_e\, R_E$ 5

$A_v = - i_e\, R_E \;/\; V_i$

The input voltage $V_i = i_b\, Z_i$---------------6

Sub eq(3) in eq(6)

$= i_b\, (h_{ie} + (1+h_{fe})\, R_E$ ----------7

$A_V = R_E\, i_e / (h_{ie} + (1+h_{fe})\, R_E)\, i_b$ W.K.T $i_e = (1+h_{fe})i_b$

$= - (1+h_{fe})\, R_E \;/\; h_{ie} + (1+h_{fe})\, R_E$

$= h_{ie} + (1+h_{fe})\, R_E - h_{ie} \;/\; h_{ie} + (1+h_{fe})\, R_E$

$= 1 - \frac{hie}{h_{ie} + (1+h_{fe})\, R_E}$ ---------------------------------8

Since $(1+h_{fe})R_E >> h_{ie}$ and $h_{fe} >> 1$ $A_v = 1-\frac{h_{ie}}{h_{fe}R_E}$--9

Output impedance: $Z_0 = \frac{Shortcircitcurrentthroughoutputterminal}{open\ circuit\ voltage\ between\ output\ terminals}$

Short circuit current through output terminal $i_b = V_s / \; h_{ie} \parallel R_B + R_S$ ------------ 10

Open circuit voltage between output terminals = V_s

$Z_0 = \frac{1+h_{fe}}{R_E \parallel h_{ie}+R_S}$ ------------------------------11

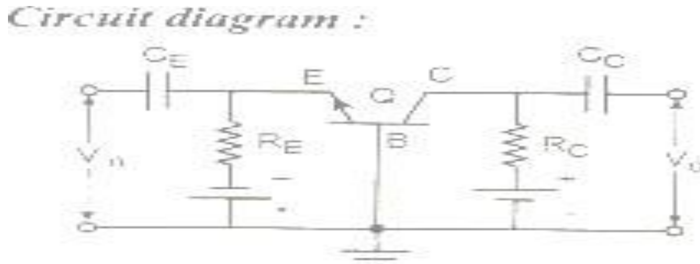
Application:

(1) The voltage gain of emitter follower as unity, thus it is used as buffer amplifier.
(2) It is used as impedance matching network.

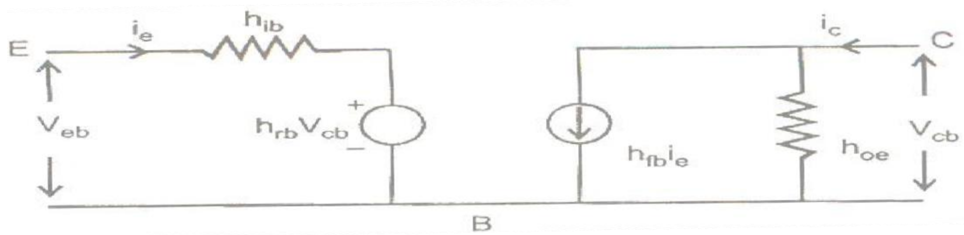
3. **Derive the expression for current gain, input impedance and voltage gain of a CB transistor Amplifier. (May/June2016)**

In this circuit only a fraction of output voltage is feedback to input thus h_{re} is very small. Therefore $h_{rb}V_0$ can be neglected when deriving CB gain and impedance.

Characteristics of CB amplifier:



(1) This CB circuit provides voltage gain and power gain but no current gain.
(2) It has high output impedance and very low input impedance thus it is unsuitable for most voltage amplification.



a. Input impedance: After neglecting $h_{rb}V_0$, The Z_e is given by,

Apply KVL , $V_i = I_eh_{ib} + I_eR_B – I_eR_B = I_eh_{ib} +I_eR_B - I_Eh_{fb}R_B$

$I_C = I_eh_{fb}=I_e [h_{ib} + R_B – h_{fb} R_B]$-------------------1

$Z_e = V_i / I_e = h_{ib} + R_B(1 - h_{fb})$ -------------- 2

The actual impedance of the circuit is given by

$Z_i = Z_e \parallel R_e$------------------------3

b. Output impedance: The output has very less impact on the input hence the output impedance can be taken as $Z_e \cong 1 / h_{ob}$

The actual output impedance is given by, $Z_0 = R_C \parallel Z_C \cong R_C$

R_C is usually much smaller than $1/ h_{ob,}$ soothe circuit impedance is approximately equal to $R_{C.}$

c. Voltage Gain: it is given by $A_v = V_0 / V_i$------------------------------ 4

$V_0 = I_C (R_C \parallel R_L)$ ------------5

$V_i=I_eh_{ib} +I_eR_B - I_Eh_{fb}R_B = I_e[h_{ib} + R_B(1 - h_{fb})]$

$A_V = I_C (R_C \parallel R_L) / I_e[h_{ib} + R_B(1 - h_{fb})]$ --------- 6

$A_V = h_{fb} (R_C \parallel R_L) / h_{ib} + R_B(1 - h_{fb})$ -------------7

d. Current gain: The transfer current gain of the device is given by $h_{fc} = I_C / I_e$---------------- 8

The signal current is divided between R_E and $Z_{e,}$and the collector current divides between R_C and $R_{L ,}$giving a lower value of current gain.

$I_L = I_C R_E / R_E + R_L$

$= h_{fc}I_e R_E / R_E + R_L$ but $I_e=I_S R_B/ R_B + Z_e$

$A_i = I_L / I_S = h_{fc}R_ER_B / (R_B + Z_e)(R_C + R_{:L})$ ---------9

e. Power Gain:

The Power gain is given by $A_{PT} = A_V * h_{fb}$-------------------10

Where A_i is significantly different from h_{fb} $A_p = A_V * A_i$ ---------11

f. Application:

It is used for very high frequency voltage amplifier.

UNIT-IV MULTISTAGE AMPLIFIERS AND DIFFERENTIAL AMPLIFIER

PART-A

BIMOS cascade amplifier, Differential amplifier

1. **What is a differential amplifier?**
   An amplifier, which is designed to give the difference between two input signals, is called the differential amplifier.

2. **What is the function of a differential amplifier?**
   The function of a differential amplifier is to amplify the difference of two signal inputs, i.e.,$V_0 = A_D(V_1 - V_2)$, where A_D is the differential gain.

3. **What is the differential-mode voltage gain of a differential amplifier?**

   It is given by $A_d = \frac{1}{2}(A_1 - A_2)$

4. **What are the ideal values of A_d and A_c with reference to the differential amplifier?**
   Ideally, Ac should be zero and A_d should be large, ideally infinite.

5. **What are advantages of differential amplifier?**
   It has high gain and high CMRR.

6. **List some applications of differential amplifiers?**
   Used in IC applications, AGC circuits and phase inverters.

Common mode and Difference mode analysis

7. **Define differential mode signals of a differential amplifier. (Nov/Dec 2018)**
   The differential mode signal is the difference between two input voltages. i.e.,
   $$V_d = V_1 - V_2$$
   The differential mode input signal is zero when V_1=V_2

8. **When two signals V_1 and V_2 are connected to the two inputs of a difference amplifier, define a difference signal V_d and common-mode signal V_c**
   The difference signal V_d is defined as the difference of the two signal inputs,
   $$\text{i.e., } V_d=V_1-V_2$$
   The common-mode signal V_c is defined as the average of the two signals,
   I.e., $V_c = (V_1+V_2)$ –
9. **What is the common-mode gain A_C in terms of A_1 and A_2?**
   It is given by $A_c = A_1 + A_2$

10. **Define CMRR what its ideal value How to improve it. (Nov/Dec2015), (May/ June2016)(May 2017)**
    The common-mode rejection ratio (CMRR) of a differential amplifier is defined as the ratio of the differential-mode gain to common-mode gain.
    $$\text{CMRR} = \frac{|A_d|}{|A_c|}$$
    Ideal value of is Infinite.
    The improve CMRR the following circuits are used
    i) Current mirror circuit ii) Temperature compensation. iii) Differential amplifier with constant current bias.

11. **Express CMRR in dB.**

    CMRR (dB)=$20\log A_d - 20\log A_c$.

Single tuned amplifiers

12. What is meant by tuned amplifiers? (A/M 2010)

Tuned amplifiers are amplifiers that are designed to reject a certain range of frequencies below a lower cut off frequency ω_L and above a upper cut off frequency ω_H and allows only a narrow band of frequencies.

13. Classify tuned amplifiers.

1. Single tuned amplifier.
2. Double tuned amplifier.
3. Synchronously tuned amplifier.
4. Stagger tuned amplifier.

14. What is the other name for tuned amplifier?

Tuned amplifiers used for amplifying narrow band of frequencies hence it is also known as "narrow band amplifier" or "Band pass amplifier.

15. What is the application of tuned amplifiers?(N/D 2007)

The application of tuned amplifiers to obtain a desired frequency and rejecting all other frequency in
(i). Radio and T .V broadcasting as tuning circuit.
(ii). Wireless communication system.

16. What are the advantages of tuned circuit?

- High selectivity
- Smaller collector supply voltage
- Small power gain.

Neutralization methods

17. What is meant by neutralization? (N/D 2012)

It is the process by which feedback can be cancelled by introducing a current that is equal in magnitude but 180^o out of phase with the feedback signal at the input of the active device. The two signals will cancel and the effect of feedback will be eliminated. This technique is termed as neutralization.

18. What is the need for neutralization (Nov/Dec2015)

In turn RF amplifier at high frequency centered around a radio frequency the inter junction capacitance between base and collector C_{bc} of the transistor becomes dominant i.e. its reactance become low enough to be considered. As reactance of C_{bc} at RF is low enough it provides the feedback path from collector to base. If this feedback is positive the circuit is converted to an unstable one generating its own oscillations and can stop working as an amplifier. In order to prevent oscillations without redacting the stage gain neutralization is used in tuned amplifiers.

19. State the merits of using push-pull configuration. (May 2018) (Apr/May 2018)

- Efficiency is high. (78.5%)
- Figure of merit is high.
- Distortion is less
- Ripple present in the output due to power supply is multiplied.

20. List the disadvantages of push-pull amplifier.

- Two identical transistors are needed.
- Centre taping is required in transformer.
- Transformers used are bulky and expensive.
- If the parameters of the two transistors differ, there will be unequal amplification of the two halves of signal which introduces more distortion.

21. How do you bias class-A operation?

In class A mode of means, the output current flows throughout the entire period of input cycle and the Q-point is chosen at the midpoint of A.C load line and biased.

22. Give two applications of class-C power amplifier.

- Used in radio and TV transmitters.
- Used to amplify the high frequency signals.
- Tuned amplifiers.

23. What is multistage amplifier?

Multistage cascading permits several single-stage amplifiers to be combined into one circuit. Multistage cascading can produce an amplifier with large gain, high input resistance and low output resistance. The small-signal behavior of a multistage amplifier can be modeled by cascading an appropriate number of small-signal two-port amplifier models.

24. A multistage amplifier employs five stages each of which has a power gain of 30. What is the total gain of the amplifier in dB. (Nov/Dec 2018)

Given that,

The power gain of each stage in a five-stage amplifier is,

$A_{Vn} = 30$, n = 1 to 5

Total gain, A_V = ?

The overall gain, A_V of an n-stage amplifier is given as,

$A_V = A_{V1} \text{ X } A_{V2} \text{ X } A_{V3} \text{ X } \ldots\ldots A_{Vn}$

Here, n = 5

$A_V = A_{V1} \text{ X } A_{V2} \text{ X } A_{V3} \text{ X } A_{V4} \text{ X } A_{V5}$

$= 30 \text{ X } 30 \text{ X } 30 \text{ X } 30 \text{ X } 30$

$A_V = 243 \text{ X } 10^5$

Total gain, $A_V = 243 \text{ X } 10^5$

$$\boxed{A_V = 147.71 \text{ dB}}$$

25. CMRR of an amplifier is 100dB, calculate common mode gain if the differential gain is 1000(Nov/Dec 2016)

CMRR=A_d/A_C, 100=1000/A_c, A_c=10

26. Define conversion efficiency of power amplifier? (Nov/Dec 2016)

It is a measure of an active device in converting the d.c power of the supply into the ac power delivered to load. It is also referred theoretical efficiency or collector circuit efficiency

- Mathematically, collector circuit efficiency,

$$\eta_c = \frac{\text{a.c.power delivered to the load}}{\text{power supplied by the d.c.source to output circuit}}$$

27. A tuned circuit has a resonant frequency of 1600 KHz and a bandwidth of 10 KHz. What is the value of its Q factor? (May 2017)

$$Q_{\text{factor}} = \frac{\text{resonant frequency}}{\text{bandwidth}} = \frac{1600}{10} = 160$$

28. What is thermal runaway? (Nov/Dec 2017)

Thermal runaway occurs in situations where an increase in temperature changes the conditions in a way that causes a further increase in temperature, often leading to a destructive result. It is a kind of uncontrolled positive feedback.

29. Compare the characteristics of CE, CB, CC amplifiers (May/June 2016) (Nov/Dec 2017)
30.

S.No	Common Emitter Amplifier	Common Base Amplifier	Common Collector Amplifier
1	In this case emitter is common to both input and output	In this case base is common to both input and output	In this case collector is common to both input and output
2	180^0 phase shift occurs	No phase shift occurs	No phase shift occurs
3	Input impedance: Low	Very low	Very high
4	Output impedance: High	Very high	Low

31. A multistage amplifier employs five stages each of which has a power gain of 30. What is the total gain of the amplifier in dB? (Nov/Dec 2017)

Solution:

Absolute gain of each stage = 30   No. of stages = 5
Power gain of one stage in dB = 10 log 10 30 = 14.77
∴ Total power gain = 5 ×14.77 = 73.85 dB

32. What is cross over distortion? (Apr/May 2018)

Crossover distortion is the term given to a type of **distortion** that occurs in push-pull class AB or class B amplifiers. It happens during the time that one side of the output stage shuts off, and the other turns **on**.

33. Determine the input impedance of a differential amplifier (emitter coupled) with R_B=3.9 KΩ and Z_B=2.4 KΩ. (April/May 2019)

$$Z_i = R_B \| Z_B$$

$$Z_i = \frac{R_B \times Z_B}{R_B + Z_B}$$

$$Z_i = \frac{3.9 \times 10^3 \times 2.4 \times 10^3}{3.9 \times 10^3 + 2.4 \times 10^3}$$

The input impedance of a differential amplifier (emitter coupled), $Z_i = 1.49\ \Omega$

34. A single tuned amplifier provides a band width of 10KHz at a frequency of 1MHz. Find the circuit Q. (April/May 2019)

$$f_O = BW \times Q_O$$

$$Q_O = \frac{f_O}{BW}$$

$$Q_O = \frac{1 \times 10^6}{10 \times 10^3}$$

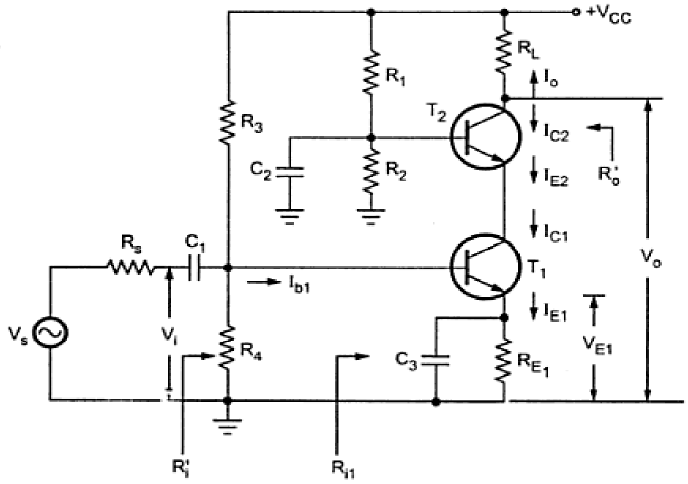
$$Q_O = 100$$

PART-B

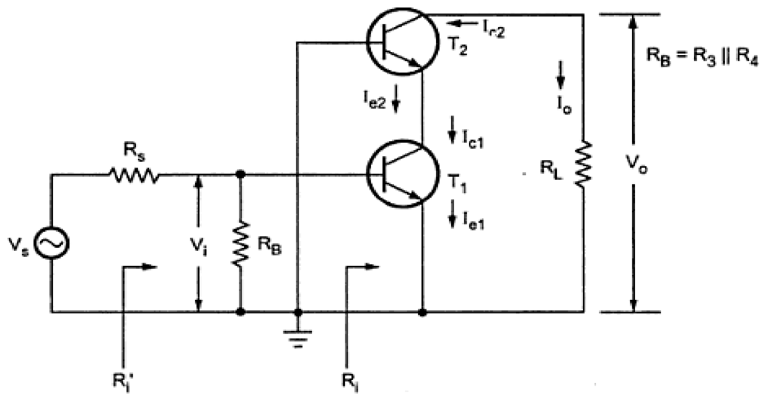
BIMOS cascade amplifier, Differential amplifier

1. Explain the operation of cascade amplifier.

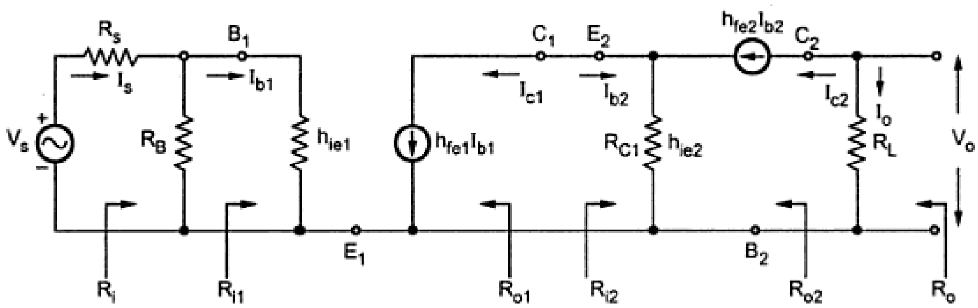
- The cascade amplifier consists of a common emitter amplifier stage in series with a common base amplifier stage.
- It solves the low impedance problem of a common base circuit.
- It gives the high input impedance of a CE amplifier as well as good voltage gain and high frequency response of CB circuit.
- For DC bias $I_{C1} = I_{E1}$, $I_{E2} = I_{C1}$



- Ac equivalent circuit for cascade amplifier is drawn by shorting dc supply and capacitors.



- A simplified h parameter equivalent circuits for cascade amplifier is drawn by replacing transistor with their equivalents



Analysis of second stage (CB)

a) Current gain (A_{i2})

$$A_{i2} = \frac{h_{fe}}{1+h_{fe}}$$

b) Input resistance (R_{i2})

$$R_{i2} = \frac{h_{ie}}{1+h_{fe}}$$

c) Voltage gain (A_{v2})

$$A_{v2} = \frac{A_{i2} R_{L2}}{R_{i2}}$$

Analysis of first stage (CE)

a) Current gain (A_{i1})

$$A_{i1} = -hfe$$

b) Input resistance (R_{i1})

$$R_{i1} = hie$$

c) Voltage gain (A_{v1})

$$A_{v1} = \frac{A_{i1} R_{L1}}{R_{i1}}$$

2. BIMOS cascade amplifier (or coupling amplifier):

- ❖ To get faithful amplification, amplifier should have desired voltage gain, current gain and it should match its input impedance with the connected source impedance. Similarly, output impedance must match with the load impedance.
- ❖ Normally, these requirements of the amplifier cannot be obtained in a single stage amplifier, which is due to the limitation of the parameters of transistor or FET or whatever device used.
- ❖ Under these situations, more than one amplifier stages are cascaded such that input and output stages provide impedance matching requirements with some amplification and remaining middle stages provide most of the amplification.

Therefore, for making cascading following reasons,

- ❖ The amplification of a single stage amplifier is not sufficient.
- ❖ When input and output impedance is not of the correct magnitude, for a particular application two or more amplifier stages are connected in cascaded fashion or coupling. This is known as multistage amplifier.

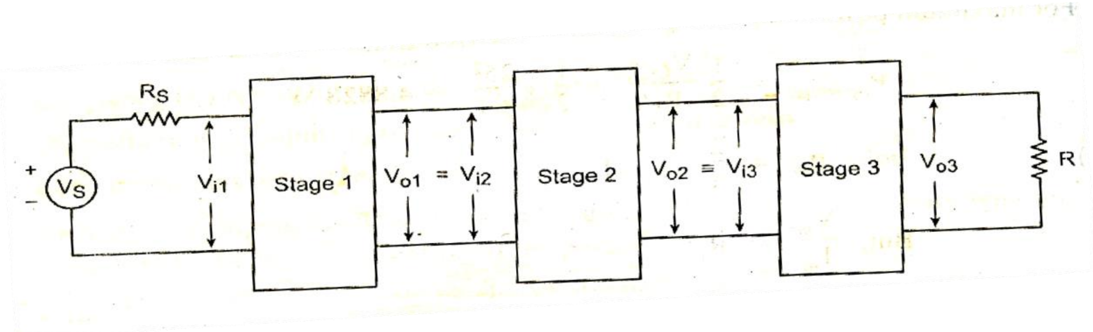


Figure: Block diagram of cascade amplifier

From the above figure, V_{i1}, V_{i2}, V_{i3} the input of first, second and third stages and V_{o1}, V_{o2}, V_{o3} are the output of the three stages. Therefore, $\frac{V_{o3}}{V_{i1}}$ is the overall voltage gain of 3 stage amplifier which is given as follows:

$$A_v = \frac{V_{o3}}{V_{i1}} \qquad \ldots\ldots\ldots\ldots\ldots (1)$$

$$= \frac{V_{o3}}{V_{i3}} \cdot \frac{V_{i3}}{V_{i2}} \cdot \frac{V_{i2}}{V_{i1}} \qquad \ldots\ldots\ldots\ldots\ldots (2)$$

From the figure, we know that,

$V_{o1} = V_{i2}$; $V_{o2} = V_{i3}$; put this into the above equation, we get

$$A_v = \frac{V_{o3}}{V_{i3}} \cdot \frac{V_{o2}}{V_{i2}} \cdot \frac{V_{o1}}{V_{i1}} \qquad \ldots\ldots\ldots\ldots\ldots\ldots (3)$$

Already we know that,

Voltage gain (A) $= \frac{Output\ voltage}{Input\ voltage} = \frac{Vo}{V_i}$

$$A_v = A_{v3} \cdot A_{v2} \cdot A_{v1} \qquad \ldots\ldots\ldots\ldots (4)$$

Therefore, the voltage gain of multistage amplifier is the product of individual gains of the each stage. Then the multistage amplifier is shown below.

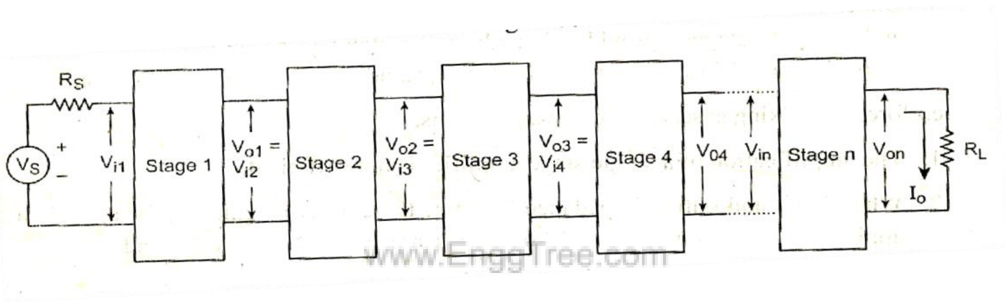


Figure: Multistage amplifier

Voltage gain: The resultant voltage gain of the multistage amplifier is the product of the voltage gains of the various stages or individual stages.

(i.e.,) $A_v == A_{v1} \cdot A_{v2} \cdot A_{v3} \cdot A_{v4} \cdot \ldots \ldots \cdot A_{vn}$.................... (5)

= Then, Voltage gain of n^{th} stage is as follows:

$$A_{v1} = \frac{A_{in} R_{ln}}{R_{in}} \ldots\ldots\ldots\ldots (6)$$

Where, R_{ln} = Effective load resistance of n^{th} stage.

R_{in}= Input resistance / impedance of 1^{st} stage.

Selection of cascading amplifier configuration:

From the above discussion, the multistage amplifier is divided into three parts:

i) Input stage
ii) Middle stage and
iii) Output stage.

- In the above, the input stage must be designed with input impedance matches with the source impedance.
- Similarly, the output stage designed must be the output impedance matches with the load impedance.
- Then, middle stage is designed with our desired voltage and current gain.

Anyhow, to select the cascading configuration, the following considerations are important since we normally use these three configurations.

Common mode and Difference mode analysis

3. Draw the circuit diagram and explain the working of a differential amplifier using FET. Derive the expression for differential mode gain and common mode gain.(May 2017)

- Normally, analysis in amplifier depends on both AC and DC analysis.
- In the above two, the d.c signals determines the operating values for the transistors and used as biasing.
- Similarly, a.c signals are used as input signals, which determine the output of the differential amplifier.
- The dual input, balanced output differential amplifier is also called **Symmetrical Differential Amplifier.**

❖ **DC ANALYSIS:**

- DC analysis means using D.c voltage as biasing voltage and keeping it constant (to obtain suitable operating point).

❖ **AC ANALYSIS:**

- For performing AC analysis, we must apply AC input signals as an input. So, we can calculate the following:
  A. Differential mode gain (A_d).
  B. Common mode gain (A_c).
  C. Input resistance (R_i).
  D. Output resistance (R_o).
  The above can be obtained by using h-parameters.

A. Differential gain (A_d)

- To obtain the Differential mode gain, the two input signals must be different from each other.
- Here, we take the two a.c input signals as equal in magnitude but having 180° phase shift between them.
- Then, the magnitude of each a.c input voltage V_{S1} and $V_{S2}$is $\frac{V_S}{2}$.
- For the a.c purposes, emitter terminal can be grounded which is shown in figure below with small signal analysis.

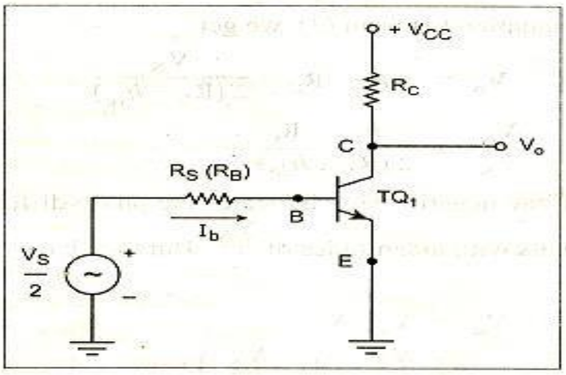
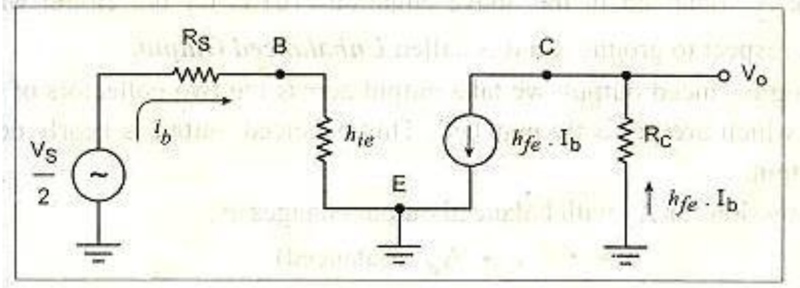


Figure (1): AC Equivalent for differential operation (half circuit concept)

- The circuit which can be analyzed by considering only one transistor is called Half circuit concept of analysis.



Figure(2): Approximate hybrid model

- For obtaining the differential mode gain (A_d) from the above hybrid model, we have to apply the Kirchhoff's voltage law in input side,

$$\frac{V_S}{2} = i_b R_S + i_b h_{ie} \quad \text{........(1)}$$

$$\frac{V_S}{2} = i_b (R_S + h_{ie}) \quad \text{........(2)}$$

$$i_b = \frac{V_S}{2(R_S + h_{ie})} \quad \text{........(3)}$$

- Similarly, applying the Kirchhoff's voltage law to output loop, we get

$$V_o = - I_b h_{fe} \cdot R_C \text{........................} (4)$$

- Put the value of I_b in equation (4) from (3), we get,

$$V_o = \frac{-h_{fe} V_S R_C}{2(R_S + h_{ie})} \ldots\ldots..(5)$$

- Then, $\frac{V_o}{V_S} = \frac{-h_{Fe} \cdot R_C}{2(R_S + h_{ie})}$ ....(6)
- Negative sign indicates that 180^0 phase difference between input and output. If the input signals are equal and are out of phase by 180^0, we get
- Differential mode signal $V_d = V_1 - V_2 = (\frac{V_S}{2}) - (-\frac{V_S}{2}) = V_S$ .....(7)

  Where, V_S is differential input voltage.
- Differential voltage gain $A_d = \frac{V_o}{V_S}$

$$A_d = \frac{h_{fe} R_C}{2(R_S + h_{ie})} \ldots\ldots\ldots.(8)$$

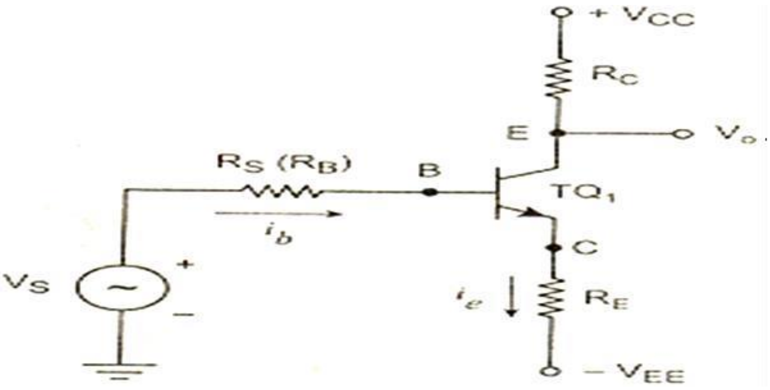
- When the output of differential amplifier is measured with reference to ground, it is called unbalanced output.
- The output across the collectors of Q_1 and Q_2 to be perfectly matched then A_d for balanced output is twice than that of A_d for unbalanced output. Therefore

$$A_d = \frac{h_{fe} R_C}{(R_S + h_{ie})} \ldots\ldots\ldots\ldots\ldots\ldots.(9)$$

B. Common mode gain (A_C)

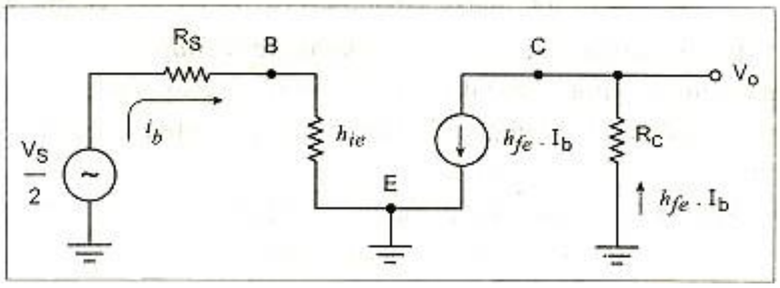
- In common mode, the both transistor's input magnitude and phases are also inphase with each other.
- Let us assume that input signals are having the same magnitude V_S and are in same phase.
- Common mode voltage $V_C = \frac{V_1 + V_2}{2} = \frac{V_S + V_S}{2} = V_S$ ....(10)
- If suppose, the output is expressed as, $V_o = A_C \cdot V_S$ ......(11)
- Common mode gain $A_C = \frac{V_o}{V_S}$ ....(12)
- In this mode, both the emitter current $I_{e1} = I_{e2} = I_e$ of TQ_1, TQ_2 flows through R_E in the same direction, with same magnitude.

- Hence, the total current flowing through R_E is nearly $2I_e$ …..(13)



Figure(1): A.C. Equivalent Circuit for Common Mode Configuration

- Then the approximate hybrid model for the above circuit can be obtained and is used to obtain the A_d.



Figure(2): Approximate Hybrid model

- As the current through R_E is $2I_e$, for simplicity of derivation, we have to assume the I_e and effective emitter resistance as $2R_E$.

- Current through R_C = Load current I_L
- Effective emitter = 2 R_E
- Current through emitter resistance = $I_L + I_b$
- Current through $h_{oe} = (I_L - h_{fe} . I_b)$
- Now, applying Kirchhoff's voltage law to input side,

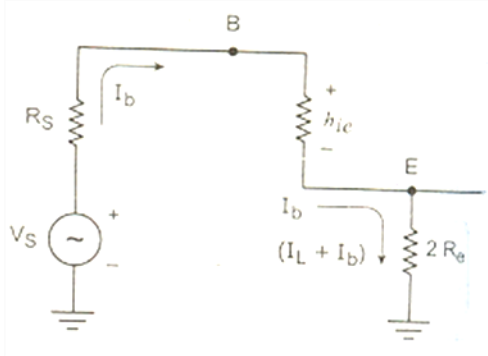


Figure (3): Input side

$$-I_b R_S + I_b h_{ie} + 2R_E(I_L + I_b) = -V_S \quad ……(14)$$

$$I_b R_S - I_b h_{ie} - 2R_E(I_L + I_b) = V_S \quad ....(15)$$

While, $V_o = -I_L . R_C$ ....(15a)

- Negative sign is due to the assumed direction of current. Similarly apply KVL to output side.

$$\frac{-(I_L - h_{Fe} I_b)}{h_{oe}} - 2R_E(I_L + I_b) - I_L R_C = 0…. (16)$$

$$\frac{-I_L}{h_{oe}} + \frac{h_{Fe} I_b}{h_{oe}} - 2I_L R_E - 2I_b R_E - I_L R_C = 0…(17)$$

$$I_b\left[\frac{h_{Fe}}{h_{oe}} - 2R_E\right] = I_L\left[\frac{1}{h_{oe}} + 2R_E + R_C\right] \quad ……… (18)$$

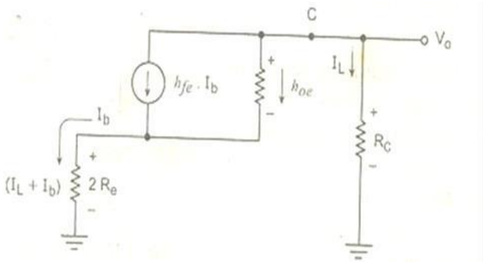


Figure (4): Output side

- Multiplying both sides by h_{oe}, then

$$I_b[h_{fe} - 2R_Eh_{oe}] = I_L[\ 1 + h_{oe}(2R_E + R_C)] \ldots\ldots\ldots\ldots\ldots(19)$$

$$\frac{I_L}{I_b} = \frac{[h_{fe} - 2R_Eh_{oe}]}{[\ 1 + h_{oe}(2R_E + R_C)]} \ldots\ldots\ldots(20)$$

$$I_b = \frac{I_L[\ 1+h_{oe}(2R_E+R_C)]}{[h_{Fe}-2R_Eh_{oe}]} \quad \ldots\ldots\ldots\ldots(21)$$

- Putting this I_b in equation (15),

$$V_S = \frac{I_L[1 + h_{oe}(2R_E + R_C)][R_S + h_{ie} + 2R_E] + 2R_E}{[h_{fe} - 2R_E h_{oe}]}$$

$$\frac{V_S}{I_L} = \frac{[1 + h_{oe}(2R_E + R_C)][R_S + h_{ie} + 2R_E] + 2R_E}{[h_{fe} - 2R_E h_{oe}]} \ldots(22)$$

- Then, find LCM and adjusting the terms,

$$\frac{V_S}{I_L} = \frac{2R_E(1 + h_{fe}) + R_S(1 + 2R_Eh_{oe}) + h_{ie}(1 + 2R_Eh_{oe}) + h_{oe}R_C(2R_E + R_S + h_{oe})}{[h_{fe} - 2R_E h_{oe}]}$$

$$\frac{V_S}{I_L} = \frac{2R_E(1 + h_{fe}) + (R_S + h_{ie})(1 + 2R_Eh_{oe}) + h_{oe}R_C(2R_E + R_S + h_{oe})}{[h_{fe} - 2R_E h_{oe}]} \ldots(23)$$

Actually $h_{oe}R_C \ll 1$. Neglecting the terms,

$$\frac{V_S}{I_L} = \frac{2R_E(1 + h_{fe}) + (R_S + h_{ie})(1 + 2R_Eh_{oe})}{[h_{fe} - 2R_E h_{oe}]} \ldots(24)$$

$$I_L = \frac{V_S.[h_{fe} - 2R_Eh_{oe}]}{2R_E(1 + h_{fe}) + (R_S + h_{ie})(1 + 2R_Eh_{oe})} \ldots(25)$$

Putting this I_L in equation (15a),

$$V_o = -\ I_L\ .\ R_C$$

$$V_o = \frac{-V_S.[h_{Fe}-2R_Eh_{oe}]R_C}{2R_E(1+h_{Fe})+(R_S+\ h_{ie})(1+2R_Eh_{oe})} \ldots\ldots(26)$$

Hence the common mode gain can be written as,

$$A_C = \frac{V_o}{V_S} = \frac{[2R_Eh_{oe} - h_{fe}]R_C}{2R_E(1 + h_{fe}) + (R_S + h_{ie})(1 + 2R_E h_{oe})} \ldots\ldots(27)$$

In practice, h_{oe} is neglected, because the expression for A_C can be further modified as,

$$A_C = \frac{-h_{fe}R_C}{R_S + h_{ie} + 2R_E(1 + h_{fe})} \ldots(28)$$

The above expression is same whether the output is balanced or unbalanced.

COMMON MODE REJECTION RATIO (CMRR):

$$CMRR = \left|\frac{A_d}{A_C}\right|$$

From equation (8) and (28),

$$CMRR = \left|\frac{\frac{h_{Fe}R_C}{2(R_S+h_{ie})}}{\frac{h_{Fe}R_C}{(R_S+h_{ie}+2R_E(1+h_{Fe})}}\right| \ldots\ldots(29)$$

$$\text{CMRR} = \left|\frac{(R_S + h_{ie} + 2R_E(1 + h_{fe})}{2(R_S + h_{ie})}\right| \quad \ldots (30)$$

This is CMRR for dual input balanced output differential amplifier circuit.

For balanced case,

$$\text{CMRR} = \left|\frac{(R_S + h_{ie} + 2R_E(1 + h_{fe})}{(R_S + h_{ie})}\right|$$

For unbalanced case,

$$\text{CMRR} = \left|\frac{(R_S + h_{ie} + 2R_E(1 + h_{fe})}{2(R_S + h_{ie})}\right|$$

C. Input Impedance (R_i):

R_i is defined as the equivalent resistance existing between any one of the input and the ground when other input terminal is grounded.

$$R_i = \frac{V_S}{I_b}$$

Put the V_S and I_b from the above discussion, $R_i = 2(R_S + h_{ie})$.

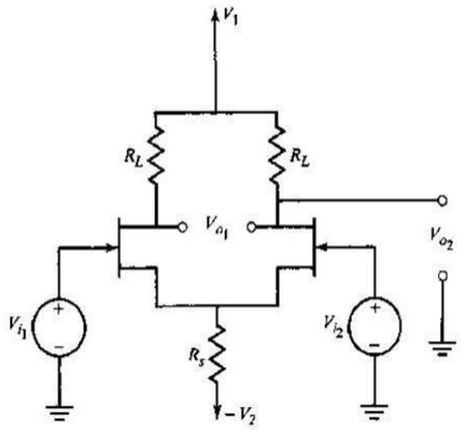
For one transistor and input pair, the resistance is $R_S + h_{ie}$.

Hence for dual input circuit, the total input resistance is $2(R_S + h_{ie})$, as the 2 circuits are perfectly matched.
This input resistance is not dependent on whether output is balanced or unbalanced.

D) OUTPUT IMPEDANCE R_O:

- It is defined as the equivalent resistance between one of the output terminals with respect to ground.
- The resistance between output terminal with respect to ground is R_C.

$R_O = R_C$



Changes to be made for FET is

BJT	FET
Rc	Rd

$re = \frac{1}{g_m}$

$$A_d = \frac{V0}{V_{in}} = \frac{R_d}{V_{g_{md}}} = g_{md} R_d$$

4. Draw a differential amplifier and its ac equivalent circuit. *(OR)* **Explain the operation of basic emitter coupled differential amplifier** *(or)* **Explain the function of differential amplifier with neat circuit. (A/M 2010) (M/J 2012)** *(OR)* **Explain the common mode and differential mode operation of the differential amplifier (May/June2016 Nov/Dec-2017, May-2018)** *(OR)*
Explain the working of a single ended input differential amplifier. (Nov/Dec 2018)

❖ **DIFFERENTIAL AMPLIFIER BASIC BLOCK DIAGRAM:**

- The differential amplifier amplifies the difference between two applied input signals V_{in1} and V_{in2} (voltage signals). Hence, it is called as **Difference amplifier.**

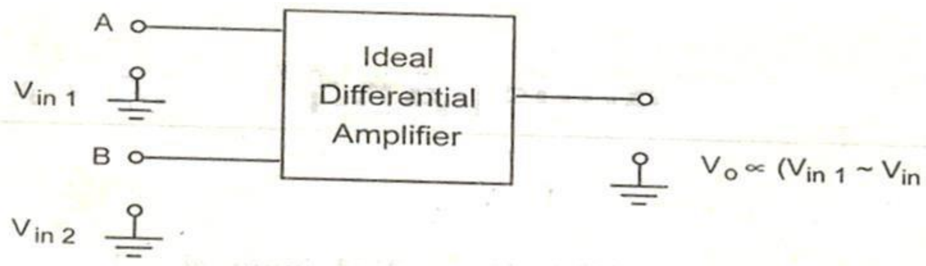


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Fig: block diagram of differential amplifier

- In an ideal amplifier, the output voltage V_o is proportional to the difference between the two input signals. Therefore we can write,

$$V_o \,\alpha\, (V_{in1} - V_{in2}) \text{ ....(1)}$$

❖ **DIFFERENTIAL GAIN A_d:**

- From the above equation, we can write the differential gain A_d is [Generally gain is nothing but the output parameter (may be voltage, current, etc.) to input parameter].
- Therefore, $V_o = A_d (V_{in1} – V_{in2})$............................ (2)

  Where A_d = Differential gain constant
- This A_d is thegain with which differential amplifier amplifies the difference between two input signal is called **Differential gain.**
- The difference between the two inputs (V_{in1}˜ V_{in2}) is generally called difference voltage and denoted as V_d.
- output foreThere voltage is $V_o = A_d . V_d$.............................(3)
- Therefore the differential gain can be expressed as,

$$A_d = \frac{V_o}{V_d} \text{ ....(4)}$$

❖ **COMMON MODE GAIN A_c :** If we apply two input voltages which are equal in all the respect to the differential amplifier i.e., $V_1 = V_2$ then, ideally the output voltage V_o is (V_1˜ V_2) .A_d , must be zero.

- In this mode the applied input signals, phase and frequency must be in same.

- But the output voltage of the practical differential amplifier not only depends on the difference voltage but also depends on the average common level of the two inputs.
- Such an average level of the two input signal is called **common mode signal** which is denoted as V_c.

$$V_c = \frac{V_1 + V_2}{2} \quad \ldots\ldots\ldots\ldots (5)$$

- In practical, the differential amplifier produces the output voltage proportional to each common mode signal. The gain which it amplifies the common mode signal to produce the output is called common mode gain of the differential amplifier denoted as A_c.

$$A_c = \frac{V_o}{V_c} \quad \ldots\ldots\ldots\ldots (6)$$

- So that total output of any differential amplifier can be expressed as,

$$V_o = A_d\,.V_d + A_c\,.V_c \quad \ldots\ldots\ldots\ldots (7)$$

❖ COMMON MODE REJECTION RATIO:

- In differential amplifier, if both transistors input the same, then that differential amplifier is called as **common mode differential amplifier.**
- In common mode operation, the output is zero.
- But due to many disturbance in signals, noise signals appear as a common input signal to both the input terminals of the differential amplifier.
- Such a common signal should be rejected by the differential amplifier(CMRR).
- Thus, the ability of a differential amplifier to reject a common mode signal is expressed by a ratio called **common mode rejection ratio.**
- CMRR is defined as the ratio of the differential mode gain (A_d) to common mode voltage gain (A_c).

$$CMRR = \frac{|Ad|}{|A_c|} = \rho \ldots\ldots\ldots\ldots (8)$$

- In ideal case the CMRR is infinite, because the common mode gain is nearly or exactly zero. But in practical, it is not infinite.
- But ρ is very large one, since A_d is very large and A_c is very small. The CMRR can be expressed in dB also.

$$\text{CMRR in dB} = 20 \log \frac{|Ad|}{|A_c|} \text{ dB} \ldots\ldots\ldots\ldots (9)$$

- The total output voltage is,

$$V_o = A_d\,.V_d + A_c\,.V_c \quad \ldots\ldots\ldots\ldots (10)$$

Where, V_o = Total output voltage of differential amplifier,

A_d = Differential mode gain of differential amplifier,

A_c = Common mode gain of differential amplifier,

V_d = Differential mode voltage.

- From equation (10), V_o can be written as,

$$V_o = A_d .V_d[1+\frac{Ac .V_c}{Ad . V_d}] .... (11)$$

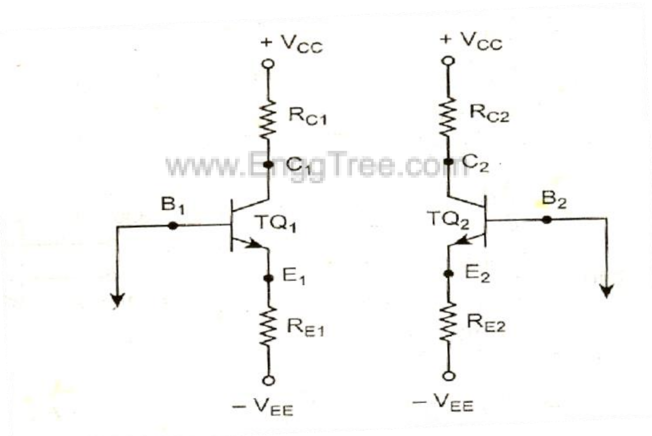
$$V_o = A_d .V_d[1+\frac{1}{\frac{A_d}{A_c}} .\frac{V_c}{V_d}] ... .(12)$$

$$V_o = A_d .V_d[1+\frac{1}{CMRR} .\frac{V_c}{V_d}]........................ (13)$$

- Therefore, from the above equation, the CMRR is practically very large, though both V_c and V_c components are present.
- The output is proportional to the difference in signal only. Then the common mode component is greatly rejected.

❖ EMITTER COUPLED DIFFERENTIAL AMPLIFIER:

- The transistorized differential amplifier is an emitter and emitter follower circuit. So this is called as Emitter coupled differential amplifier.



Figure(1): Emitter biased circuit

- Figure(1) shows the emitter coupled biased circuit. The transistor TQ_1 and TQ_2used in the figure are identical in characteristics and also having exactly matched characteristics.
- Then the two collector resistances R_{C1} and R_{C2} are equal while the two emitter resistances R_{E1} and R_{E2} are also equal.

Therefore $R_{C1} = R_{C2}$ and $R_{E1}= R_{E2}$

- In this the magnitude of V_{CC} and $-V_{EE}$ are also same. Therefore the differential amplifier can be obtained by using such two emitter biased circuits.
- This emitter biased circuit can be obtained by connecting the E_1 of TQ_1 with E_2 of TQ_2.
- Because of this connection the R_{E1} is parallel with R_{E2}.

- The applied input V_{s1} is connected with base of TQ_1 and V_{s2} input is connected with the base of TQ_2.
- Both input voltages in Base is with respect to ground. Then its balanced output is taken in between the respective collector terminals of both transistors (TQ_1 and TQ_2).
- This amplifier is called Emitter coupled Differential Amplifier. In this circuit, the two collector resistanceR_C used are also same.
- Then the dual input differential balanced output differential amplifier is shown below. Because, none of the output terminal is grounded, the output is taken between two output terminals.
- So it is called as Balanced Differential Amplifier and it is shown in figure (2).

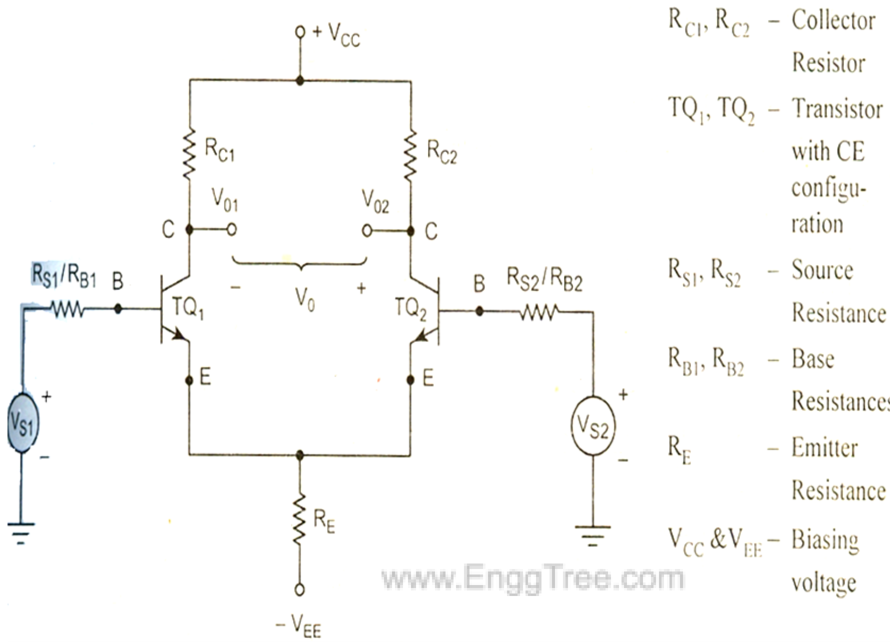


Figure (2): Balanced differential amplifier

- For studying the operation of differential amplifier, the following modes are used. (i) Differential mode, and (ii) Common mode.

i) Differential mode operation:

- In this mode, both inputs are different in either magnitude or phase like 180° phase. This opposite phase can be obtained from the Center tap Transformer.
- That is assume that the sine wave on the base of TQ_1 is positive going while on the base of TQ_2 is negative going.
- With a positive going signal on the base of TQ_1, if amplified, a negative going signal develops and appears on the collector of TQ_1.
- Due to positive going signal, current through R_E also decrease and hence a positive going current wave is developed across R_E.

- Due to negative going signal on the base of TQ_2 an amplified positive going signal develops on the collector of TQ_2 and anegative going signal develops across R_E, because of emitter follower action of TQ_2.
- So. The signal voltage across R_E due to effect of TQ_1 and TQ_2 are equal in magnitude and 180^o out of phase due to method pair of transistors.
- Hence these two signals cancel each other and there is no signal across the emitter resistance.
- Hence there is no AC signal current flowing through the emitter resistance. Hence R_E in this case does not introduce negative feedback.
- While V_o is the output taken across collector of TQ_1 and collector ofTQ_2, the two outputs on collector C_1 and C_2 are equal in magnitude but opposite in polarity.
- And V_o is the difference between these two signals. Hence, the different output V_o is twice as large as the signal voltage from collector to ground.

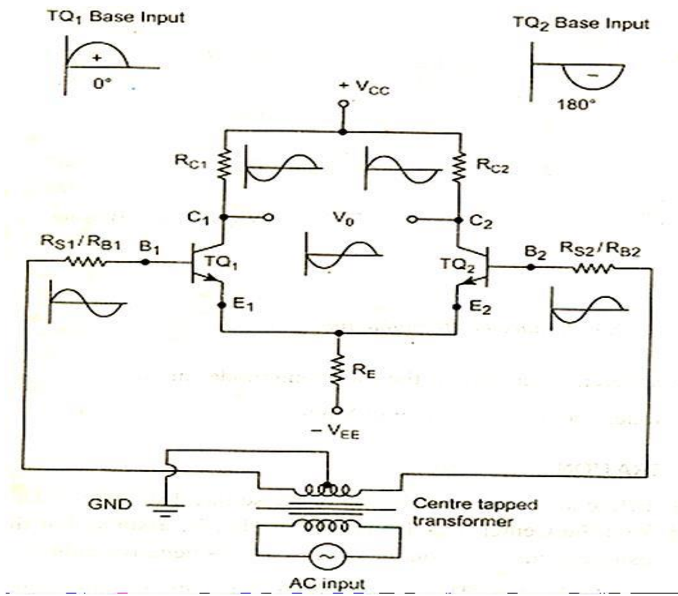


Figure (3): Differential mode

COMMON MODE OPERATION:

- In common mode the signals applied to the base of the both transistor TQ_1 and TQ_2 are in same phase, frequency and also in magnitude.

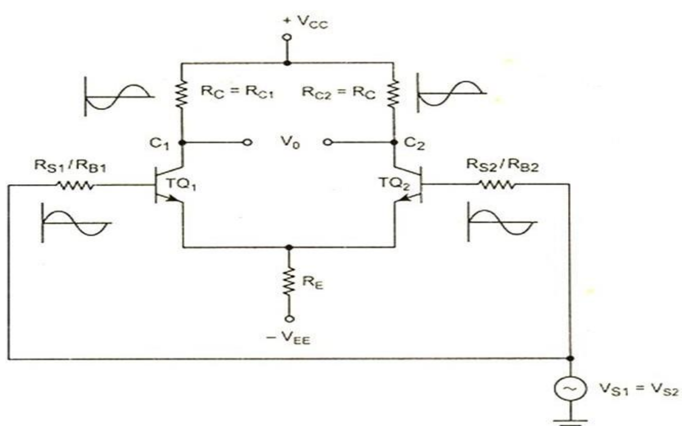


Figure (4): common mode

- In phase signal voltages at the bases of TQ_1 and TQ_2 causes in phase signal voltages to appear across R_E which add together.
- Hence R_E causes a signal current and provides negative feedback.
- This feedback reduces the common mode gain of differential amplifier.

5. **Explain the analysis of Differential amplifier. With neat sketch explain the BJT differential amplifier with active load and derive for A_d, A_c, and CMRR How CMRR improved (Nov/Dec 2015)(Nov/Dec 2016,May-2018) (OR)**
   Deduce the expression for Emitter currents in a differential amplifier under large signal operation. (April/May 2019)

- Normally, analysis in amplifier depends on both AC and DC analysis.
- In the above two, the d.c signals determines the operating values for the transistors and used as biasing.
- Similarly, a.c signals are used as input signals, which determine the output of the differential amplifier.
- The dual input, balanced output differential amplifier is also called **Symmetrical Differential Amplifier.**

❖ **DC ANALYSIS:**

- DC analysis means using D.c voltage as biasing voltage and keeping it constant (to obtain suitable operating point).
- For obtaining DC analysis, we must obtain operating point values i.e., I_{CQ} and V_{CQ} for the transistors used.
- In DC analysis, the supply voltage d.c is taken as biasing voltage and the applied input a.c signals of both V_{s1} and V_{s2} are to be zero.

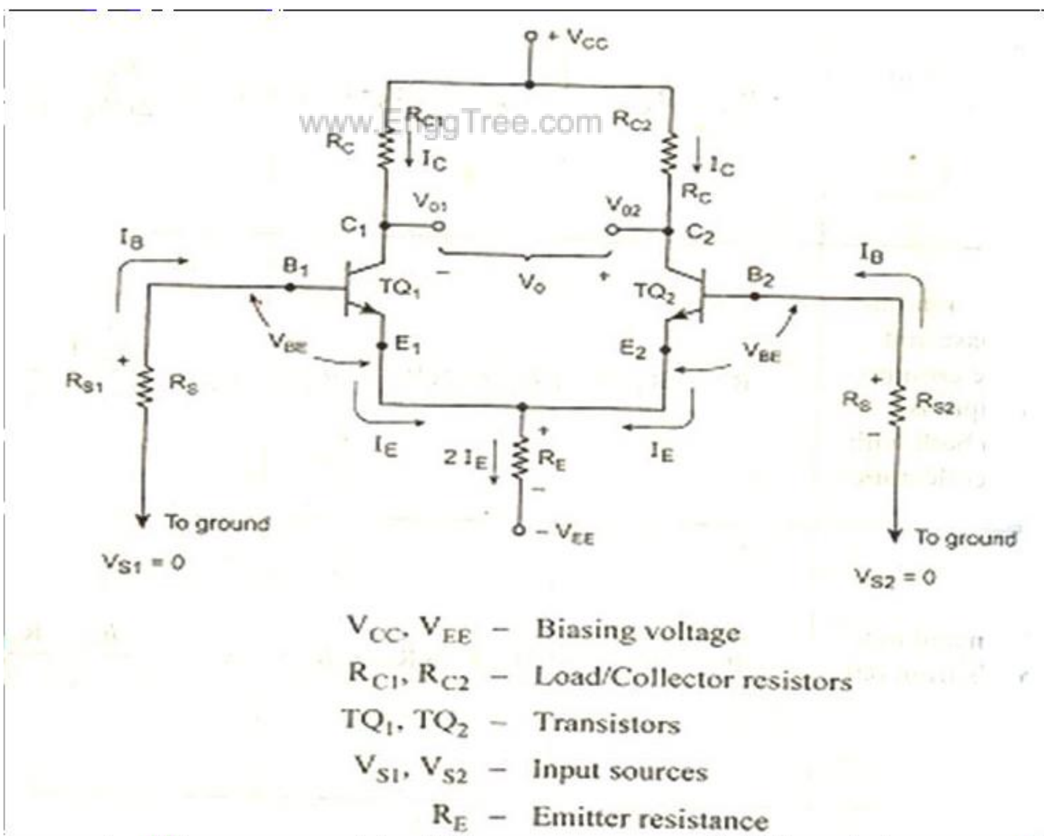


Figure (1): DC Equivalent circuit

To obtain DC analysis following assumptions are to be taken:

1) Assuming $R_{S1} = R_{S2}$ (source resistances of both sides) and is simply denoted by R_S.
2) The transistor used TQ_1 and TQ_2 both are matched in their ideal identical characteristics.
3) Emitter resistances connected in both R_{E1} and R_{E2} must be the same.

   i.e., $R_{E1} = R_{E2} = R_E$

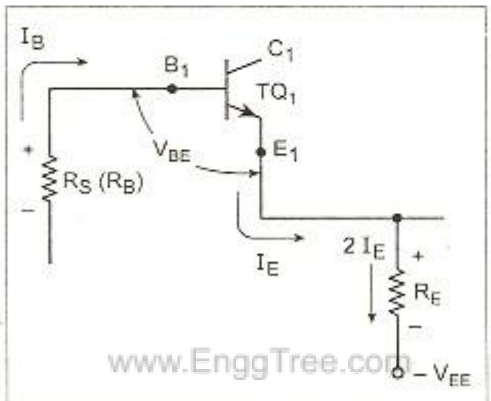
$$\text{Hence} \quad R_E = R_{E1} \| R_{E2} = \frac{R_{E1} \cdot R_{E2}}{[R_{E1}+R_{E2}]}$$

The collector resistances of both transistors also must be in same value.

i.e., $R_{C1} = R_{C2} = R_C$

The magnitude of $|V_{CC}| = |V_{EE}|$ are measured with respect to ground.

- Because of the above identical characteristics of both transistors, there is no necessity for finding out the operating point of each transistors.
- So, simply finding out the operating point to one is enough (I_{CQ} and V_{CEQ}).
- For finding out the I_{CQ} and $V_{CE,}$ the DC analysis diagram is needed.



Figure(2): DC analysis diagram

$$-I_B R_S - V_{BE} - 2I_E R_E = -V_{EE} \quad \ldots\ldots(1)$$

$$-I_B R_S - V_{BE} - 2I_E R_E + V_{EE} = 0 \quad \ldots\ldots(2)$$

But, $\quad I_C = \beta I_B \quad$ and $\quad I_C \approx I_E$ ....(3)

- According to equation (3), $\quad I_B = \frac{I_C}{\beta} = \frac{I_E}{\beta} \quad$ …………(4)

- Putting the value of equation (4) in (2),we get,

$$-\frac{I_E}{\beta} R_S - V_{BE} - 2I_E R_E + V_{EE} = 0 \quad \ldots\ldots\ldots\ldots (5)$$

$$-I_E\left[\frac{R_S}{\beta} + 2R_E\right] + V_{EE} - V_{BE} = 0 \quad \ldots\ldots\ldots\ldots (6)$$

$$I_E\left[\frac{R_S}{\beta} + 2R_E\right] = V_{EE} - V_{BE} \quad \ldots\ldots\ldots\ldots (7)$$

$$I_E = \frac{V_{EE}-V_{BE}}{\left[\frac{R_S}{\beta} + 2R_E\right]} \quad \ldots\ldots\ldots\ldots (8)$$

In practice, $\quad \frac{R_S}{\beta} << 2R_E \quad$ ..………(9)

$I_E = \frac{V_{EE}-V_{BE}}{2R_E}$ …………(10)

- From the above equation (1), we can observe the following points.
  i. R_E(Emitter resistance) determines the emitter circuit of TQ_1 and TQ_2 for the known value of V_{EE}.
  ii. Then, the collector resistance (R_L) is independent of current that flows through Emitter terminals of TQ_1 and TQ_2.

The collector voltage, $V_C = V_{CC} - I_C R_C$.........................(11)

- Neglecting the drop across R_S, we can obtain the emitter voltage of TQ_1 as approximately equal to $-V_{BE}$.
- Then, $V_{CE} = V_C - V_E = (V_{CC} - I_C R_C) - V_{BE}$ .... (12)
  $V_{CE} = V_{CC} + V_{BE} - I_C R_C$
- Hence, $I_E = I_C = I_{CQ}$ while $V_{CE} = V_{CEQ}$ for given values of V_{CC} and V_{EE}.
- Therefore operating point (Q) can be obtained from equation (10) and (12).

❖ **AC ANALYSIS:(Nov/Dec 2016)**

- For performing AC analysis, we must apply AC input signals as an input. So, we can calculate the following:

E. Differential mode gain (A_d).
F. Common mode gain (A_c).
G. Input resistance (R_i).
H. Output resistance (R_o).

The above can be obtained by using h-parameters.

D. Differential gain (A_d)

- To obtain the Differential mode gain, the two input signals must be different from each other.
- Here, we take the two a.c input signals as equal in magnitude but having 180^o phase shift between them.
- Then, the magnitude of each a.c input voltage V_{S1} and V_{S2} is $\frac{V_S}{2}$.
- For the a.c purposes, emitter terminal can be grounded which is shown in figure below with small signal analysis.

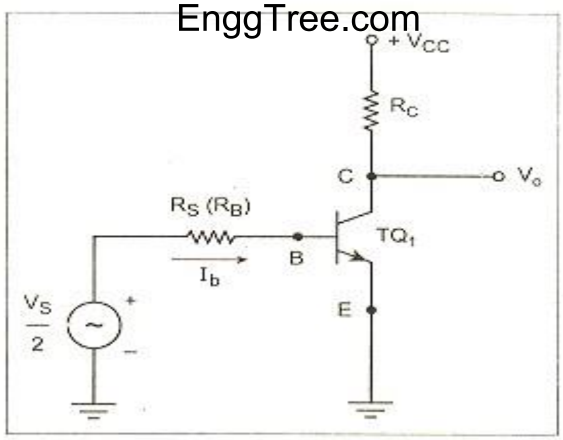
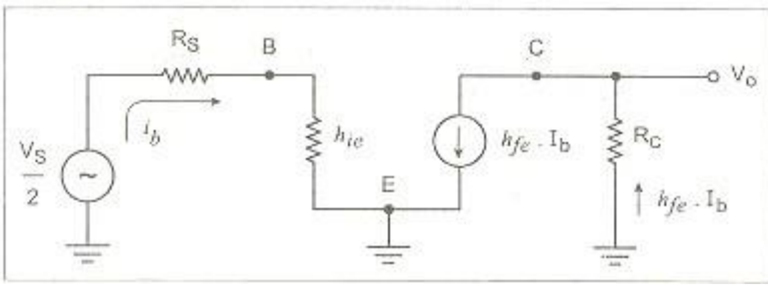


Figure (1): AC Equivalent for differential operation (half circuit concept)

- The circuit which can be analyzed by considering only one transistor is called Half circuit concept of analysis.



Figure(2): Approximate hybrid model

- For obtaining the differential mode gain (A_d) from the above hybrid model, we have to apply the Kirchhoff's voltage law in input side,

$$\frac{V_S}{2} = i_b R_S + i_b h_{ie} \quad \text{........(1)}$$

$$\frac{V_S}{2} = i_b (R_S + h_{ie}) \quad \text{........(2)}$$

$$i_b = \frac{V_S}{2(R_S + h_{ie})} \quad \text{.........(3)}$$

- Similarly, applying the Kirchhoff's voltage law to output loop, we get

$V_o = - I_b h_{fe} \cdot R_C$ ....(4)

- Put the value of I_b in equation (4) from (3), we get,

$$V_o = \frac{-h_{fe} V_S R_C}{2(R_S + h_{ie})} \text{.........(5)}$$

- Then, $\frac{V_o}{V_S} = \frac{-h_{Fe} \cdot R_C}{2(R_S + h_{ie})}$ ....(6)

- Negative sign indicates that 180^0 phase difference between input and output. If the input signals are equal and are out of phase by 180^0, we get

- Differential mode signal $V_d = V_1 - V_2 = \left(\frac{V_S}{2}\right) - \left(-\frac{V_S}{2}\right) = V_S$ ……(7)

Where, V_S is differential input voltage.

- Differential voltage gain $A_d = \frac{V_o}{V_S}$

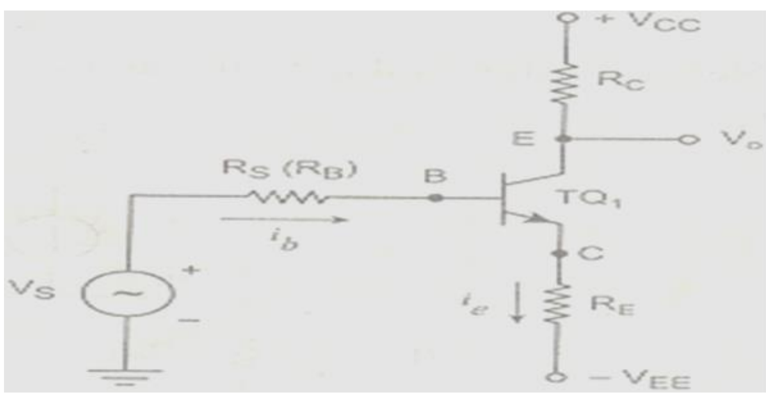
$$A_d = \frac{h_{fe}R_C}{2(R_S + h_{ie})} \dots\dots\dots (8)$$

- When the output of differential amplifier is measured with reference to ground, it is called unbalanced output.
- The output across the collectors of Q_1 and Q_2 to be perfectly matched then A_d for balanced output is twice than that of A_d for unbalanced output. Therefore

$$A_d = \frac{h_{fe}R_C}{(R_S + h_{ie})} \dots\dots\dots\dots\dots\dots (9)$$

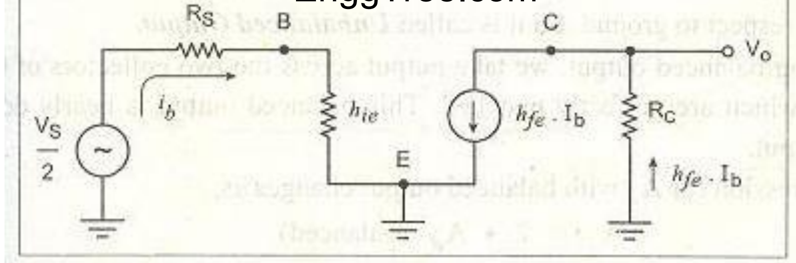
E. Common mode gain (A_C)

- In common mode, the both transistor's input magnitude and phases are also inphase with each other.
- Let us assume that input signals are having the same magnitude V_S and are in same phase.
- Common mode voltage $V_C = \frac{V_1+V_2}{2} = \frac{V_S+V_S}{2} = V_S$ ………(10)
- If suppose, the output is expressed as, $V_o = A_C . V_S$ ……(11)
- Common mode gain $A_C = \frac{V_o}{V_S}$ …….(12)
- In this mode, both the emitter current $I_{e1} = I_{e2} = I_e$ of TQ_1, TQ_2 flows through R_E in the same direction, with same magnitude.
- Hence, the total current flowing through R_E is nearly $2I_e$ …..(13)



Figure(1): A.C. Equivalent Circuit for Common Mode Configuration

- Then the approximate hybrid model for the above circuit can be obtained and is used to obtain the A_d.



Figure(2): Approximate Hybrid model

- As the current through R_E is $2I_e$, for simplicity of derivation, we have to assume the I_e and effective emitter resistance as $2R_E$.
- Current through R_C = Load current I_L
- Effective emitter = 2 R_E
- Current through emitter resistance = $I_L + I_b$
- Current through h_{oe} = ($I_L - h_{fe} . I_b$)
- Now, applying Kirchhoff's voltage law to input side,

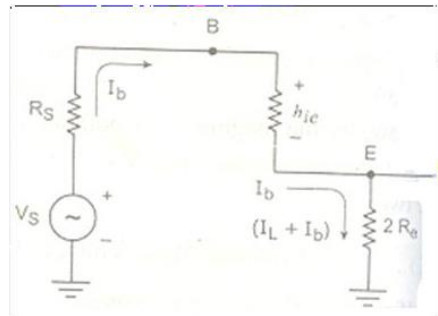


Figure (3): Input side

$-I_b R_S + I_b h_{ie} + 2R_E(I_L + I_b) = - V_S$ ……(14)

$I_b R_S - I_b h_{ie} - 2R_E(I_L + I_b) = V_S$............................(15)

While, $V_o = - I_L . R_C$..(15a)

- Negative sign is due to the assumed direction of current. Similarly apply KVL to output side.

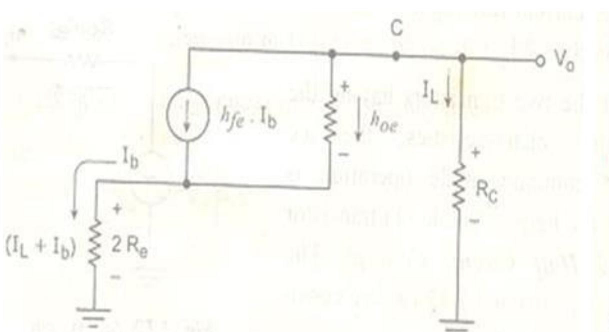


Figure (4): Output side

$$\frac{-(I_L - h_{Fe} I_b)}{h_{oe}} - 2R_E(I_L + I_b) - I_L R_C = 0 \ldots. (16)$$

$$\frac{-I_L}{h_{oe}} + \frac{h_{Fe} I_b}{h_{oe}} - 2I_L R_E - 2I_b R_E - I_L R_C = 0 \ldots(17)$$

$$I_b\left[\frac{h_{Fe}}{h_{oe}} - 2R_E\right] = I_L\left[\frac{1}{h_{oe}} + 2R_E + R_C\right] \ \ldots\ldots\ldots (18)$$

- Multiplying both sides by h_{oe}, then

$I_b[h_{fe} - 2R_E h_{oe}] = I_L[\,1 + h_{oe}(2R_E + R_C)]$.................(19)

$$\frac{I_L}{I_b} = \frac{[h_{fe} - 2R_E h_{oe}]}{[1 + h_{oe}(2R_E + R_C)]} \ldots\ldots\ldots(20)$$

$$I_b = \frac{I_L[1+h_{oe}(2R_E+R_C)]}{[h_{Fe}-2R_E h_{oe}]} \ldots\ldots\ldots\ldots(21)$$

- Putting this I_b in equation (15),

$$V_S = \frac{I_L[1 + h_{oe}(2R_E + R_C)][R_S + h_{ie} + 2R_E] + 2R_E}{[h_{fe} - 2R_E h_{oe}]}$$

$$\frac{V_S}{I_L} = \frac{[1 + h_{oe}(2R_E + R_C)][R_S + h_{ie} + 2R_E] + 2R_E}{[h_{fe} - 2R_E h_{oe}]} \ldots(22)$$

- Then, find LCM and adjusting the terms,

$$\frac{V_S}{I_L} = \frac{2R_E(1 + h_{fe}) + R_S(1 + 2R_E h_{oe}) + h_{ie}(1 + 2R_E h_{oe}) + h_{oe}R_C(2R_E + R_S + h_{oe})}{[h_{fe} - 2R_E h_{oe}]}$$

$$\frac{V_S}{I_L} = \frac{2R_E(1 + h_{fe}) + (R_S + h_{ie})(1 + 2R_E h_{oe}) + h_{oe}R_C(2R_E + R_S + h_{oe})}{[h_{fe} - 2R_E h_{oe}]} \ldots(23)$$

- Actually $h_{oe}R_C \ll 1$. Neglecting the terms,

$$\frac{V_S}{I_L} = \frac{2R_E(1 + h_{fe}) + (R_S + h_{ie})(1 + 2R_E h_{oe})}{[h_{fe} - 2R_E h_{oe}]} \ldots(24)$$

$$I_L = \frac{V_S.[h_{fe} - 2R_E h_{oe}]}{2R_E(1 + h_{fe}) + (R_S + h_{ie})(1 + 2R_E h_{oe})} \ldots(25)$$

- Putting this I_L in equation (15a),

$$V_o = - I_L . R_C$$

$$V_o = \frac{-V_S.[h_{Fe}-2R_E h_{oe}]R_C}{2R_E(1+h_{Fe})+(R_S+h_{ie})(1+2R_E h_{oe})} \ldots\ldots(26)$$

- Hence the common mode gain can be written as,

$$A_C = \frac{V_o}{V_S} = \frac{[2R_E h_{oe} - h_{fe}]R_C}{2R_E(1 + h_{fe}) + (R_S + h_{ie})(1 + 2R_E h_{oe})} \ldots\ldots(27)$$

- In practice, h_{oe} is neglected, because the expression for A_C can be further modified as,

$$A_C = \frac{-h_{fe}R_C}{R_S + h_{ie} + 2R_E(1 + h_{fe})} \ldots(28)$$

- The above expression is same whether the output is balanced or unbalanced.

COMMON MODE REJECTION RATIO (CMRR):

- $CMRR = \left|\frac{A_d}{A_C}\right|$
- From equation (8) and (28),

$$CMRR = \left|\frac{\frac{h_{Fe}R_C}{2(R_S+h_{ie})}}{\frac{h_{Fe}R_C}{(R_S+h_{ie}+2R_E(1+h_{Fe})}}\right| \ldots\ldots(29)$$

$$\text{CMRR} = \left|\frac{(R_S + h_{ie} + 2R_E(1 + h_{fe}))}{2(R_S + h_{ie})}\right| \quad \dots (30)$$

- This is CMRR for dual input balanced output differential amplifier circuit.

- For balanced case,

$$\text{CMRR} = \left|\frac{(R_S + h_{ie} + 2R_E(1 + h_{fe}))}{(R_S + h_{ie})}\right|$$

- or unbalanced case,

$$\text{CMRR} = \left|\frac{(R_S + h_{ie} + 2R_E(1 + h_{fe}))}{2(R_S + h_{ie})}\right|$$

C. Input Impedance (R_i):

- R_i is defined as the equivalent resistance existing between any one of the input and the ground when other input terminal is grounded.

$$R_i = \frac{V_S}{I_b}$$

- Put the V_S and $I_b$from the above discussion, $R_i = 2(R_S + h_{ie})$.

- For one transistor and input pair, the resistance is $R_S + h_{ie}$.

- Hence for dual input circuit, the total input resistance is $2(R_S + h_{ie})$, as the 2 circuits are perfectly matched.

- This input resistance is not dependent on whether output is balanced or unbalanced.

D) OUTPUT IMPEDANCE R_O:

- It is defined as the equivalent resistance between one of the output terminals with respect to ground.
- The resistance between output terminal with respect to ground is R_C.

  $R_O = R_C$

6. Explain the FET input stages.

❖ **FET parameters:**

- The following are the parameters of FET as an amplifier.

1. The transcondutance 'g_m'
2. The dynamic resistance 'r_d' and
3. The amplification factor μ.

- **Transcondutance:**

✓ It is defined as the ratio of change in drain current to the change in gate source voltage at a constant drain source voltage.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} / \Delta V_{DS} = \text{Constant}$$

✓ It is expressed in mill amperes per volt or micro mhos. It is sometimes referred to as the common source forward trans admittance.

- **Dynamic Drain Resistance or output Resistance:**

✓ The drain resistance is defined as the ratio of change in drain source voltage V_{DS} to the change in drain current I_D at a constant gate source voltage.

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} / \Delta V_{GS}$$

✓ The reciprocal of drain resistance is the drain conductance, it is called sometimes as common source output conductance.

- **Amplification factor:**

✓ Amplification factor is defined as the ratio of change in drain source voltage to the change in gate source voltage at a constant drain current.

$$\mu = \frac{\Delta VDS}{\Delta V_{GS}} / \Delta I_D$$

- **Relation between FET parameters:**

✓ We know that $\mu = \frac{\Delta VDS}{\Delta V_{GS}}$

✓ Multiplying the numerator and the denominator on the R.H.S by ΔI_D, We have

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \text{ x } \frac{\Delta I_D}{\Delta I_D} = \frac{V_{DS}}{I_D} \text{ x } \frac{I_D}{V_{GS}} = g_m \text{ x } r_d$$

✓ Therefore μ = g_m x $r_d$is the relation between the parameters of a FET.

- **FET configurations:**

✓ There are three types of configurations in the FET amplifier, they are:

- Common source configuration
- Common drain configuration
- Common gate configuration

✓ A FET can be connected in any one of the three configurations. The common drain circuit also called source follower circuit.

Single tuned amplifiers

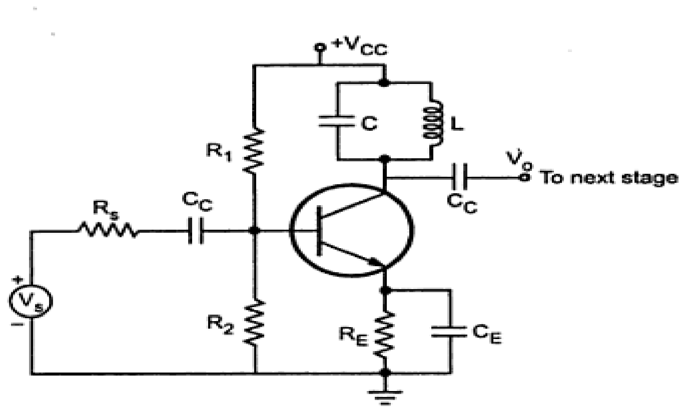
7. Draw the circuit diagram of a single tuned amplifier and obtained expression for its gain ,resonant and cut off frequency (May/June 2016), (Nov/Dec2015)

(OR)

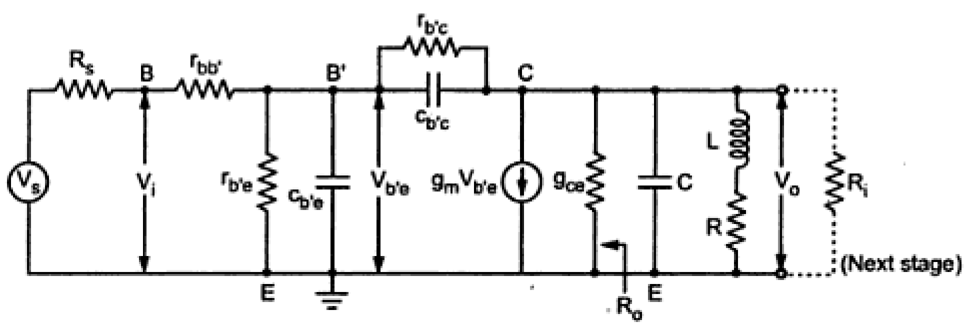
Illustrate the behavior of a MOSFET based amplifier circuit tuned load. Also deduce expression for voltage gain at Centre frequency, Q and bandwidth. (April/May 2019)

SINGLE TUNED CAPACITIVE COUPLED TUNED AMPLIFIER

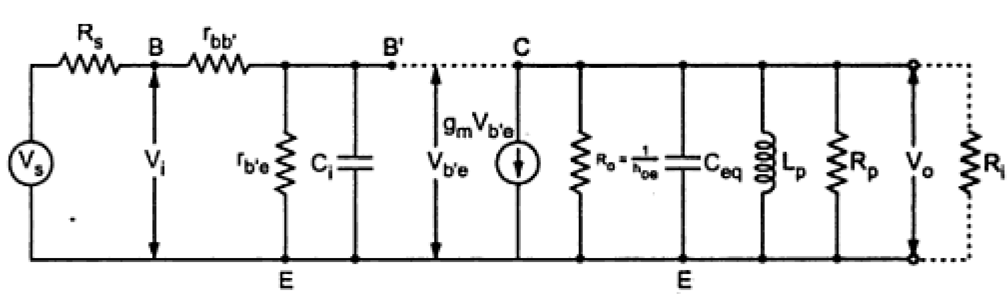
- Tuned amplifiers are amplifiers that are designed to reject a certain range of frequencies below a lower cut off frequency ω_L and above a upper cut off frequency ω_H and allows only a narrow band of frequencies.



- The output across the tuned circuit is coupled to the next stage through the coupling capacitor. The tuned circuit is formed by L and C resonates at the frequency of operation.



Equivalent circuit of single tuned amplifier



Here C_i and C_{eq} represent input and output circuits capacitance respectively. They can be given as

$C_i = C_{be} + C_{bc}$ (1-A) where A is the voltage gain of the amplifier

$C_{eq} = C_{be}$((A-1) / A)+C where C is the tuned circuit capacitance

The g_{ce} is represented as the output resistance of current of generator gmV_{be}

$g_{ce} = (1 / r_{ce}) = h_{ce} - gm*h_{ce} = h_{ce} = (1/R_0)$

The admittance of the inductor along with resistor R is given by

$$Y = \frac{1}{R + j\omega L}$$

Multiplying numerator and denominator by $R + j\omega L$we get

$$Y = \frac{R - j\omega L}{R^2 + \omega^2 L^2} = \frac{R}{R^2 + \omega^2 L^2} - \frac{j\omega L}{R^2 + \omega^2 L^2} = \frac{R}{R^2 + \omega^2 L^2} - \frac{j\omega^2 L}{\omega(R^2 + \omega^2 L^2)} = \frac{1}{R_P} + \frac{1}{j\omega L_P}$$

Where $R_P = \frac{R^2 + \omega^2 L^2}{R}, and L_P = \frac{R^2+\omega^2 L^2}{\omega^2 L}$

The LP and RP are in shunt quality factor of the coil at resonance is given by

Qo = WoL/ R

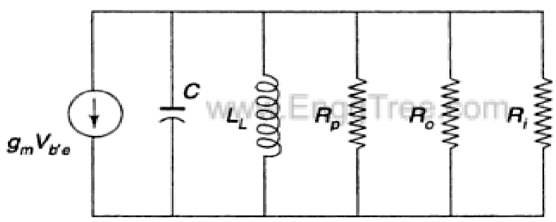
$$L_P = \frac{R^2 + \omega^2 L^2}{\omega^2 L}$$

Dividing numerator and denominator terms by$\omega^2 L$,

$$L_P = \frac{R^2/\omega^2 L + L}{1}$$

$$L_{P \approx L}$$

Hence, The output circuit of the amplifier can be modified as



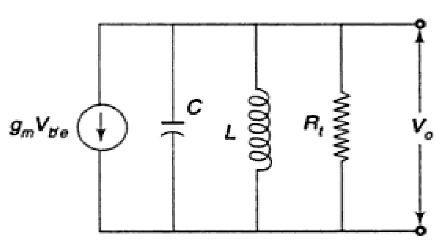
Equivalent circuit of the output part of the tuned amplifier

Taking R_1 as the parallel combination of R_0, R_P and R_i i.e.

$$\frac{1}{R_t} = \frac{1}{R_0} + \frac{1}{R_P} + \frac{1}{R_i}$$

The output circuit can be modified as shown in fig.

$$\boldsymbol{Q_e} = \frac{\text{Susceptance of inductance L C}'\text{capacitance C}}{\text{Conductance shunt resistance R}_t}$$



Simplified output circuit of the tuned amplifier

Where Z is the impedance of C, L and $R_t$inparallel. The admittance Y = (1/Z) is given by

$$Y = \frac{1}{Z} = \frac{1}{R_t} + \frac{1}{j\omega L} + j\omega C = \frac{1}{R_t}[1 + \frac{R_t}{j\omega L} + j\omega CR_t]$$

Multiplying numerator and denominator by ω_0

$$Y = \frac{1}{R_t}[1 + \frac{R_t\omega_0}{j\omega L\omega_0} + \frac{j\omega\omega_0 CR_t}{\omega_0}]$$

$$\frac{R_t}{L\omega_0} = \omega_0 CR_t = Q_e$$

$$Y = \frac{1 + jQ_e[\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}]}{R_t}$$

$$Z = \frac{1}{Y} = \frac{R_t}{1 + jQ_e[\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}]}$$

Let δ the fractional frequency variation.

$$\delta = \frac{\omega - \omega_0}{\omega_0} = \frac{\omega}{\omega_0} - 1 = \frac{\omega}{\omega_0} = 1 + \delta$$

$$Z = \frac{R_t}{1 + jQ_e[(1+\delta) - (\frac{1}{1+\delta})]} = \frac{R_t}{1 + jQ_e[\frac{1 + \delta^2 + 2\delta - 1}{1+\delta}]}$$

$$Z = \frac{R_t}{1 + j2Q_e\delta[\frac{\frac{\delta}{2} + 1}{1+\delta}]}$$

Frequency close to resonance $\omega_0, \delta << 1$

$$Z = \frac{R_t}{1 + j2Q_e\delta}$$

At resonance $\omega = \omega_0, \delta = 0$

$$Z = R_t = R_0 \; parallel \; R_P \; Parallel \; R$$

$$R_P = \frac{\omega_0 L^2}{R} = \frac{\omega_0 L}{\omega_0 CR}$$

$$V_{b'e} = V_i \frac{r_{b'e}}{r_{bb'} + r_{b'e}}$$

$$V_0 = -g_m V_{b'e} Z = -g_m (V_i \frac{r_{b'e}}{r_{bb'} + r_{b'e}}) Z$$

Voltage gain with out considering the source resistance is given by

$$A_v = \frac{V_o}{V_i} = -g_m \left(\frac{r_{b'e}}{r_{bb'} + r_{b'e}}\right) Z$$

$$A_v = -g_m \left(\frac{r_{b'e}}{r_{bb'} + r_{b'e}}\right) * \frac{R_t}{1 + j2Q_e\delta}$$

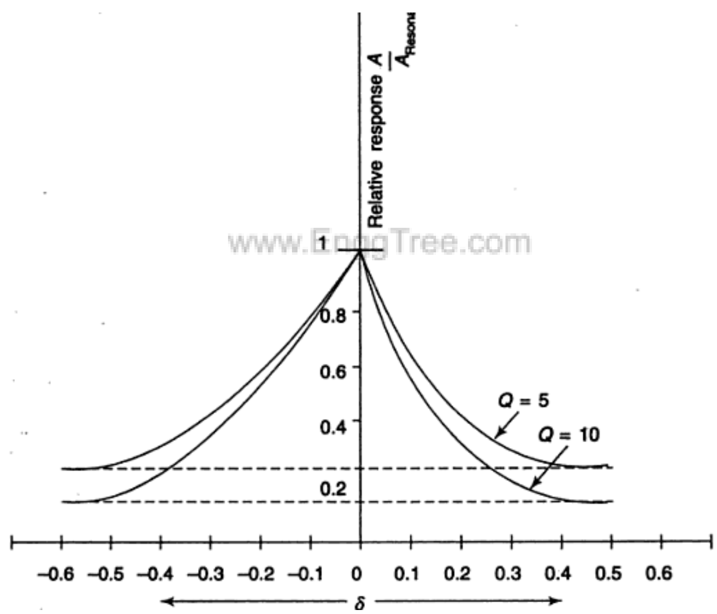
$$A_v(at\ resonance) = -g_m \left(\frac{r_{b'e}}{r_{bb'} + r_{b'e}}\right) * R_t$$

$$\left|\frac{A_v}{A_v(at\ resonance)}\right| = \frac{1}{\sqrt{1 + (2\delta Q_e)^2}}$$

$$2\delta = \frac{1}{Q_e}$$

$$\Delta\omega = \frac{1}{R_t C}\ rad/sec$$

Gain $\frac{Av}{A_v(at\ resonance)}$ plotted against δ



8. Draw the frequency response of an ideal and a practical tuned amplifier and discuss their characteristics. (Nov/Dec 2018)

The amplifier that amplifies a particular frequency and rejects other frequencies are termed as tuned amplifiers.

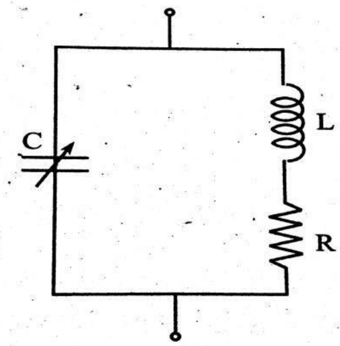


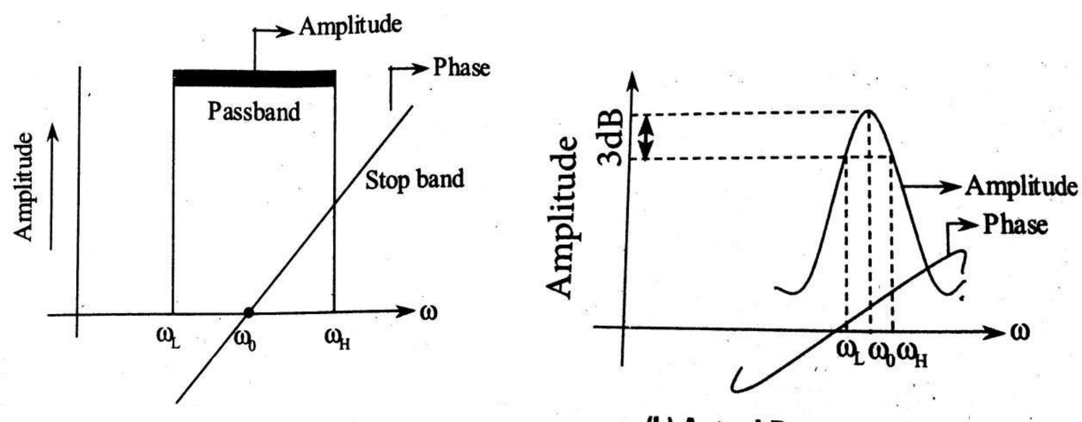
Figure (1): Ideal Tuned Circuit

Basically the tuned amplifier amplify the signal within a narrow frequency band that is centered about a frequency f_0. The signal between the lower and higher cut-off frequencies is amplified. The resonant frequency of an ideal tuned circuit is expressed as,

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \quad \text{(or)} \quad \omega_0 = \frac{1}{\sqrt{LC}} \quad [\text{since } \omega_0 = 2\pi f_0]$$

Figures 2(a), 2(b) illustrates the ideal response and actual response curve of a tuned amplifier circuit respectively.

From the figure 2(b), it is observed that at higher and lower cut-off frequencies, the curve decreases and is maximum at resonant frequency (f_0).



(a) Ideal Response **(b) Actual Response Curve**

The behavior of tuned circuit at various frequencies is,

1. At frequencies *above resonant frequency*, the circuit behaves as *capacitive load* due to which the *current leads the applied voltage*.
2. At frequencies *below resonant frequency*, the circuit behaves as *inductive load* due to which the *current lags behind the applied voltage*.
3. *At resonant frequency*, the circuit behaves as *resistive load* since the *inductive and capacitive effects are nullified*.

9. Explain briefly about gain and frequency response of single-tuned amplifier.

- The voltage gain of an amplifier depends upon current gain (β), input resistance (R_i) and effective or a.c load resistance.
- The voltage gain is given by the relation,

$$A_v = \beta \times \frac{r_L}{R_i}$$

- The a.c load resistance of a parallel resonant circuit (i.e., tuned circuit) is given by the relation,

$$R_L = Z_p = \frac{L}{CR}$$

Where, L = value of inductance,

C = value of capacitance, and

R = value of effective resistance of the inductor.

- Voltage gain of a voltage amplifier is given by the relation,

$$A_v = \beta \times \frac{\frac{L}{CR}}{R_i}$$

- We know that the value of the quantity $\frac{L}{CR}$ (changes above or below the resonant called impedance of the tuned circuit) is very high at the resonant frequency and it decreases as the frequency changes above or below the resonant frequency.
- Therefore voltage gain of a tuned amplifier is very high at the resonant frequency and it decreases as the frequency changes above or below the resonant frequency.
- The above facts are shown in the form of a voltage gain versus frequency plot shown in figure below.

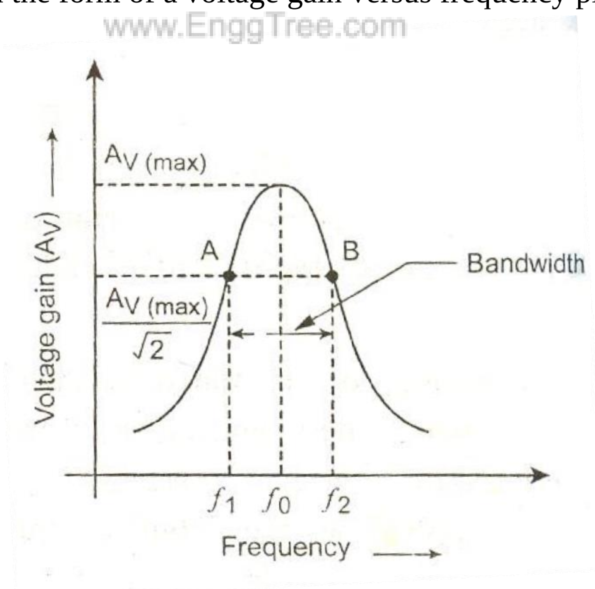


Figure: Frequency response curve

- Such a plot is called Frequency response curve of a tuned voltage amplifier.
- The bandwidth (BW) of an amplifier is equal to the frequency difference between the point A and B on either side of the resonant frequency, where the value of voltage gain drops to $1/\sqrt{2}$ of its maximum value of resonance.
- Thus bandwidth,

$$BW = \Delta f = f_2 - f_1 = \frac{f_o}{Q_o}$$

Where Q_o is the quality factor (or Q-factor) of the tuned circuit.

Neutralization methods

10. Describe any one method of neutralization used in tuned amplifier?
Briefly explain Hazel line neutralization used in tuned amplifiers for stabilization (May/June 2016)(Nov/Dec 2016,May-2018)

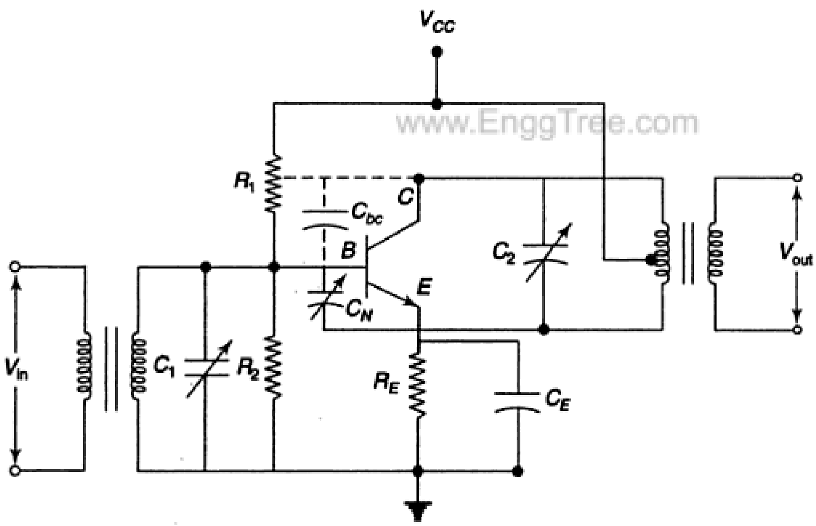
STABILITY OF TUNED AMPLIFIER

Stability of tuned amplifier is achieved by neutralization

i). Hezeltine neutralization *ii). Neutrodyne neutralization*

- ❖ In a tuned RF amplifier the transistor are used at the frequency near to their unity gain bandwidth. To amplify the narrow band of high frequencies.
- ❖ At this frequency inter-junction capacitor b/w base and collector of transistor (Cbc)of transistor becomes dominant
- ❖ As a reactance of Cbc at Rf is low and its provide feedback path from a collector to base.
- ❖ If some feedback signal reaches the input from output in a positive manner with proper phase shift then the circuit is unstable, generating its own oscillation.

Amplifier, it was necessary to reduce stage gain to a level that ensures the circuit stability



. This can be achieved in several ways

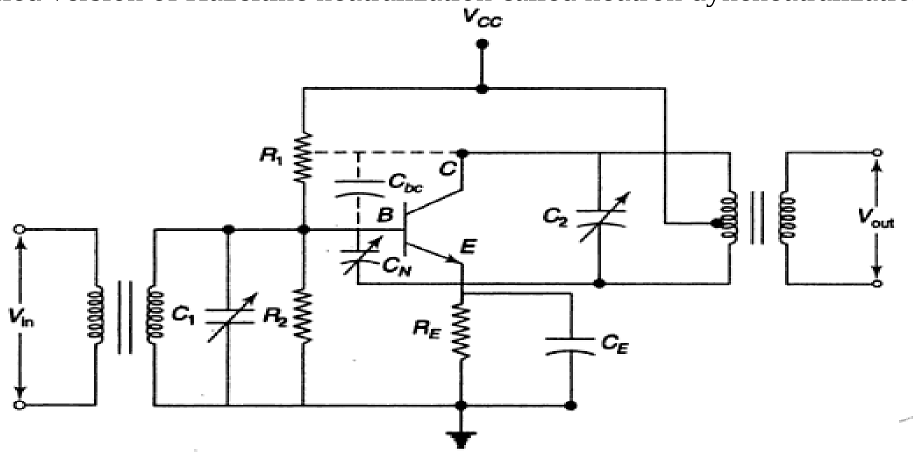
i) favoring the stability factor of the tuned circuits
ii) loose coupling b/w stages
iii) Increase looser element into the element.

- ❖ To achieve stability the professor Hazettile introduced a circuit in which the troublesome effects of the c_{bc} was neutralized by introducing a signal coupled through the C_{bc}.

HAZELTINE NEUTRALIZATION:-

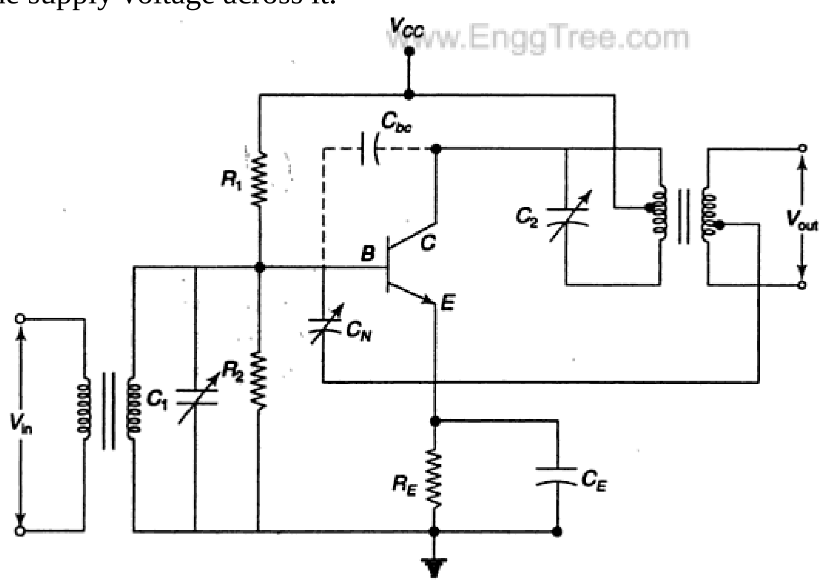
- ❖ This is the neutralization technique employed in tuned RF amplifier to maintain stability .

- ❖ The undesired effect of collector to base capacitance of the transistor is neutralized by introducing a signal which cancels the signal coupled through the collector to base capacitance
- ❖ This is achieved by a small variable capacitance (C_N)is connected from the bottom of coil to the base of the transistor .It introduce a signal to the base of the transistor such that it cancels out the signal fed to the base by Cbc
- ❖ By properly adjusted Cn exactly neutralized achived.
- ❖ Modified version of Hazeltine neutralization called neutron dyneneutralization.



NEUTRODYNE NEUTRALIZATION:-

- ❖ In a neutrodyne neutralization technique, Cn is connected to the centre trapped to the secondary coil.
- ❖ Hence it is connected with Vcc which ensures that it is insensitivity to any variation is supply voltage Vcc .Hence provided higher neutralization for the tuned amplifier.
- ❖ In principle, the circuit functions are the same manner as the hazeltine neutralizing capacitor does not have the supply voltage across it.



Power amplifiers –Types (Qualitative analysis).

11. Write a short notes on Power amplifier.(Nov/Dec 2017)

- A power amplifier is an amplifier, which is capable to providing a large amount of power to the load such as loudspeaker, or motor etc.

- It is essential in almost all electronic systems where a large amount of power is required to be supplied to the load.
- The power amplifier, is used as a last stage in a electronic system. For example, a public address system (PAS) consists of a microphone, a multistage amplifier, a power amplifier and a loudspeaker.
- The microphone converts the sound waves into electrical signal, which is of very low voltage (usually of few millivolts).
- This signal is insufficient to drive the loudspeaker. Therefore this signal is first raised to a sufficiently high value (a few volts) by passing it through a multistage small-signal (or voltage) amplifier.
- This signal is then used to drive the power amplifier, because it is incapable of delivering a large amount of power to the loudspeakers.
- A power amplifier is more commonly known as audio amplifier. The audio amplifiers are used in public address system, tape recorders, stereo systems, television receivers, radio receivers, broadcast transmitters etc.
- It will be interesting to know that a power amplifier dies not actually amplify the power. As a matter of fact, it takes power from the d.c. power supply connected to the output circuit and converts it into useful a.c. signal power.
- The power is fed to the load. The type of a.c. power developed, at the output of a power amplifier, is controlled by the input signal.
- Thus we can say that actually a power amplifier is a d.c. to a.c. power converter, whose action is controlled by the input signal.
- The power amplifiers, are also known as large signal amplifiers.
- The term 'large signal' for the power amplifiers arises because these amplifiers use a large part of their a.c. load line for operation.
- It is in contrast to the small signal amplifiers, which use only 10% of their a.c. load line for operation. The small signal amplifiers are commonly known as voltage amplifiers.

12. Explain in detail the various types of power amplifier. *(OR)* **Explain with circuit diagram class B power amplifier and derive for its efficiency (Nov/Dec2015)(May 2017)(Nov/Dec-2017)**

i. Class-A amplifier:

- A class-A amplifier is one in which the operating point and the input signal are such that the current in the output circuit, flows at all times.
- A class-A amplifier operates essentially over a linear portion of its characteristics.
- In class-A operation, the transistor stays in the active region throughout the a.c cycle.
- The point and the input signal are such as to make the output current flows for 360°.
- **Voltage gain:** The voltage gain for a class-A amplifier may be obtained in the same way as the small-signal amplifier. It is given by the relation,

$$A_v = \frac{r_L}{r_e}$$

r_L = A.C. load resistance whose value is equal to the parallel combination of collector resistance (R_c) and load resistance (R_L).

r_e= A.C. emitter diode resistance.

- **Current gain:** the current gain of a transistor is the ratio of a.c. collector current (i_c) to the a.c. base current (i_b).

$$A_i = \frac{i_c}{i_b} = \beta$$

- **Power gain:** The a.c. input power to the base of transistor,

$$P_{in} = V_{in} \cdot i_b$$

And the a.c. output power from the collector.

$$P_o = -V_o \cdot i_c$$

- The negative sign in the above equation indicates that the phase of input signal is reversed at the output.

$$\text{Power gain, } A_p = \frac{P_o}{P_{in}} = \frac{-V_o . i_c}{V_{in} \cdot i_b} = -\frac{V_o}{V_{in}} \text{ x } \frac{i_c}{i_b}$$

$$= -A_v \cdot A_i = -\frac{r_L}{r_e} \text{ x } \beta$$

Where A_v = voltage gain, and

A_i = current gain.

- The overall efficiency or circuit efficiency of the amplifier circuit is defined as the ratio of a.c. power delivered to the load to the total power supplied by the d.c. source.
- Mathematically, the overall efficiency,

$$\eta_o = \frac{\text{a.c.power delivered to the load}}{\text{Total power supplied by the d.c. source}} = \frac{V_{CEQ}.I_{CQ}}{2V_{CC}.I_{CQ}}$$

- Maximum value of overall efficiency,

$$\eta_{o(max)} = \frac{V_{CEQ}.I_{CQ}}{2(\ V_{CEQ}.I_{CQ}\ )} = 0.25 = 25\%$$

- The collector efficiency of the amplifier circuit is defined as the ratio of a.c. power delivered to the load, to the power supplied by thed.c. source to the transistor.
- Mathematically, collector circuit efficiency,

$$\eta_c = \frac{\text{a.c.power delivered to the load}}{\text{power supplied by the d.c.source to the transistor}}$$

- Maximum value of collector efficiency,

$$\eta_{c(max)} = \frac{V_{CEQ}.I_{CQ}}{2(\ V_{CEQ}.I_{CQ}\ )} = 0.5 = 50\%$$

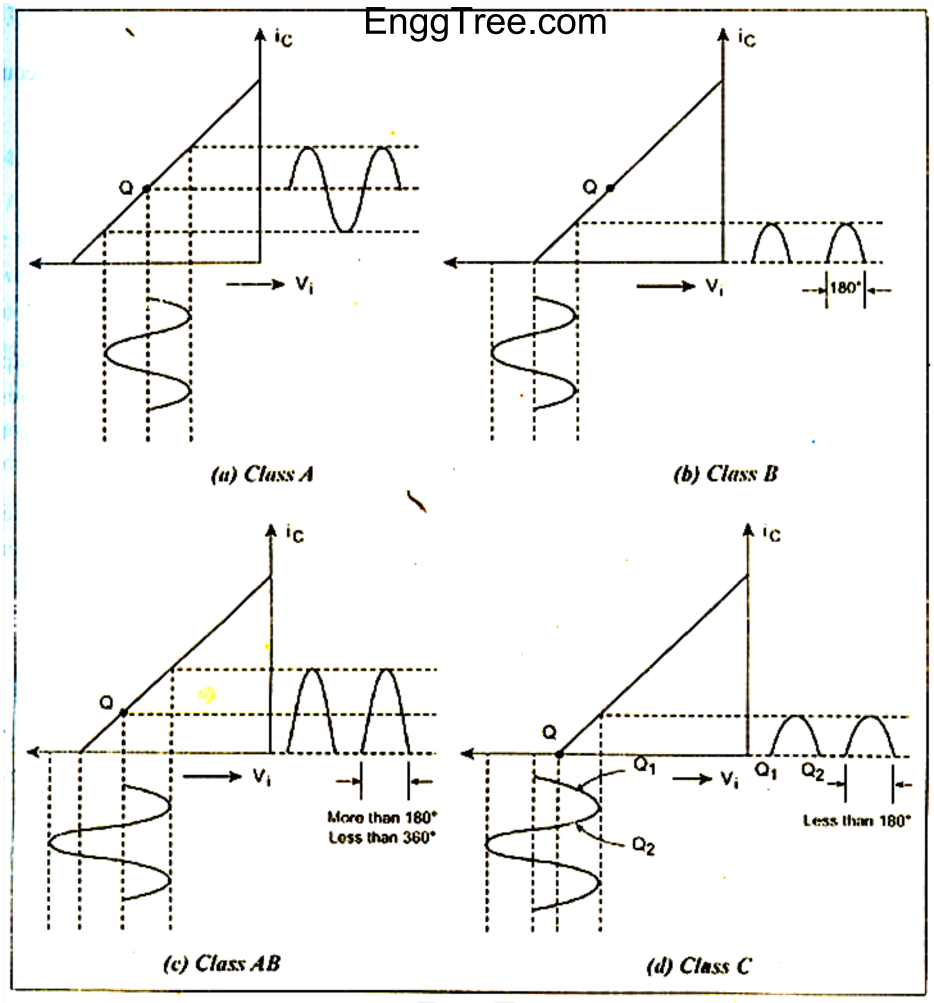


Figure: classification of amplifiers based on the biasing condition

ii. Class-B amplifier:

- A class-B amplifier is one in which the operating point is at an extreme end of its characteristics, so that the quiescent power is very small.
- Hence either the quiescent current or the quiescent voltage is approximately one half a cycle.
- In class-B operation, the transistor stays in the active region only for half the cycle. The Q-point is fixed at the cut-off point of the characteristics.
- The output current flows for 180°.
- D.C. input power: the input power comes from the d.c. source (i.e., the V_{CC} supply) and is given by the relation,

$$P_{in(dc)} = V_{CC} \, . \, I_{dc}$$

Where I_{dc} is the average value of current drawn from the V_{CC}supply.

- D.C. power loss in load resistor: Its value is given by the relation,

$$P_{RL(dc)} = I^2_{dc} \, . \, R_L$$

- A.C. output power in load resistor: Its value is given by the relation,

$P_{o(ac)} = I^2 \cdot R_L = V^2 / R_L$

Where I = the r.m.s. value of a.c. output current,

V = Ther.m.s. value of a.c. output voltage, and

V_P= The peak value of a.c. output voltage.

- Power dissipated within the resistor: Its value is given by the relation,

$$P_{c(dc)} = P_{in(dc)} - P_{RL(dc)} - P_{o(ac)}$$

- Overall efficiency: $\eta_o = \frac{P_{o(ac)}}{P_{in(dc)}} = \frac{P_o}{V_{CC} \cdot I_{dc}}$
- Maximum value of overall efficiency,

$$\eta_o = \frac{P_{o(ac)}}{P_{in(dc)}} = \frac{\frac{1}{4} V_{CP} \cdot I_{CP}}{V_{CC} \cdot I_{dc}} = 0.785 = 78.5\%$$

iii. Class-AB amplifier:

- A class-AB amplifier is one operating point between class A and class B.
- Hence the output signal is zero for part but less than one-half of an input sinusoidal signal cycle.
- The output current flows for more than 180° but less than 360°.
- a.c. power delivered to the load resistor,

$$P_{o(ac)} = V_C \cdot I_C = \left(\frac{V_P}{\sqrt{2}}\right) \cdot \left(\frac{I_P}{\sqrt{2}}\right) = \frac{V_P \cdot I_P}{2}$$

- And total power dissipation of the two transistors,

$$2\,P_{C(dc)} = P_{in(dc)} - P_{o(ac)} = V_C \cdot I_C - \frac{V_P \cdot I_P}{2}$$

$$= V_{CC} \cdot \frac{2\,I_P}{\pi} - \frac{V_P \cdot I_P}{2}$$

$$= 2\,I_P\left(\frac{V_{CC}}{\pi} - \frac{V_P}{4}\right)$$

- Overall efficiency,

$$\eta_o = \frac{P_{o(ac)}}{P_{in(dc)}} = \frac{\frac{V_P \cdot I_P}{2}}{V_{CC} \cdot \frac{2\,I_P}{\pi}} = \frac{\pi}{4} \cdot \frac{V_P}{V_{CC}} = 0.785 \frac{V_P}{V_{CC}}$$

- For the largest possible output signal, the peak value of the output voltage is equal to the V_{CC} supply (i.e., $V_P = V_{CC}$). In the case, the overall efficiency is maximum, and its value,

$$\eta_{o(max)} = 0.785 = 78.5\%$$

- The value of collector efficiency is equal to the overall efficiency, whose maximum value is also 78.5%.

iv. Class-C amplifier:

- A class-C amplifier is one in which the operating point is chosen so that the output current (or voltage) is zero for more than one-half of an input sinusoidal signal cycle.
- In class-C amplifier, the Q-point is fixed beyond the extreme end of the characteristics. The output current remains zero for more than half cycle.

- The unturned audio or video voltage amplifier with a resistive load is operated as small signal amplifier under class-A operation.
- class-B amplifiers are mostly used for power amplification in push-pull arrangement.
- class-AB and class-B operation are used with unturned power amplifiers, whereas class-C operation is used with tuned radio frequency amplifiers.

Additional Questions:

Explain briefly about push-pull amplifier

❖ **Introduction:**

- This means **one in on** and another **one is off.**
- It needs same type of transistors(i.e., NPN or PNP).
- Also it needs two transformers in both input and output sides.
- One is input transformer and other is called output transformer.
- Input is applied to input driver transformer's primary winding.
- Both transformers (input and output) is centre tapped one.
- Both are NPN means voltage V_{CC} is positive.
- Both are PNP means voltage V_{CC} is negative.

❖ **Basic principle of operation:**

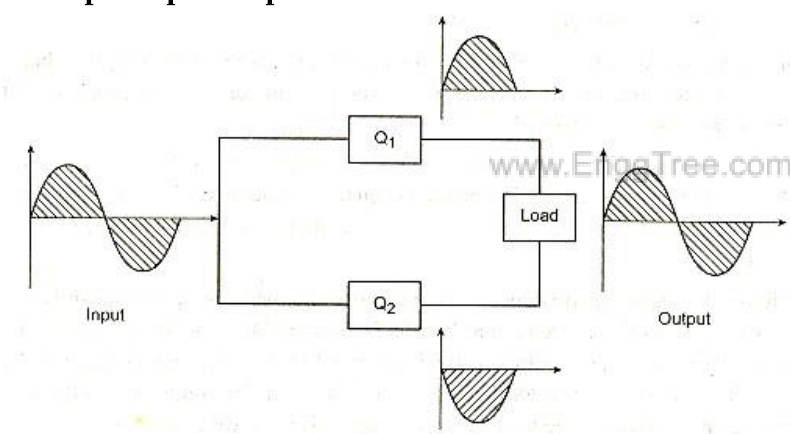


Figure: Basic operation diagram

- During the positive half cycle of the applied input Q_1 is only under ON condition. The positive half cycle is across the load.
- Similarly, During the Negative half cycle of the applied input Q_2 is only under ON condition. So the Negative half cycle is across the load.

❖ **Push-pull class-B amplifier:**

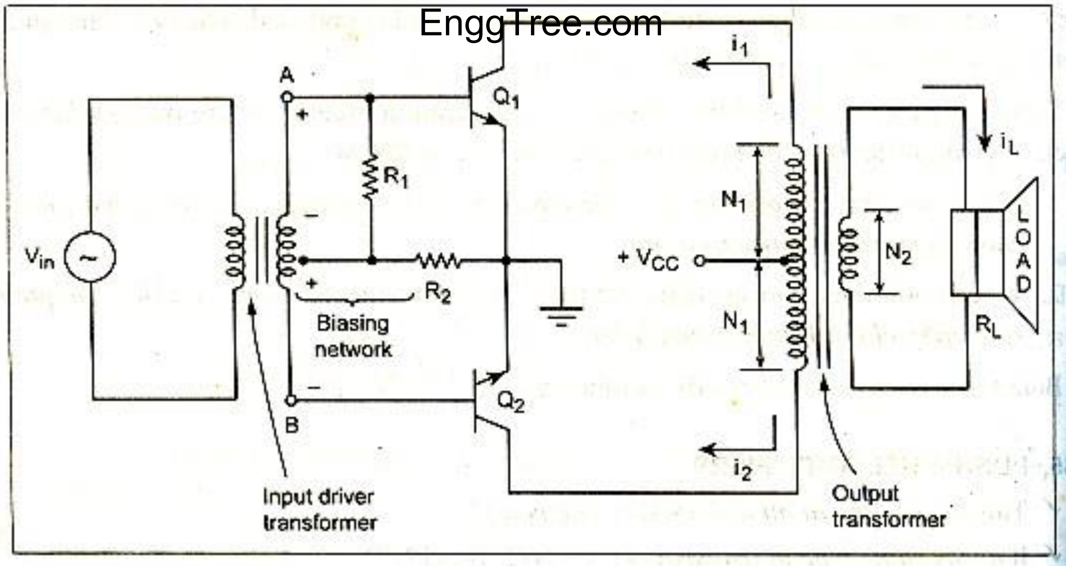


Figure: Push-pull amplifier- class-B

- In the above circuit, both transistors is of NPN type.
- If both are PNP, the supply voltage must be $-V_{CC}$. but basic diagram is same.
- Input driver transfer driver circuit drives the circuit, then the input signal is applied to the primary of the driver transformer.
- The centre tap on the secondary of the driver transformer is grounded. The centre tap on the primary of the output transformer is connected to the supply voltage $+V_{CC}$.
- Whenever the input signal is under positive half cycle, when point A is positive with respect to B, then the transistor Q_1 is in the active region. But Q_2 is under in OFF condition now.So the load gets this positive voltage drop output across it.
- Then, point B is positive with respect to A under negative half cycle. So, Q_1 is in the OFF condition.so the load gets voltage in negative across it due to negative voltage. This is shown in the waveform.
- For the output transformer, the number of turns of each half of the primary is N_1. But in the secondary, it is N_2.
- Hence, the total number of turns in primary side of output transformer is $2N_1$.
- Then turns ratio is $2N_1 : N_2$.
- **D.C operation:**
  - ✓ The Q-point is adjusted on the X-axis such that, $V_{CEQ} = V_{CC}$ and I_{CEQ} is zero. The coordinates of the Q-point are $(V_{CC},0)$. There is no d.c base bias voltage.
- **D.C power input:**
  - ✓ Each transistor output is in the form of half rectified waveform. Hence, if I_m is the peak value of the output current of each transistor, the dc or A_V value is $\frac{I_m}{\pi}$, due to half rectified waveform.
  - ✓ Then, two currents drawn by the two transistors, form the A.C supply are in the same direction.
  - ✓ Therefore, the total D.C or average current drawn from the A.C supply is algebraic sum of the individual average current drawn by each transistor,

$$I_{dc} = \frac{I_m}{\pi} + \frac{I_m}{\pi} = \frac{2I_m}{\pi} \quad \text{.............................(1)}$$

✓ The total d.c power input is given by,

$$P_{dc} = V_{CC} * I_{dc} \quad \text{.............................(2)}$$

$$P_{dc} = \frac{2}{\pi} V_{CC} . I_m \quad \text{...........................(3)}$$

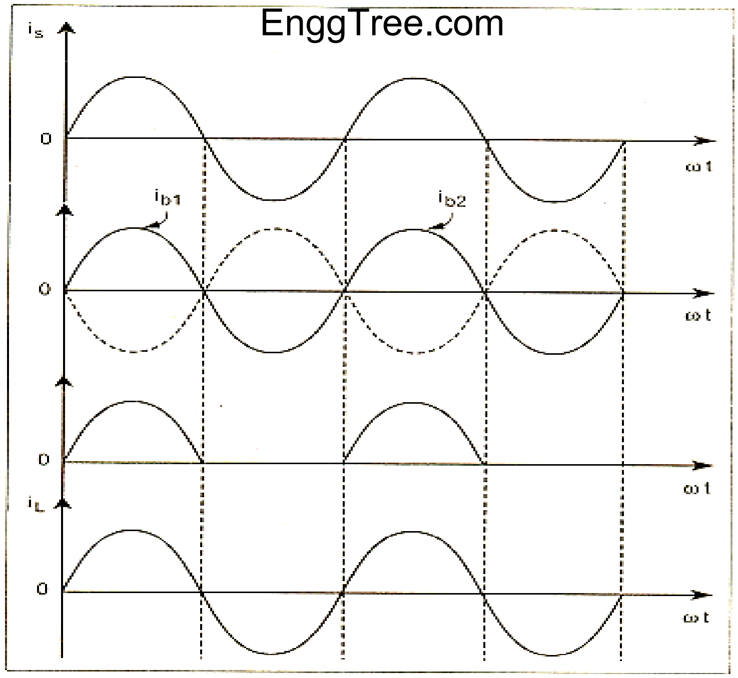


Figure: Waveform output

- **A.C operation:**
  - ✓ When A.C signal is applied to the input driver transformer, for positive half cycle Q_1 transistor is under ON condition. Then, its current flow path is shown in the following diagram.

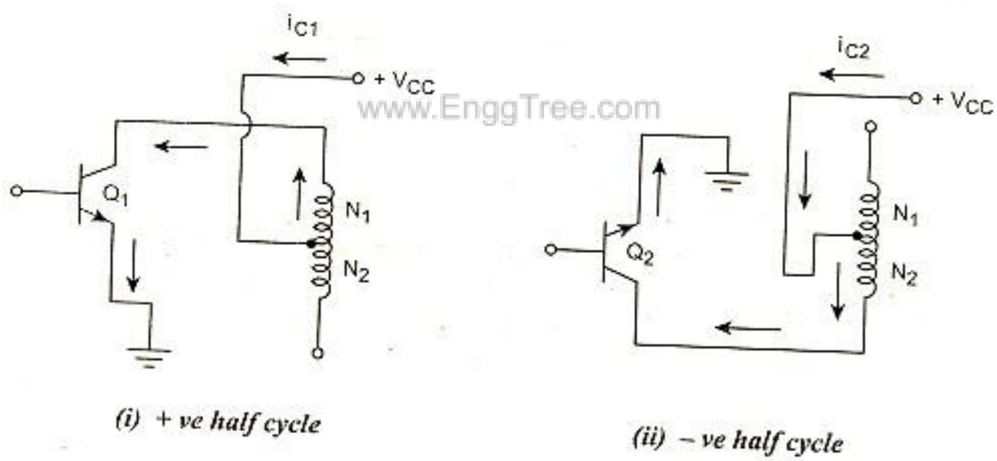


Figure: current path

  - ✓ From the above figure, when Q_1 conducts, lower half of the primary of the input transformer does not carry any current. Hence. Only N_1number of turns carry the current.
  - ✓ While, when Q_2conducts , upper half of the primary does not carry any current. Therefore again only N_1 number of turns carry the current.
  - ✓ Hence, the reflection on the primary can be written as,

$$R_L' = \frac{R_L}{n.n} \text{……..(4)and} \quad n = \frac{N_2}{N_1} \quad \text{……..(5)}$$

  - ✓ Note that the step down turns ratio is $2N_1 : N_2$ but while calculating the reflected load, the ratio n becomes $N_2 : N_1$.
  - ✓ So each transistor shares equal load which is the reflected load R_L'.

- ✓ The slope of the a.c load line is $\frac{1}{R_L'}$. The dc load line is the vertical line passing through the Q on the X-axis. The load lines are shown below.

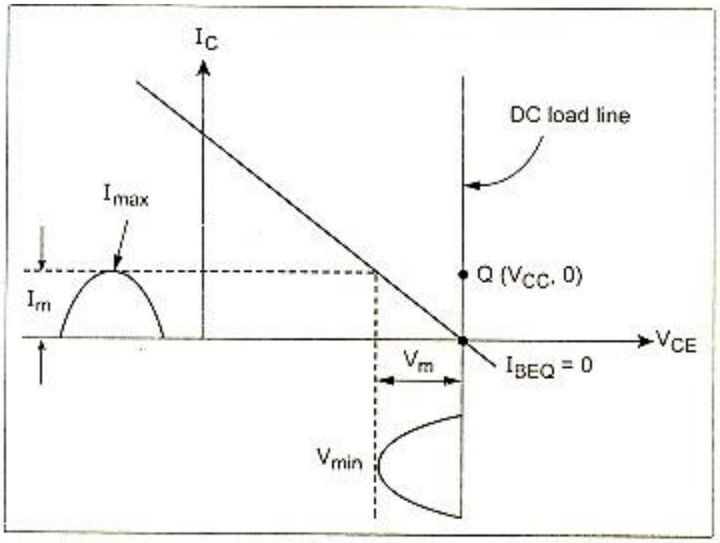


Figure: load lines for push-pull class B amplifier

- ✓ The slope of the a.c load line (magnitude of slope) can be represented in terms of V_m and I_m,

$\frac{1}{R_L'} = \frac{I_m}{V_m}$ ………..(6)

$$R_L' = \frac{V_m}{I_m} \text{ ………(7)}$$

Here, V_m = peak value of the collector circuit

- **A.C power output:**

  - ✓ As I_m and V_m are the peak values of the output current and the output voltage respectively. Then

$V_{rms} = \frac{V_m}{\sqrt{2}}$ …..(8) and $I_{rms} = \frac{I_m}{\sqrt{2}}$ ……(9)

The power output is, $P_{ac} = V_{rms} . I_{rms}$

$= I_{rms} . R_L' . I_{rms}$

$= I_{rms}^2 . R_L'$ …………………… (10)

$= V_{rms}^2 / R_L'$

- **Efficiency:** The efficiency of class-B amplifier can be calculated as follows:

$\%\eta = \frac{P_{ac}}{P_{dc}} \times 100$ ....(11)

$= \frac{\frac{V_m I_m}{2}}{\frac{2}{\pi} V_{CC} . I_m} * 100$ ……(12)

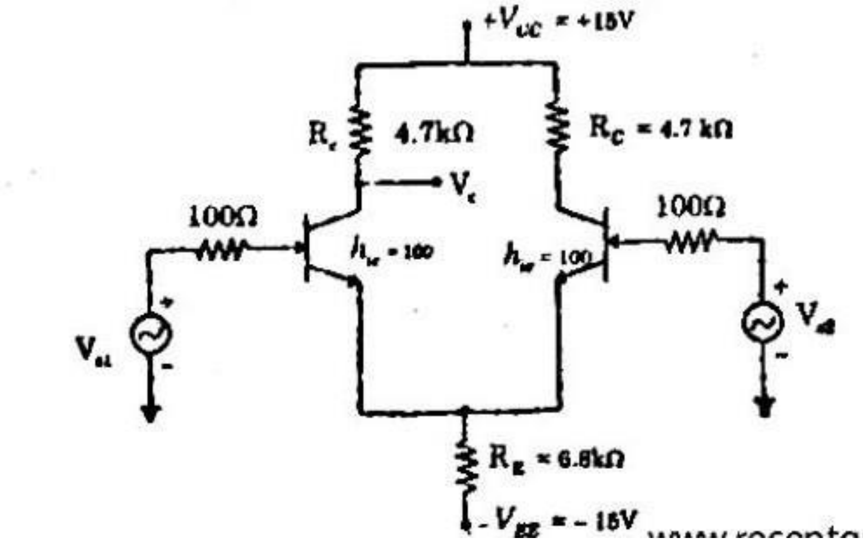
$= \frac{\pi}{4} \frac{V_m}{V_{CC}} * 100$ ……..(13)

- **Maximum efficiency:**
  - ✓ As the peak value of the collector voltage V_m increases, the efficiency also increases.
  - ✓ Then the maximum value of V_m is possible which is equal to V_{CC}.

$\%\eta_{max} = \frac{P_{ac}}{P_{dc}} * 100$

$= \frac{\pi}{4} \frac{V_m}{V_{CC}} * 100 = 78.5\%$

13. Evaluate the (1) operating point (2)differential gain(3)common mode gain(4)CMRR and (5)output voltage if Vs1=70mV peak to peak at 1 Khz and Vs2=40 mV peak to peak at 1 Khz of dual input balanced output differential amplitude h_{ie}=2.8 KΩ.(Nov/Dec 2016)



1. Operating point value are I_{CQ}, V_{CEQ}. Apply KVL to input side.

$$-I_B R_S - V_{BE} - 2R_E I_E + V_{EE} = 0$$

$$\frac{-I_E}{\beta} R_S - V_{BE} - 2R_E I_E + V_{EE} = 0$$

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E + \frac{R_S}{\beta}}$$

$$\beta = h_{fe} = 100$$

$$I_E = \frac{15 - 0.7}{2 \times 6.8 \times 10^3 + \frac{100}{100}} = 1.051\, mA$$

$$I_C = I_E = 1.051\, mA$$

$$V_{CE} = V_{CC} + V_{BE} - I_C R_C = 15 + 0.7 - 1.051 \times 10^{-3} \times 4.7 \times 10^3$$

$$\therefore V_{CEQ} = 10.758\, V$$

Differential gain, A_d $= \frac{h_{fe} R_C}{R_s + h_{ie}}$

$$A_d = \frac{100 \times 4.7 \times 10^3}{100 + 2.8 \times 10^3} = 162.068$$

Common mode gain, A_c $= \frac{h_{fe} R_c}{2R_E(1+h_{fe}) + R_s + h_{ie}}$

$$A_C = \frac{100 \times 4.7 \times 10^3}{2 \times 6.8 \times 10^3 (1 + 100) + 100 + 2.8 \times 10^3}$$

$$CMRR = \frac{A_d}{A_c} = \frac{162.068}{0.3414} = 474.652$$

$$\therefore CMRR = 20\log(474.652) = 53.527\ dB$$

Output voltage, $V_o = A_d V_d + A_c V_c$

$$V_d = V_{s1} - V_{s2} = 70 - 40 = 30\ mV\ (P-P)$$

$$V_c = \frac{V_{s1} + V_{s2}}{2} = \frac{70+40}{2} = 55\ mV\ (P-P)$$

$$V_o = 162.068 \times 30 \times 10^{-3} + 55 \times 10^{-3} \times 0.3414$$

$$= 4.86204 + 0.0187$$

$$= 4.88\ V\ (Peak - Peak)$$

14. A parallel resonant circuit has a capacitor of 250 pF in one branch and inductance of 1.2 mH and a resistance of 10Ω in parallel branch. Find (1). Resonant frequency (2). Impedance of the circuit at resonance (3). Q-factor of the circuit. **(Nov/Dec 2018)**

Solution:

i. Resonant frequency of the parallel tuned circuit is defined as,

$$f_r = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{R^2}{L^2}}$$

$$f_r = \frac{1}{2\pi}\sqrt{\frac{1}{1.25\ X\ 10^{-3}\ X\ 250\ X\ 10^{-12}} - \frac{10\ X\ 10}{(1.25\ X\ 10^{-3})^2}}$$

$f_r = \frac{1}{2\pi}$ X 178836.493 = 284.7 X 10^3 Hz

$$\boxed{\mathbf{f_r = 284.7\ KHz}}$$

ii. Impedance of the circuit, Z_r is given by,

$$Z_r = \frac{L}{RC} = \frac{1.25\ X\ 10^{-3}}{250\ X\ 10^{-12}\ X\ 10}$$

Z_r = 500000

$$\boxed{\mathbf{Z_r = 500\ K\Omega}}$$

iii.Q-factor of the circuit is defined as,

$$Q = \frac{2\pi f_r L}{R} = \frac{2\pi\ X\ 284.7\ X\ 10^3 X\ 1.25\ X\ 10^{-3}}{10} = \frac{2236.02}{10} = 223.6$$

$$\boxed{\mathbf{Q = 223.6}}$$

15. Compare voltage and power amplifiers. (Nov/Dec 2018)

Voltage Amplifier		Power Amplifier	
1.	The amplitude of input A.C signal is small	1.	The amplitude of A.C signal is large.
2.	The collector current is low (about 1 mA)	2.	The collector current is very high (greater than 100 mA)
3.	RC coupling is used.	3.	Transformer coupling is used
4.	The A.C power output is low	4.	The A.C power output is high
5.	Heat dissipation is less	5.	Heat dissipation is high
6.	The size of power transistor is small	6.	The size of power transistor is large
7.	Current gain is low	7.	Current gain is high
8.	Output impedance is high	8.	Output impedance is low

16. Explain the self-biasing of a JFET. (Nov/Dec 2018)

- Self-bias is the most common type of JFET bias. Recall that a JFET must be operated such that the gate source junction is always reverse-biased.
- The condition requires a negative V_{GS} for an n-channel JFET and a positive V_{GS} for p-channel JFET. This can be achieved using the self-bias arrangement shown in Fig.1
- The gate resistor, R_G, does not affect the bias because it has essentially no voltage drop across it; and therefore the gate remains at 0 V.
- R_G is necessary only to isolate an A.C. signal from ground in amplifier applications.
- The voltage drop across resistor, R_S makes gate source junction reverse biased.

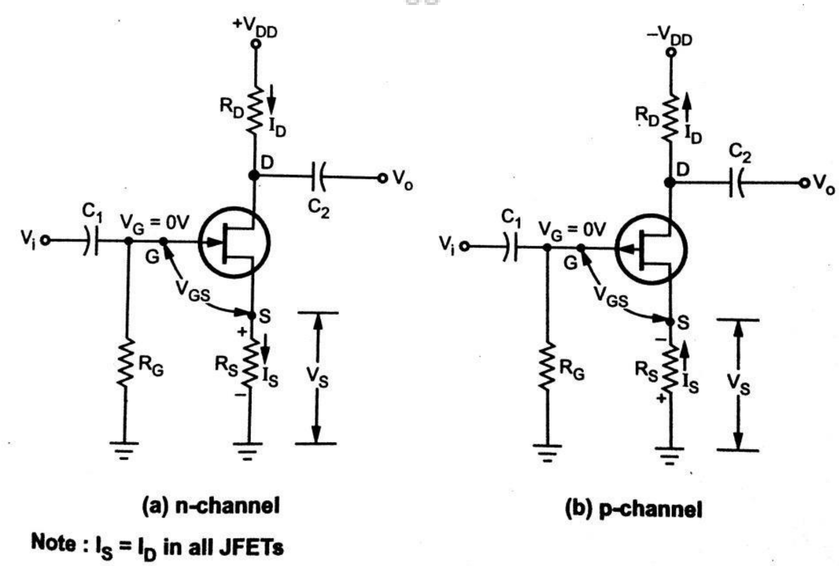


Fig 1: self-bias circuit for JFET

Step 1: Obtain expression for V_{GS}

- For the n-channel FET in Fig. 1(a), I_S produces a voltage drop across R_S and makes the source positive with respect to ground. Since $I_S = I_D$ and $V_G = 0$, then $V_S = I_S R_S = I_D R_S$. The gate to source voltage is,
  $V_{GS} = V_G – V_S = 0 – I_D R_S = - I_D R_S$
- For the p-channel FET in Fig. 1(b), I_S produces a voltage drop across R_S and makes the source negative with respect to ground. Since $I_S = I_D$ and $V_G = 0$, then $V_S = - I_S R_S = -I_D R_S$ the gate to source voltage is
  $V_{GS} = V_G – V_S = 0 – (-I_D R_S) = + I_D R_S$

- In the following D.C. analysis, the n-channel JFET shown in Fig. 1(a) is used to for illustration.
- For D.C. analysis we can replace coupling capacitors by open circuits and we can also replace the resistor R_G by a short circuit equivalent, since $I_G = 0$. This is illustrated in Fig.2.

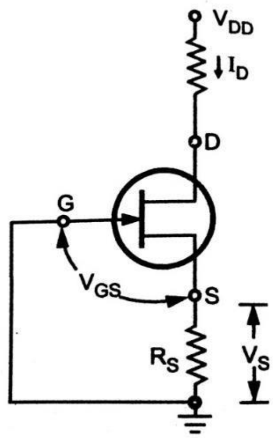


Fig 2: Simplified self-bias circuit for dc analysis

Step 2: Calculate I_{DQ}

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

Substituting value of V_{GS} in above equation we get,

$$I_D = I_{DSS}\left[1 - \frac{-I_D R_S}{V_P}\right]^2 = I_{DSS}\left[1 + \frac{I_D R_S}{V_P}\right]^2$$

Step 3: Calculate V_{DS}

Applying KVL to the output circuit we get,

$$V_S + V_{DS} + I_D R_D - V_{DD} = 0$$

$$V_{DS} = V_{DD} - V_S - I_D R_D = V_{DD} - I_D R_S - I_D R_D = V_{DD} - I_D(R_S + R_D)$$

EC8353-ELECTRON DEVICES AND CIRCUITS

UNIT-V FEEDBACK AMPLIFIERS AND OSCILLATORS

PART-A

FEEDBACK AMPLIFIERS

1. Define feedback and feedback factor. Define Positive feedback and Negative feedback.

Feedback: The process of *injecting a fraction of the output voltage of an amplifier into the input* so that it becomes a part of the input is known as feedback.

Feedback Factor: Feedback factor is defined as the ratio of feedback signal (Voltage/Current) to the amplifier output which is given as input to the feedback network. Hence, it is also called as feedback ratio and is denoted by β.

i.e., $\beta = \frac{V_f}{V_o}$; $V_f - Feedback\ Voltage$ $V_O - Amplifier\ Output\ Voltage$

Positive feedback: If the *feedback voltage is in-phase to the input from the source*, i.e., feedback signal in-phase with the original input signal. It is called positive feedback.

Negative feedback: If the *feedback voltage is opposite (out of phase) to the input from the source*, i.e., feedback signal opposes the original input signal. It is called negative or degenerative feedback.

Advantages of negative feedback

2. Mention/List the advantages of negative feedback circuits. (Nov/Dec2015), (May/June2016)

- In negative feedback amplifiers, the **voltage gain** of the amplifier remains **stable**.
- High input resistance of a voltage amplifier can be made larger
- Low output resistance of a voltage amplified can be lowered
- Frequency response improves
- Significant improvement in the linearity of operation
- The transfer gain of the amplifier with feedback can be stabilized against variation in the h parameters.

3. Write the disadvantages of negative feedback in amplifier circuits and how it can be overcome? (April/May 2015)

The main **disadvantage** of using negative or degenerative feedback in amplifier is ***Reduction*** *in* ***Gain***.
The required Gain can be attained by increasing the number of amplifier stages

4. What are the effects of a negative feedback?

a) Reduces noise
b) Reduces distortion
c) Reduces gain
d) Increases band width
e) The gain becomes stabilized with respect to changes in the amplifier active device parameters like h_{fe}.
f) The non-linear distortion is reduced there by increasing the signal handling capacity or the dynamic range of the amplifier.

5. What is the condition required for satisfactory operation of a negative feedback amplifier? (April/May 2019)

The open-loop voltage gain must be much greater than the required closed-loop gain.

Overall Voltage Gain with -ve feedback (Closed-loop Gain), $A_{vf} = \frac{A_v}{1+\beta A_v}$

$$A_{vf} = \frac{A_v}{\beta A_v} \qquad \{Since, \beta A_v \gg 1\}$$

Therefore, $A_{vf} = \frac{1}{\beta}$

{Where A_v is the voltage gain without a feedback and β is the feedback factor is due to negative feedback the gain is reduced by factor $1 + \beta A_v$}

6. **With negative feedback the bandwidth of the amplifier increases- True/False?**
   True.
   Bandwidth of amplifier with feedback is greater than bandwidth of amplifier without feedback.

Voltage / current, Series, Shunt feedback

7. **Mention the four connections in Feedback.**
   a. Voltage series feedback.
   b. Voltage shunts feedback.
   c. Current series feedback.
   d. Current shunt feedback.

8. **Explain the voltage series feedback.**
   In this case, the feedback voltage is derived from the output voltage and fed in series with input signal. The input of the amplifier and the feedback network are in series is also known as series parallel in parallel, hence this configuration is also known as series parallel feedback network.

9. **Explain the voltage shunt feedback.**
   The input of amplifier and the feedback network are in parallel and known as parallel –parallel feedback network. This type of feedback to the ideal current to voltage converter, a circulating having very low input impedance and very low output impedance.

10. **Explain the current series feedback.**
    When the feedback voltage derived from the load current and is fed in series with the input signal, the feedback is said to be current series feedback, the inputs of the amplifier and the feedback network are in series and the output are also in series. This configuration is also called as series-series feedback configuration.

11. **Explain the current shunt feedback.**
    When the feedback voltage is derived from the load current and a fed in parallel with the input signal, the feedback is said to be current shunt feedback. Here in the inputs of the amplifier and the feedback network are in parallel and the outputs are in series. This configuration is also known as parallel series feedback.

12. **Which is the most commonly used feedback arrangement in cascaded amplifier and why? (Nov/Dec-2013-R13)**
    A voltage series feedback s commonly used in cascaded amplifiers. Since, it has high input impedance and low output impedance that is needed for cascaded amplifiers.

Positive feedback (Oscillators)

13. **What is Oscillator?**
    Oscillator is an electronic device which generates electrical oscillations (i.e., repeated waveforms) of required frequency. It is used for converting DC energy into AC energy of the desired frequency.
    {An oscillator is a circuit which generates an alternating voltage without any input signal. Instead of external input signal, it uses feedback path through which it provides its own input signal.
    It is used for converting DC energy into AC energy of the desired frequency.}

14. **What are sustained Oscillations?**
    Electrical oscillations in which amplitude does not change with time are called sustained oscillations. It is called as un-damped oscillations.

15. **What is frequency of Oscillations?**
    The frequency at which circuit satisfies both the Barkhausen conditions i.e. $|A\beta| = 1$ and $\angle A\beta = 0°$ or $360°$ simultaneously is called frequency of oscillations

16. **Classify the various oscillators based on the output waveforms, circuit components, operating frequencies and feedback used.**
    According to the *nature of waveform generated*.
    1. *Sinusoidal or Harmonic Oscillators*
    2. *Non-sinusoidal or Relaxation oscillators*

Based on circuit components. (Nov/Dec 2017)

According to the frequency determining networks,

1. RC oscillators (Phase-shift Oscillator and Wien Bridge Oscillator)
2. LC oscillators (Hartley Oscillator and Colpitts Oscillator)
3. Crystal oscillators

According to the frequency of the Generated Signals

1. AFO (Audio Frequency Oscillators) – upto 20 KHz
2. RFO (Radio Frequency Oscillators) – 20 KHz to 30 MHz
3. VHFO (Very High Frequency Oscillators) - 30 MHz to 300 MHz
4. UHFO (Ultra High Frequency Oscillators) - 300 MHz to 3 GHz
5. MFO (Microwave Frequency Oscillators) – above 3 GHz

17. What are the types of sinusoidal oscillator? [or] Mention the different types of sinusoidal oscillator?

a) RC phase shift Oscillator.
b) Wein bridge Oscillator.
c) Hartley Oscillator
d) Colpitts Oscillator
e) Crystal Oscillator

18. Name two low frequency oscillators?

a) RC phase shift oscillator.
b) Wein bridge oscillator.

19. Name three high frequency oscillators?

The high frequency oscillators are

a) Hartley oscillator.
b) Colpitts oscillator.
c) Crystal oscillator

Condition for oscillations

20. Write the conditions for a Oscillator. (OR)
State. Barkhausen criterion (Barkhausen condition) for sustained oscillations. (Nov/Dec-2012,2011,09), (May/June2016) (Nov/Dec-2016) (May 2017)

The Barkhausen criterion for obtaining sustained oscillations,

1. The feedback voltage must be in-phase with the input, i.e., total phase-shift around the closed-loop must be 0° or 360°, and
2. Magnitude of the loop gain must be unity i.e., $|A\beta| = 1$

Where, A – Open loop Gain of the system & β – Feedback ratio.

Phase Shift and Wien bridge oscillator (RC oscillators)

21. Why an RC phase shift oscillator is called so?

An RC network products 180º phase shift. Hence it is called RC phase shift oscillator.

22. List the advantages of phase shift oscillator. (May/June-2012)

- The phase shift oscillator does not required conductance or transformers.
- It is suitable for the low frequency range i.e., from a few hertz to several 100 kHz. The upper frequency is limited because the impedance of RC network may become so small that it loads the amplifier heavily.

23. Write the disadvantages of Phase shift oscillator.

1. It is necessary to change the C or R in all the three RC networks simultaneously for changing the frequency of oscillations. This is practically difficult.
2. It is not suitable for high frequencies.

24. Which oscillator uses both positive and negative feedback?
Wien bridge oscillator.

Hartley and Colpitts oscillators. (LC oscillators)

25. Distinguish between LC and RC oscillator.

LC Oscillator	RC Oscillator
It operates at high frequencies	It operates at low frequencies
It is suitable for RF only	It is suitable for AF only
Frequency is variable	The frequency is constant. It is known as fixed frequency oscillator.

26. Write the main drawback of LC oscillators.

1. The frequency stability is not very good.
2. They are too bulky and expensive and cannot be used to generate low frequencies.

27. What is the advantage of a colpitts oscillator compared to a phase shift oscillator? (Nov/Dec 2015)

ii) The advantage of colpitts oscillator is the frequency of oscillation is very high.
iii) We can vary the frequency of oscillation.

Crystal oscillators.

28. What is piezo electric effect? (May/June-2013)
The piezo electric crystal exhibits a property, that is, if a mechanical stress is applied across one face, an electrical potential is developed across the opposite face. The inverse is also true. This phenomenon is called piezo-electric effect.

29. Why Quartz crystal is commonly used in crystal oscillator?
Quartz crystals are generally used in crystal oscillator because of their great mechanical strength, simplicity of manufacture and abeyance to the piezo electric effect accurately.

30. What are the advantages of crystal oscillators? (NOV/DEC 2012)
The advantages of crystal oscillators are

a) Excellent frequency stability.
b) High frequency of operation
c) Automatic amplitude control.
d) It is suitable for only low power circuits
e) Large amplitude of vibrations may crack the crystal.
f) It large in frequency is only possible replacing the crystal with another one by different frequency.

31. An oscillator operating at 1 MHz has a stability of 1 in 10^4. What will be the minimum value of frequency generated? (April/May 2019)
The typical frequency stability of oscillators that do not use CRYSTAL is about 1 in 10^4.
The minimum value of frequency generated might be 100KHZ *or lower than* 1MHZ *for the oscillator operating at* 1MHZ.
{If the crystal is used, the frequency stability can be improved to better than 1 in 10^6, which gives a ±1 Hz variation in the output of a 1 MHz oscillator.}

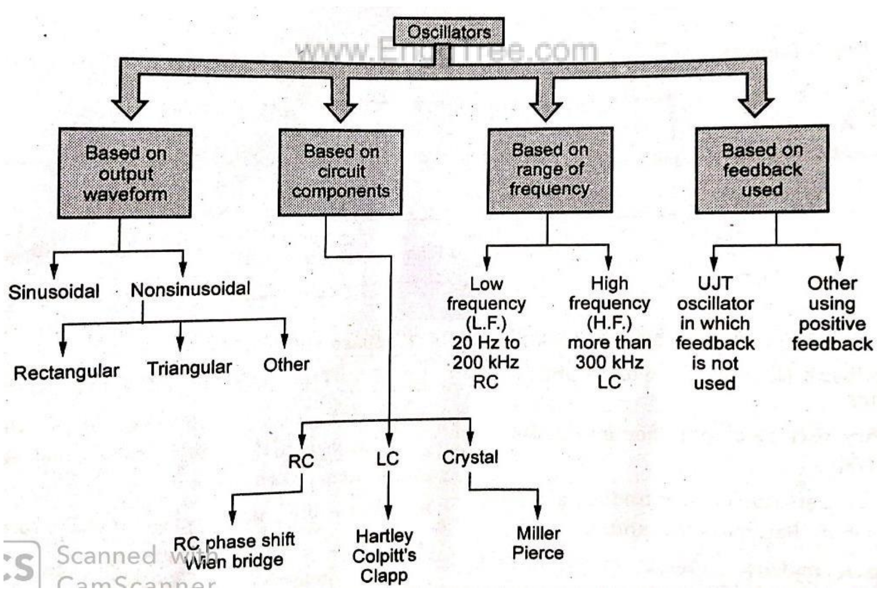
32. How does an oscillator differ from an amplifier? (or) Differentiate oscillator & amplifier. [Nov/Dec 2013] [Nov/Dec 2016]

S.No.	Oscillators	Amplifiers
1	They are self-generating circuits. They generate waveforms like sine, square and triangular waveforms of their own without having input signal.	They are not self-generating circuits. They need a signal at the input and they just increase the level of the input waveform.
2	It has infinite gain	It has finite gain
3	Oscillator uses positive feedback.	Amplifier uses negative feedback.

33. Compare RC Phase-Shift Oscillators and Wien Bridge Oscillator.

Sr. No.	RC phase shift oscillator	Wien bridge oscillator
1.	It is a phase shift oscillator used for low frequency range.	It is also a phase shift oscillator used for low frequency range.
2.	The feedback network is RC network with three RC sections.	The feedback network is lead-lag network which is called Wien bridge circuit.
3.	The feedback network introduces 180° phase shift.	The feedback network does not introduce any phase shift.
4.	Op-amp is used in an inverting mode.	Op-amp is used in non-inverting mode.
5.	Op-amp circuit introduces 180° phase shift.	Op-amp circuit does not introduce any phase shift.
6.	The frequency of oscillations is, $f = \frac{1}{2\pi RC\sqrt{6}}$	The frequency of oscillations is, $f = \frac{1}{2\pi RC}$
7.	The amplifier gain condition is, $\lvert A \rvert \geq 29$	The amplifier gain condition is, $\lvert A \rvert \geq 3$
8.	The frequency variation is difficult.	Mounting the two capacitors on common shaft and varying their values, frequency can be varied.

34. Classification of Oscillators



PART-B

Advantages of negative feedback & positive feedback

1. What is meant by feedback? What are the types of feedback and effects of negative feedback? (May/June-2012) (Nov/Dec 2017)

Negative feedback

If β is negative, the voltage feedback subtracts from the input yielding a lower output and reduced voltage gain. Hence this feedback is known as negative feedback.

Positive feedback

If the phase of the voltage feedback is such as to increase the input, then β is positive and the result is positive feedback.

Increase Stability:

The voltage gain due to a negative feedback is given by

$$A_{vf} = \frac{A_v}{1+\beta A_v} \ldots\ldots\ldots\ldots\ldots..(1)$$

Where A_v is the voltage gain without a feedback and β is the feedback factor is due to negative feedback the gain is reduced by factor $1+\beta A_v$

If $\beta A_v >> 1$ then $A_{vf} = \frac{A_v}{\beta A_v} = \frac{1}{\beta}$

Hence the gain of the amplifier with feedback has been stabilized against such problems as ageing of a transistor or a transistor being re-placed by a transistor with a different value of β.

Sensitivity of transfer gain:

The fractional change in amplification with feedback divided by the fractional change without feedback is called the sensitivity of the transfer gain

From equ 1

$$\frac{dA_{vf}}{dA_v} = \frac{(1+\beta A_v)-A_v\beta}{(1+\beta A_v).^2} = \frac{1}{(1+\beta A_v).^2}$$

$$\frac{dA_{vf}}{dA_v} = \frac{1}{((1+\beta A_v)^2)}$$

$$dA_{vf} = \frac{dA_v}{(1+\beta A_v)^2}$$

Dividing both side by A_{vf}

$$\frac{dA_{vf}}{A_{vf}} = \frac{dA_v}{((1+\beta A_v)^2).A_{vf}}$$

Instead of A_{vf} sub $\frac{A_v}{1+\beta A_v}$ in above equation

$$\frac{dA_{vf}}{A_{vf}} = \frac{dA_v}{((1+\beta A_v)^2).(\frac{A_v}{1+\beta A_v})}$$

$$= \frac{dA_v}{A_v(1+\beta A_v)}$$

Taking absolute value of the resultant equation we get

$$\frac{dA_{vf}}{A_{vf}} = \frac{1}{|1+\beta A_v|}\left|\frac{dA_v}{A_v}\right| \ldots\ldots\ldots\ldots\ldots..3$$

$$\text{Sensitivity} = \frac{\left|\frac{dA_{vf}}{A_{vf}}\right|}{\left|\frac{dA_v}{A_v}\right|} = \frac{1}{|1+\beta A_v|} \ldots\ldots\ldots\ldots\ldots\ldots 4$$

The densitivity is reciprocal of sensitivity. Hence

$$D = 1 + A_v\beta \ldots\ldots\ldots\ldots\ldots\ldots 5$$

Frequency distortion

From equ 1 we find that for a negative feedback amplifier having $A_v\beta >> 1$ the gain withfeedback is $A_{vf}=1/\beta$. If the feedback network does not contain any reactive elements the gain is not function of frequency.

Reduction in noise

There are many sources of noise is an amplifier. If the noise present at the output is N and the amplifier gain is A. then the noise present in the amplifier with negative feedback is

$$N1 = \frac{N}{1+\beta A_v}.$$

Reduction in distortion

Let us assume that the distortion in the absence of feedback is D. Because the effect of feedback the distortion present at the input is equal to

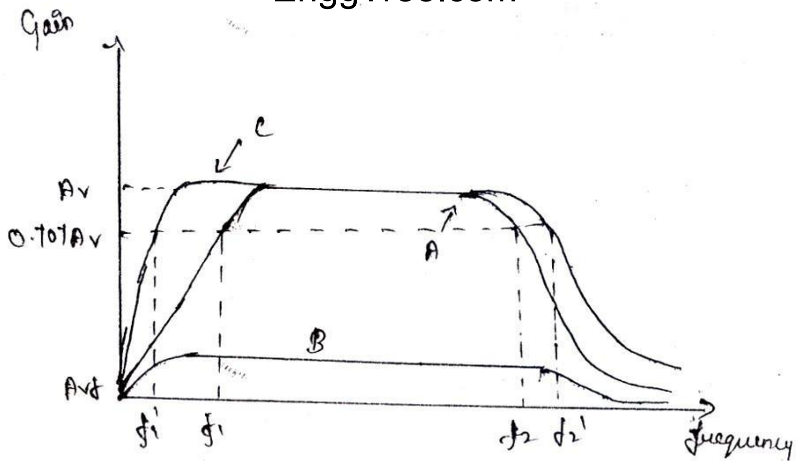
$$D_f = \frac{D}{1+\beta A_v}$$

Bandwidth

If the bandwidth of an amplifier without feedback is given by

$Bw_f = BW(1+\beta A_v)$

In curve a source the frequency response of an amplifier without feedback when a negative feedback is introduced the gain of the amplifier decreases.



Frequency response of an amplifier with and without feedback

Obtain curve C. from fig we can observe that there is decrease in the lower cutoff frequency and increase in upper cutoff frequency hence the bandwidth increases. Therefore β increases Bandwidth also increases ***Loop Gain***

A loop gain is used to describe the product of voltage gain A_v and feedback factor β. The amount of feedback introduced into an amplifier may be expressed in decibels according to the following definition.
F=feedback in db

$$= 20\log\frac{A_{vf}}{A_v}$$

$$= 20\log\frac{1}{1+\beta A_v}$$

2. Advantages of Negative feedback in amplifiers. (Nov/Dec 2018)

The advantages of negative feedback in amplifiers are listed as follows.

1. The negative feedback amplifiers, the voltage gain of an amplifier remains stable.
2. It reduces the non-linear distortion produced in large signal amplifiers.
3. It improves the frequency response of the amplifier.
4. It increases the stability of the circuit.
5. Negative feedback increases the input impedance and decreases the output impedance of the amplifier.
6. It decreases the noise voltage in the amplifier.
7. Negative feedback amplifier is less sensitive to variations in amplifier parameters.
8. It increases the amplifier bandwidth.
9. The input and output impedances of feedback amplifier can be adjusted to desired value.
10. It has less phase, amplitude and frequency distortion.
11. Amplifier with negative feedback operates linearly.
12. Operating point of amplifier can be stabilized.

3. With proper mathematical derivation, proven that bandwidth increases in a negative feedback amplifier. (April/May 2019)

The negative feedback increases amplifier bandwidth which can be proven mathematically as below

ADDITIONAL EFFECTS OF NEGATIVE FEEDBACK

Decibels of Feedback

Negative feedback can be measured in decibels. A statement that 40 dB of feedback has been applied to an amplifier means that the amplifier gain has been reduced by 40 dB (that is, by a factor of 100). Thus,

$$A_{CL} = A_v - 40\text{ dB} = \frac{A_v}{100}$$

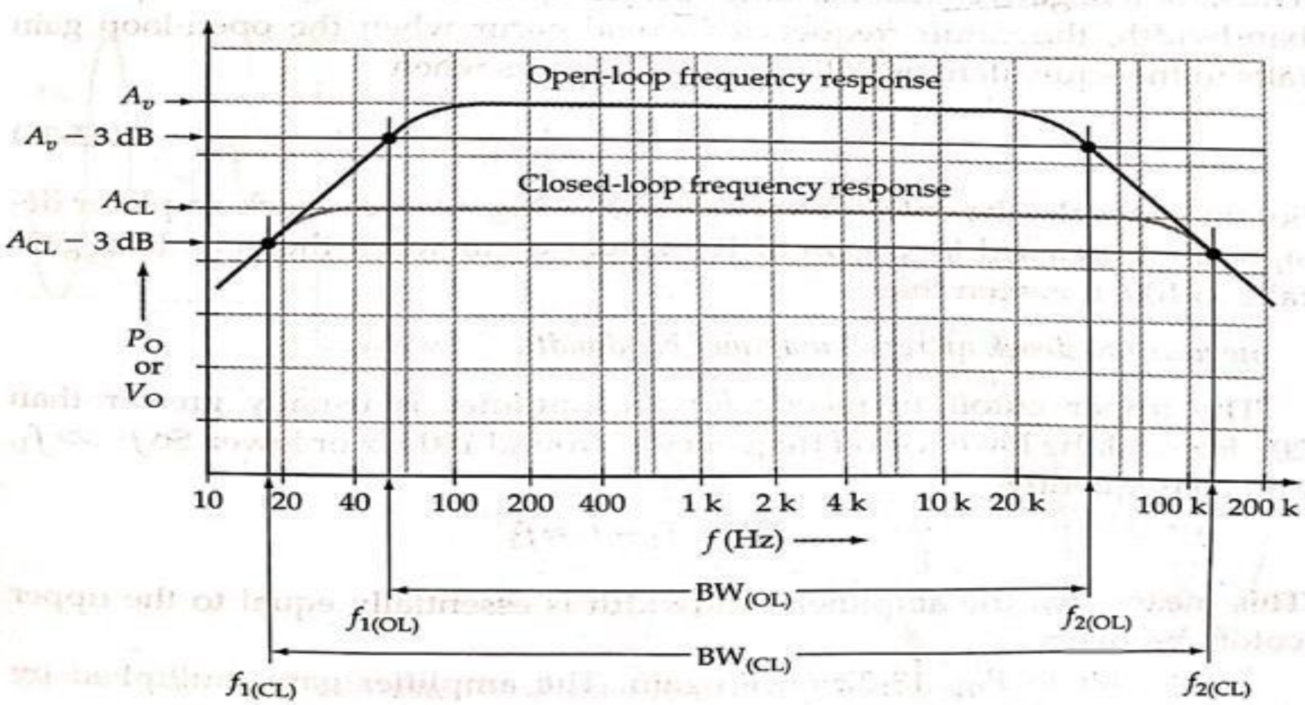
Bandwidth

Consider the typical gain-frequency response of an amplifier, as illustrated in Fig. . Without negative feedback, the amplifier open-loop gain (A_v) falls off to its lower 3 dB frequency ($f_{1(OL)}$), as illustrated. This is usually due to the impedance of bypass capacitors increasing as the frequency decreases. Similarly, the open-loop upper cutoff frequency ($f_{2(OL)}$) is produced by transistor cutoff, by shunting capacitance, or by a combination of both.

the circuit open-loop bandwidth is given by

$$BW_{OL} = f_{2(OL)} - f_{1(OL)}$$

Now look at the typical frequency response for the same amplifier when negative feedback is used. The closed-loop gain (A_{CL}) is much smaller than the open-loop gain, and A_{CL} does not begin to fall off (at high or low frequen-



Amplifier frequency response with and without negative feedback. Negative feedback extends the amplifier bandwidth.

cies) until A_v (open-loop gain) falls substantially. Consequently, $f_{1(CL)}$ is much lower than $f_{1(OL)}$, and $f_{2(CL)}$ is much higher than $f_{2(OL)}$. So the circuit bandwidth with negative feedback (the closed-loop bandwidth) is much greater than the bandwidth without negative feedback.

$$BW_{CL} = f_{2(CL)} - f_{1(CL)}$$

$$A_{CL} = \frac{A_v}{1 + A_v B}$$

It can be shown that there is a 90° phase shift associated with the open-loop gain at frequencies below $f_{1(OL)}$ and above $f_{2(OL)}$. Thus, above Eq. must be rewritten as

$$A_{CL} = \frac{-jA_v}{1 - jA_v B}$$

or
$$|A_{CL}| = \frac{A_v}{\sqrt{[1 + (A_v B)^2]}}$$

When $A_v = 1/B$,

$$|A_{CL}| = \frac{1/B}{\sqrt{[1 + 1]}} = \frac{A_{CL}}{\sqrt{2}}$$
$$= A_{CL} - 3\text{ dB}$$

Thus, for a negative feedback amplifier designed to have the widest possible bandwidth, the cutoff frequencies would occur when the open-loop gain falls to the equivalent of $1/B$. Thus, $f_{2(CL)}$ occurs when

$$A_v = 1/B \approx A_{CL}$$

So, for example, the cutoff frequencies for a negative feedback amplifier designed for a closed-loop gain of 100 would occur when the open-loop gain falls to 100. It is seen that

negative feedback increases amplifier bandwidth.

The upper cutoff frequency for an amplifier is usually greater than 20 kHz, and the lower cutoff frequency is around 100 Hz or lower. So $f_2 \gg f_1$, and consequently,

$$BW = f_2 - f_1 \approx f_2$$

This means that the amplifier bandwidth is essentially equal to the upper cutoff frequency.

Now refer to Fig. once again. The amplifier gain multiplied by the upper cutoff frequency is a constant quantity. This is known as the *gain-bandwidth product*. Therefore,

$$A_{CL} \times f_{2(CL)} = A_v \times f_{2(OL)}$$

or
$$f_{2(CL)} = \frac{A_v f_{2(OL)}}{A_{CL}} \qquad \textbf{(13-27)}$$

Thus the closed-loop upper cutoff frequency for a negative feedback amplifier can be calculated from the open-loop upper cutoff frequency, the open-loop gain, and the closed-loop gain.

TYPES OF NEGATIVE FEEDBACK AMPLIFIER

4. Explain the various types of feedback amplifier (May 2017)

(OR)

With a neat block diagram, explain the operation of Current Shunt Feedback Amplifier.

(OR)

Determine R_{if}, R_{of}, A_v, A_{vf} for the following feedback amplifier

A. Voltage series feedback amplifier (Series-Shunt feedback amplifier) (Nov/Dec 2016) (May 2017)
B. Current Series Feedback Amplifier (Shunt-Series feedback amplifier)
C. Current Shunt Feedback Amplifier (Series-Series feedback amplifier) (May 2017)
D. Voltage Shunt Feedback Amplifier (Shunt-Shunt feedback amplifier)

(OR)

Discuss the effect of voltage series feedback and derive the expression for input resistance, output resistance and voltage gain.

(OR)

Discuss about the following feedback configurations of amplifiers and obtain the feedback factor and closed loop gain. ***(April/May 2018-R13)***

A. Shunt-Shunt Feed Back
B. Series-Series Feed Back
C. Shunt-Series Feed Back
D. Series-Shunt Feed Back

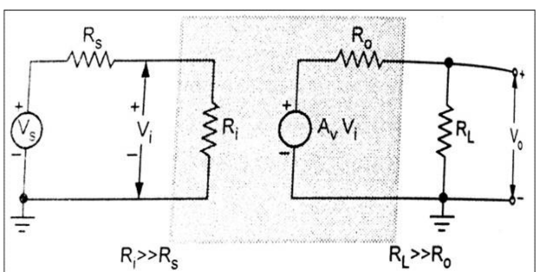
Feedback amplifier, the output signal sampled may be either voltage or current and sampled signal can be mixed either is series or in shunt with the input

The four types of amplifiers, they are

- Voltage series feedback amplifier (Series-Shunt feedback amplifier) **(Nov/Dec 2016) (May 2017)**
- Current Series Feedback Amplifier (Shunt-Series feedback amplifier)
- Current Shunt Feedback Amplifier (Series-Series feedback amplifier) **(May 2017)**
- Voltage Shunt Feedback Amplifier (Shunt-Shunt feedback amplifier)

(A) VOLTAGE SERIES AMPLIFIER:

With proper mathematical derivation, proven that output resistance reduces in a negative feedback amplifier. Assume a series shunt feedback scheme. (April/May 2019)

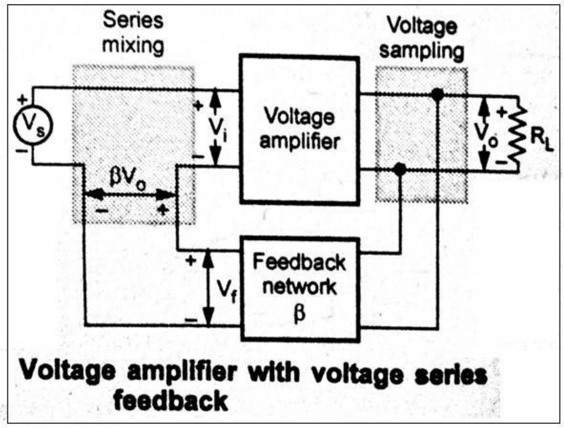


Thevenin's equivalent circuits of a voltage amplifier

- R_i – input resistance
- R_s – source resistance
- R_L – load resistance
- R_O – output resistance
- A_V – voltage gain

- $R_i >> R_S$ then $V_i = V_s$
- $R_L >> R_o$ then $V_o = A_V V_i = A_v V_s$
- Amplifier provides a voltage output proportional to the voltage input
- The proportionality factor does not depend on magnitudes of the source an load resistance
- Hence it is called voltage amplifier

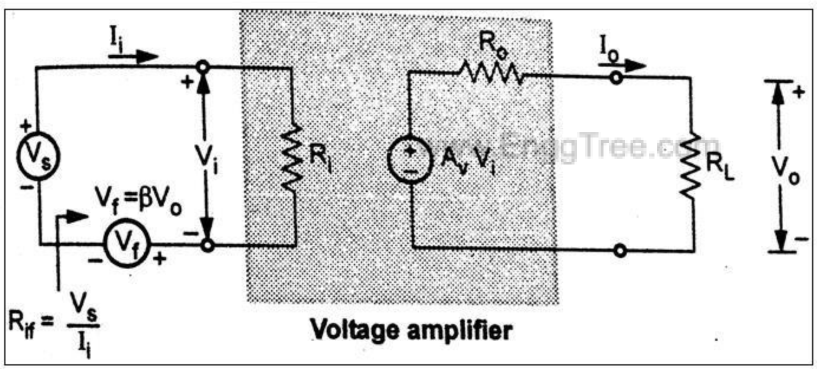
Feedback Topology



Voltage amplifier with voltage series feedback

Input resistance

Step 1: equivalent circuit



Voltage amplifier

Step 2: obtain expression for V_S

Applying KVL to the input side we get,

$V_S - I_i - V_f = 0 \qquad \therefore V_s = I_i R_i + V_f = I_i R_i + \beta V_o$

$\therefore \; V_f = \beta V_o$

Step 3: obtain expression for V_o in terms of I_i

The output voltage V_o is given as

$$V_o = \frac{A_V V_i R_L}{R_O + R_L} = A_V V_i \quad where, \qquad A_v = \frac{A_v R_L}{R_o + R_L}$$

$V_o = A_v I_i R_i \qquad\qquad \therefore V_i = I_i R_i$

Step 4: obtain expression for R_{if}

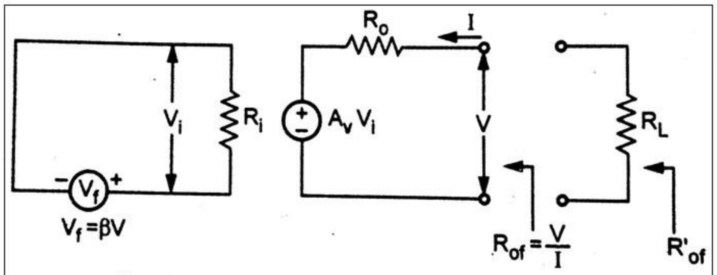
Substituting value of V_0 from above equation we get

$V_S = I_i R_i + \beta A_v I_i R_i$ $\therefore R_{if} = V_s / I_i = R_i + \beta A_v R_i$

$R_{if} = R_i (1+\beta A_v)$

Output Resistance

Step 1: Equivalent circuit



Equivalent circuit with V_s = 0 and R_L disconnected

Step 2: obtain expression for I in terms of V

Applying KVL to the output side we get

$A_v V_i + IR_0 - V = 0$ $\therefore I = \frac{V - A_V V_i}{R_0}$

The input voltage is given as

$V_i = - V_f = -\beta V$ $\therefore V_s = 0$

Substituting the V_i from above equation we get

$$I = \frac{V + A_v \beta V}{R_0} = \frac{V(1 + \beta A_V)}{R_0}$$

Step 3: obtain expression for R_{of}

$$R_{of} = \frac{V}{I} \qquad R_{of} = \frac{R_o}{(1 + \beta A_v)}$$

Step 4: obtain expression for R_{of}'

$$R'_{of} = R_{of} \parallel R_L = \frac{R_{Of} X R_L}{R_{Of} + R_L} = \frac{\left(\frac{R_O}{1+\beta A_V}\right) X R_L}{\frac{R_O}{(1+\beta A_V)} + R_L}$$

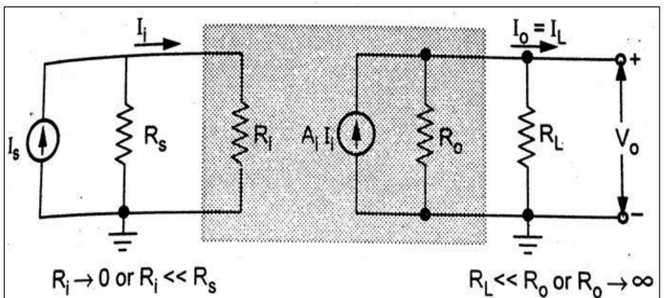
$$= \frac{R_O R_L}{R_O + R_L(1+\beta A_V)} \qquad = \frac{R_O R_L}{R_O + R_L + \beta A_V R_L}$$

Dividing numerator and denominator by $(R_o + R_L)$

$$R'_{of} = \frac{\frac{R_o R_L}{R_o + R_L}}{1 + \frac{\beta A_v R_L}{R_o + R_L}} \quad \therefore R'_o = \frac{R_o R_L}{R_o + R_L} \quad and \quad A_v = \frac{A_v R_L}{R_o + R_L}$$

$$R'_{of} = \frac{R'_o}{1 + \beta A_v}$$

(B)<u>CURRENT SERIES AMPLIFIER:</u>

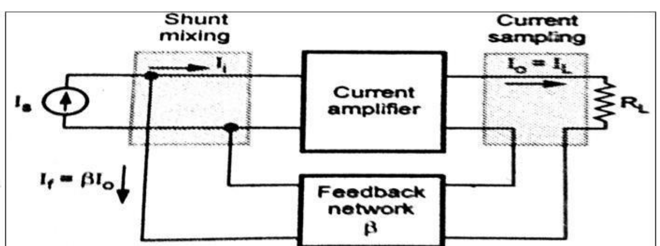


Norton's equivalent circuits of a current amplifier

- R_i – input resistance
- R_s – source resistance
- R_L – load resistance
- R_O – output resistance
- A_I – current gain

- $R_s >> R_i$ and $I_i = I_s$
- $R_o >> R_L$ $\quad I_L = A_I I_i$
- Amplifier provides a current output proportional to the current input
- The proportionality factor does not independent on source and load resistance
- Hence it is called current amplifier

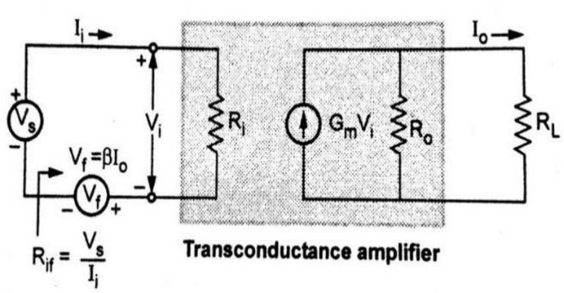
Feedback Topology



Current amplifier with current-shunt feedback

Input Resistance

Step 1: equivalent circuit



Transconductance amplifier

Step 2: obtain expression for V_S

Applying KVL to the input side we get,

$V_S - I_i R_i - V_f = 0 \qquad \therefore V_s = I_i R_i + V_f = I_i R_i + \beta I_o$

$\therefore V_f = \beta I_o$

Step 3: obtain expression for I_o in terms of V_i

The output current I_o is given by

$$I_o = \frac{G_m V_i R_o}{R_o + R_L} = G_M V_i \text{ where } G_M = \frac{G_m R_o}{R_o + R_L}$$

Step 4: obtain expression for R_{if}

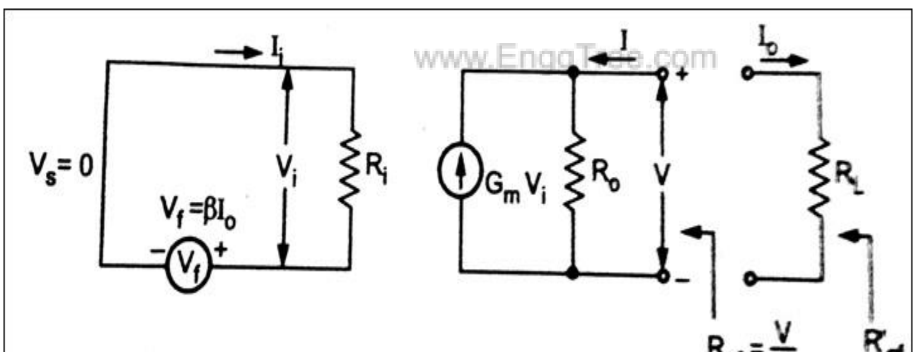
Substituting value of I_o from above equation

$$V_S = I_i R_i + \beta G_M V_i = I_i R_i + \beta G_M I_i R_i \qquad \{\text{Since, } V_i = I_i R_i\}$$

$$R_{if} = V_s / I_i = R_i (1 + \beta G_M)$$

Output Resistance

Step 1: equivalent circuit



Equivalent circuit $V_s = 0$ and R_L disconnected

Step 2: obtain expression for I in terms of V

Applying KVL to the output node we get

$$I = \frac{V}{R_o} - G_m V_i$$

The input voltage is given as $V_i = -V_f = -\beta I_o = \beta I \qquad \therefore I_o = -I$

Substituting value of V_i from above equation we get

$$I = \frac{V}{R_o} - G_m \beta I \qquad \frac{V}{R_o} = I + G_m \beta I = I(1 + G_m \beta)$$

Step 3: obtain expression for R_{of}

$$R_{of} = \frac{V}{I} = R_o(1 + G_m\beta)$$

$$R'_{of} = R_{of} || R_L = \frac{R_{of} \, X \, R_L}{R_{of} + R_L}$$

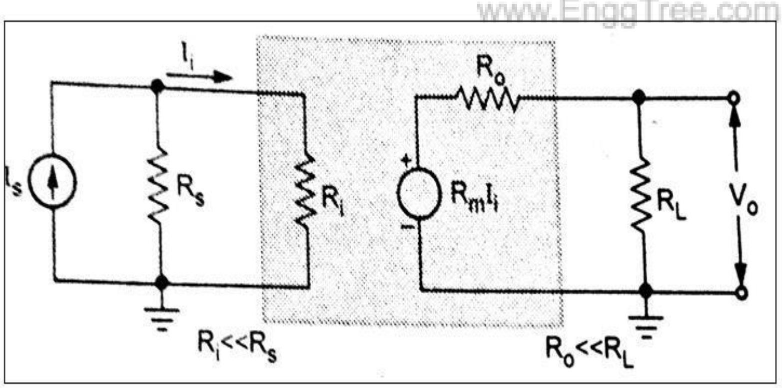
$$= \frac{R_o(1+\beta G_m)R_L}{R_o(1+\beta G_m) + R_L} = \frac{R_o R_L(1+\beta G_m)}{R_o + R_L + \beta G_m R_o}$$

Dividing numerator and denominator by $R_o + R_L$ we get

$$R_{fo} = \frac{\frac{R_L R_o(1+\beta G_m)}{R_o + R_L}}{1 + \frac{\beta G_m R_o}{R_o + R_L}}$$

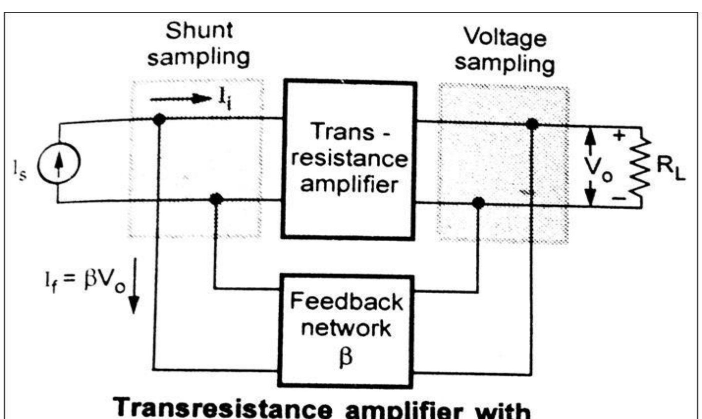
$$R'_{of} = \frac{R'_o(1+\beta G_m)}{1+\beta G_m} \qquad \therefore R'_o = \frac{R_o R_L}{R_o + R_L} \; and \; G_M = \frac{G_m R_o}{R_o + R_L}$$

(C) VOLTAGE SHUNT AMPLIFIER



- $R_i << R_s$ and $R_o << R_s$'
- Since $R_i << R_s$'
- $I_i = I_s$ and $R_o << R_L$, $V_o = R_m I_s$
- Where $R_m = V_o / I_s$ is the transfer or mutual resistance

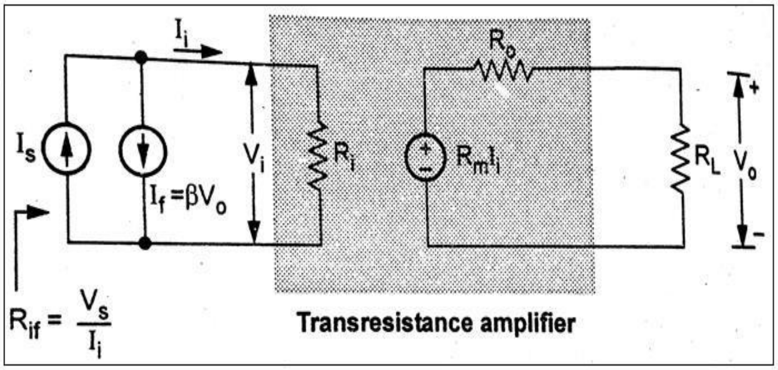
Feedback Topology



Transresistance amplifier with voltage shunt feedback

Input Resistance

Step 1: Equivalent Circuit



Step 2: obtain expression for I_s

Applying KCL at input node we get

$I_s = I_i + I_f = I_i + \beta V_o \qquad \therefore I_f = \beta V_o$

Step 3: obtain expression for R_{if}

The output voltage V_o is given by

$$V_o = \frac{R_m I_i R_o}{R_o + R_L} = R_M I_i \quad \text{where } R_M = \frac{R_m R_o}{R_o + R_L}$$

Step 4: obtain expression for R_{if}

Substituting value of V_o from above equation we get

$I_s = I_i + \beta R_M I_i = I_i (1 + \beta R_M)$

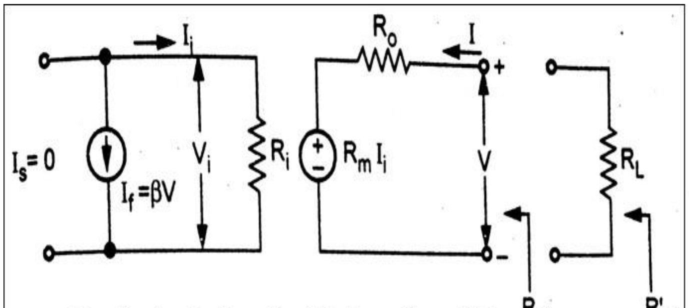
The input resistance with feedback R_{if} is given by

$$R_{if} = \frac{V_i}{I_s} = \frac{V_i}{I_i(1+\beta R_M)} \qquad \therefore R_i = \frac{V_i}{I_i}$$

$$\therefore R_{if} = \frac{R_i}{(1+\beta R_M)}$$

Output Resistance

Step 1: Equivalent Circuit



Equivalent circuit with $I_s = 0$ and R_L disconnected

Step 2: obtain expression for I in terms of V

Applying KVL to the output side we get

$R_m I_i + I R_o - V = 0 \qquad \therefore I = \frac{V - R_m I_i}{R_o}$

The input current is given as

$I_i = - I_f = - \beta V$

Substituting I_i in above equation we get

$$I = \frac{V + R_m \beta V}{R_o} = \frac{V(1 + R_m \beta)}{R_o}$$

Step 4: obtain expression for R'_{of}

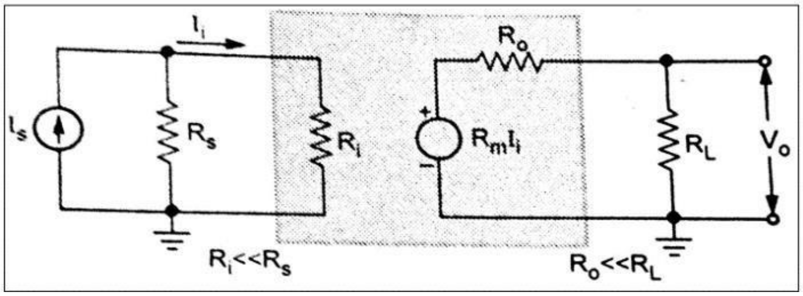
$$R'_{of} = R_{of} || R_L = \frac{R_{of} X R_L}{R_{of} + R_L} = \frac{\frac{R_o X R_L}{1 + R_m\beta}}{\frac{R_o}{1 + R_m\beta} + R_L} = \frac{R_o R_L}{R_o + R_L(1 + R_m\beta)}$$

Dividing numerator and denominator by (R_o + R_L) we get

$$R'_{fo} = \frac{\frac{R_o R_L}{R_o + R_L}}{1 + \frac{\beta R_m R_L}{R_o + R_L}}$$

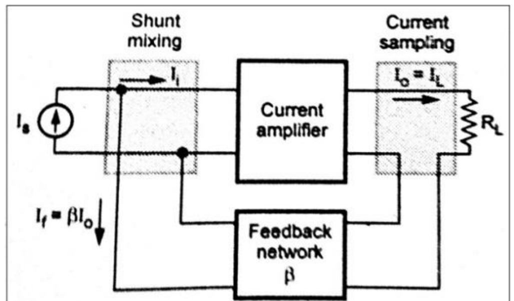
$$R'_{fo} = \frac{R_o^F}{1 + \beta R_M} \quad \text{where } R'_o = \frac{R_L X R_{of}}{R_L + R_{of}} \quad and \quad R_M = \frac{R_m R_L}{(R_o + R_L)}$$

(D) CURRENT SHUNT AMPLIFIER:



- $R_i << R_s$ and $R_o << R_s'$
- Since $R_i << R_s'$
- $I_i = I_s$ and $R_o << R_L$, $V_o = R_m I_s$

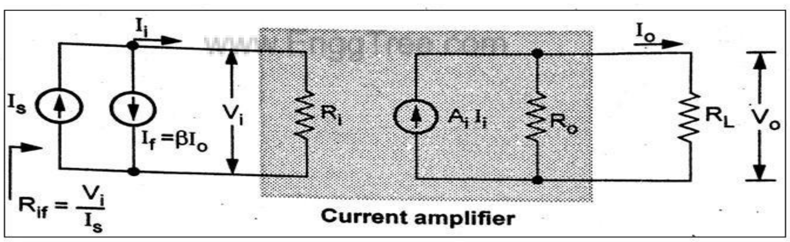
Feedback Topology



Current amplifier with current-shunt feedback

Input Resistance

Step 1: Equivalent Circuit



Step 2: obtain expression for I_s

Applying KCL to the input node we get

$$I_s = I_i + I_f = I_i + \beta\, I_o \quad \therefore I_f = \beta\, I_o$$

Step 3: obtain expression for I_o in terms of I_i

$$I_o = \frac{A_i I_i R_o}{R_o + R_L} = A_I I_i \quad \text{where } A_I = \frac{A_i R_o}{R_o + R_L}$$

Step 4: obtain expression for R_{if}

Substituting value of I_o in above equation we get

$$I_s = I_i + \beta\, A_I\, I_i = I_i\,(1 + \beta\, A_I)$$

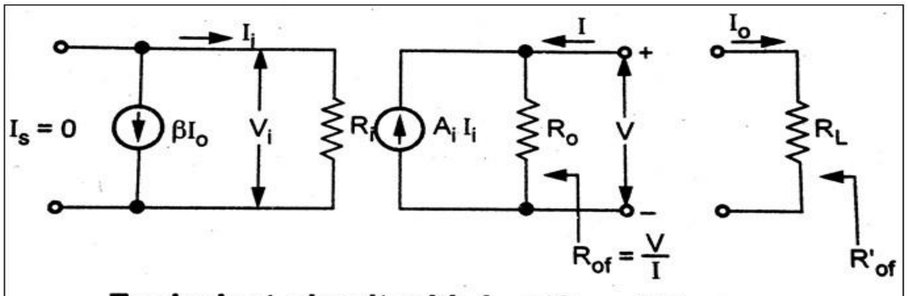
The input resistance with feedback is given as

$$R_{if} = \frac{V_i}{I_s} = \frac{V_i}{I_i(1+\beta A_I)}$$

$$R_{if} = \frac{R_i}{(1+\beta A_I)}$$

Output Resistance

Step 1: Equivalent Circuit



Equivalent circuit with $I_s = 0$ and R_L disconnected

Step 2: obtain expression for I in terms of V

Applying KCL to the output node we get

$$I = \frac{V}{R_o} - A_i I_i$$

The input current is given as

$I_i = - I_f = - \beta I_o \qquad \therefore I_s = 0$

$I_i = \beta I \qquad \therefore I = - I_o$

Substituting value of I_i in above equation we get

$$I = \frac{V}{R_o} - A_i \beta I \qquad \therefore \frac{V}{R_o} = I + A_i \beta = I\,(1+\beta A_i)$$

Step 3: obtain expression for R_{of}

$$R'_{of} = R_{of} || R_L = \frac{R_{of}\ X\ R_L}{R_{of} + R_L}$$

$$= \frac{R_o(1+\beta A_i)R_L}{R_o(1+\beta A_i) + R_L} \qquad \therefore = \frac{R_o R_L(1+\beta A_i)}{R_o + R_L + \beta A_i R_o}$$

Dividing numerator and denominator by $(R_o + R_L)$ we get

$$R'_{of} = \frac{\frac{R_o R_L(1 + \beta A_i)}{R_o + R_L}}{1 + \frac{\beta A_i R_o}{R_o + R_L}}$$

$$R'_{of} = \frac{R'_o(1 + \beta A_i)}{(1 + \beta A_I)}$$

$$R'_o = \frac{R_o R_L}{R_o + R_L} \quad and \quad A_I = \frac{A_i R_o}{R_o + R_L}$$

OSCILLATORS:

5. **Explain the construction and working of the following oscillators and derive the expression for frequency of oscillation. Also, write about advantages and disadvantages.**
    - **A. Phase-Shift Oscillator (RC type Oscillator)**
    - **B. Wein Bridge Oscillator (RC type Oscillator)**
    - **C. Hartley Oscillator (LC type Oscillator)**
    - **D. Colpitts Oscillator (LC type Oscillator)**
    - **E. Crystal Oscillator**

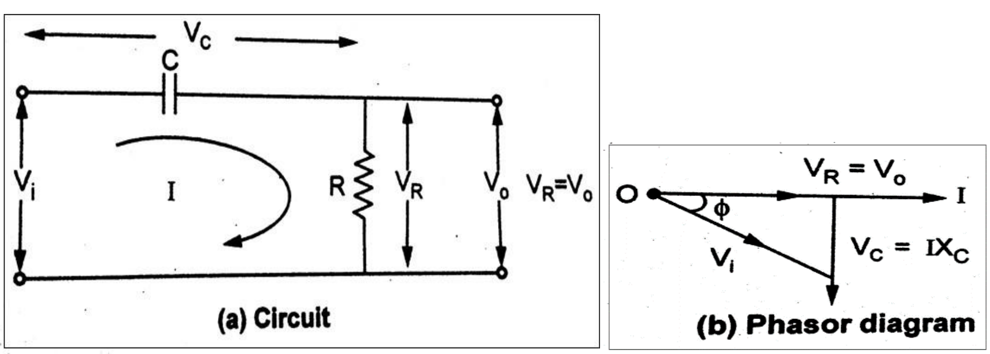
(A) RC Phase Shift Oscillator:

Explain the construction and working of RC Phase-Shift oscillator and derive the expression for frequency of oscillation.

- It consists of an amplifier and feedback network consisting of resistors and capacitors.
- An amplifier can be BJT, FET or operational amplifier.

Analysis of RC circuit:

- In this circuit output is taken across resistor R.



(a) Circuit (b) Phasor diagram

- The capacitive reactance X_C is given by $X_C = \frac{1}{2\pi fC}$ Ω where f is frequency of the input.
- The total impedance of the circuit is,

$$Z = R - jX_C = R - j\left(\frac{1}{2\pi fC}\right) \ \Omega$$

$$= |Z| < -\Phi^0 \quad \Omega$$

- The current ‘I’ flowing in the circuit is,

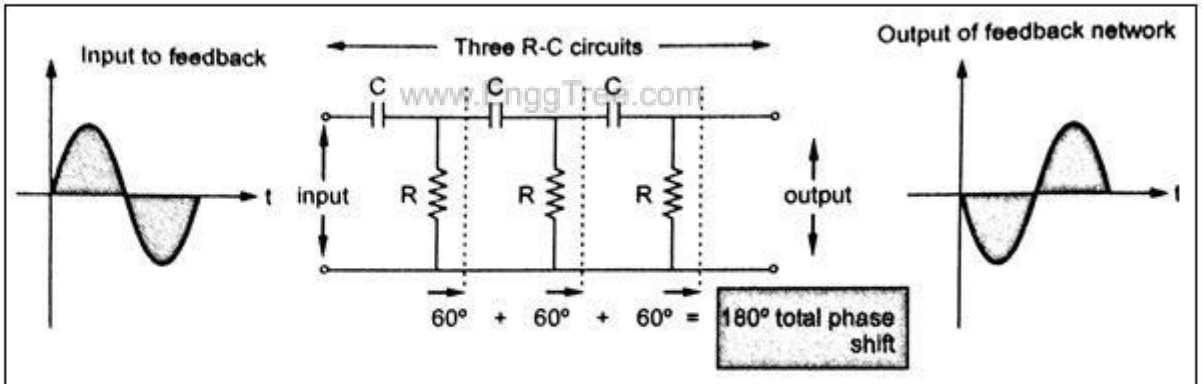
$$I = \frac{V_i < 0^0}{Z} = \frac{V_i < 0^0}{|Z| < -\Phi^0} = |\frac{V_i}{Z}| < +\Phi^0 \quad A$$

$$\boxed{|Z| = \sqrt{R^2 + X_C^2} \;\; and \;\; \Phi = \tan^{-1}\frac{X_C}{R}}$$

- In this equation the current ‘I’ leads input voltage by angle Φ
- The output voltage is drop across R hence $V_O = V_R = IR$
- The output voltage is in phase with current hence it leads input voltage by angle Φ
- Thus, RC circuit introduces a phase shift Φ between input and output which depends on R, C and frequency f.

RC Feedback Network for phase shift oscillator:

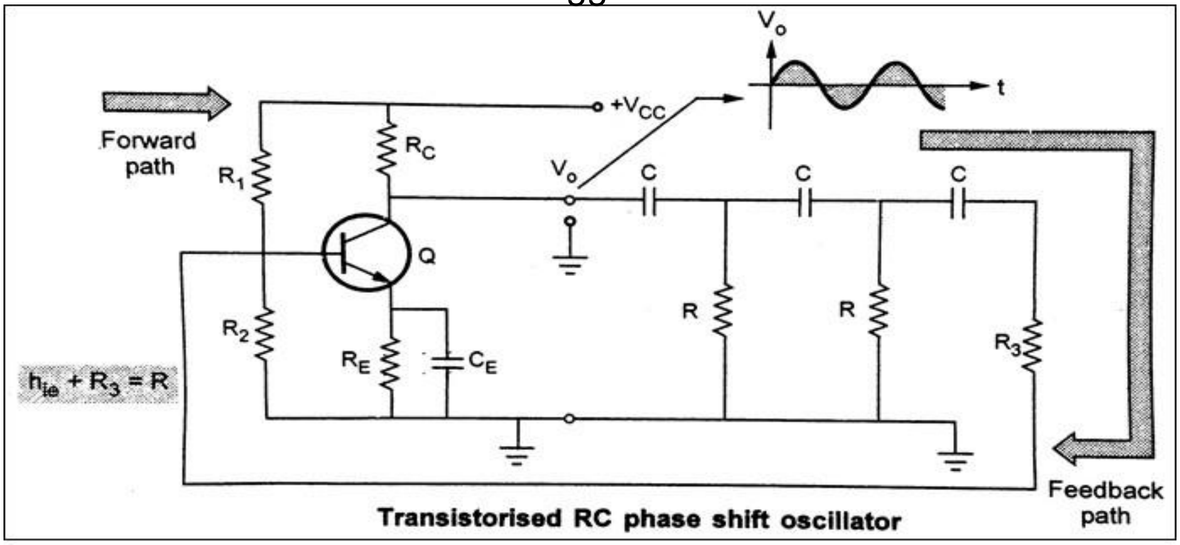
- In RC phase shift oscillator, amplifier introduces a phase shift of 180^0
- Thus, the feedback network must introduce a phase shift of 180^0 to satisfy Barkhausen condition.
- The RC feedback network consists of three RC sections, with each RC section contributing 60^0 phase-shift.
- Hence in RC phase shift oscillator, the feedback network consists of three RC sections are shown in fig.
- In all the three sections, resistance values and capacitance values are same so that at a particular frequency, each section produces precisely 60^0 phase-shift. This is the operating frequency of oscillator.



Feedback network in RC phase shift oscillator

Transistorized RC phase shift oscillator:

- The RC phase shift oscillator uses BJT amplifier stage which is single stage amplifier in common emitter configuration.
- A phase shift network has three RC sections
- The output of CE amplifier is connected as input to the RC phase shifting network
- The output of RC phase shifting network is connected as input to the amplifier
- Due to common emitter amplifier it introduces a phase shift of 180^0 between its input and output
- The RC phase shift network contributes further 180^0 phase shift so that phase shift around a loop is 360^0



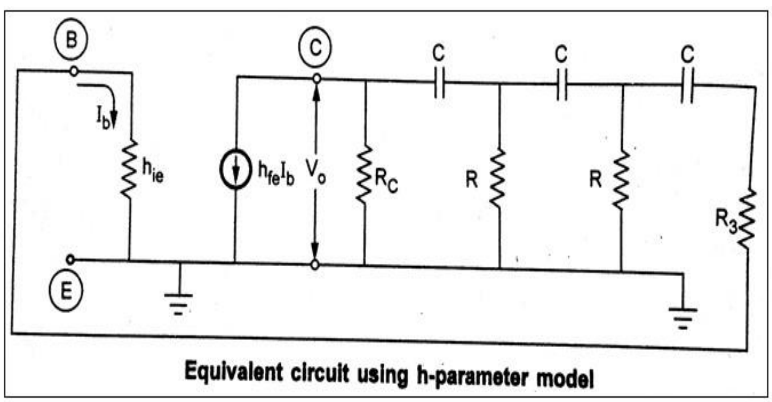
Transistorised RC phase shift oscillator

- From the fig. neglecting R1 and R2 we can write h_{ie}= input impedance of amplifier stage
- Thus, to have all three resistance values in three RC section equal, resistance in the last section is selected as R_3 so that $R_3+h_{ie}=R$

  $\boxed{R_3 + h_{ie} = R}$ i.e $\boxed{R_3 = R- h_{ie}}$ ------------- ***eq. 1***
- If R1 and R2 are not neglected then, $\boxed{R3 = R- [R_1 \parallel R_2 \parallel h_{ie}]}$ ----- ***eq. 2***
- When gain A of the amplifier stage and feedback factor β are adjusted to give |Aβ| = 1, then the circuit works as an oscillator, satisfying both Barkhausen condition.

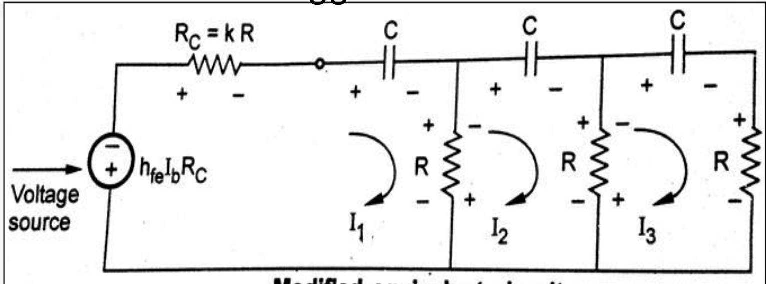
<u>Derivation for frequency of oscillation:</u>

- Replacing the transistor by its approximate h-parameter model, the equivalent circuit of RC phase shift oscillator is shown in fig.



Equivalent circuit using h-parameter model

- It is known that $R = h_{ie} + R_3$ and replace current source by equivalent voltage source.
- The ratio of resistance R_C to R is K. $\boxed{\frac{R_C}{R} = K}$
- The modified equivalent circuit is shown below



Modified equivalent circuit

- Applying KVL to the three loops

$$I_1 R_C - \frac{1}{j\omega C} I_1 - R(I_1 - I_2) - h_{fe} I_b R_c = 0 \quad and\ use\ \ R_C = k\,R$$

$\therefore\ I_1\ [kR + R + \frac{1}{j\omega C}] + I_2 R\ = h_{fe}\ I_b\ k\ R$ --------- ***eq. 3***

$-\frac{1}{j\omega C} I_2 - R(I_2 - I_1) - R(I_2 - I_3) = 0\ \ i.e\ \ I_1 R - I_2\ (2R + \frac{1}{j\omega C}) + I_3 R = 0$ ----- ***eq. 4***

$-\frac{1}{j\omega C} I_3 - I_3 R - R(I_3 - I_2) = 0\ \ \ i.e\ \ I_2 R - I_3\ (2R + \frac{1}{j\omega C}) = 0$ ----- ***eq. 5***

- Using jω = s and Cramers's rule

$$D = \begin{vmatrix} -(k+1)R - \frac{1}{sC} & +R & 0 \\ R & -2R - \frac{1}{sC} & R \\ 0 & R & -2R - \frac{1}{sC} \end{vmatrix}$$

- Solving the determinant, we get,

$$D = -\{\frac{s^3C^3R^3(3k+1) + s^2C^2R^2(4k+6) + sRC(5+k) + 1}{s^3C^3}\}$$ ------- ***eq. 6***

- To find I_3, find D_3 as,

$$D_3 = \begin{vmatrix} -(k+1)R - \frac{1}{sC} & R & h_{fe}\ I_b kR \\ R & -2R - \frac{1}{sC} & 0 \\ 0 & R & 0 \end{vmatrix} = kR^3 h_{fe} I_b$$ -------------------***eq. 7***

$$I_3 = \frac{D_3}{D} = \frac{-kR^3 h_{fe} I_b s^3 C^3}{s^3C^3R^3(3k+1) + s^2C^2R^2(4k+6) + sRC(5+k) + 1}$$ ------------------------***eq. 8***

I_3 = Output current of the feedback circuit
I_b = Input current of the amplifier
I_C = h_{fe} I_b = input current of the feedback circuit

$$\beta = \frac{\text{Output of the feedback circuit}}{\text{Input to feedback circuit}} = \frac{I_3}{I_C} = \frac{I_3}{h_{fe} I_b}$$

$$A = \frac{\text{Output of the amplifier}}{\text{Input to the amplifier}} = \frac{I_3}{I_b} = h_{fe}$$

$$A\beta = h_{fe} \, X \, \frac{I_3}{h_{fe} I_b} = \frac{I_3}{I_b} \qquad \text{------- } \textbf{\textit{eq. 9}}$$

From equation 8 and 9,

$$A\beta = \frac{-kR^3 h_{fe} s^3 C^3}{s^3C^3R^3(3k+1) + s^2C^2R^2(4k+6) + sRC(5+k) + 1} - - - - - - \textbf{eq. 10}$$

Using s = jω $s^2 = j^2 \omega^2 = -\omega^2$, $s^3 = j^3 \omega^3 = -j\omega^3$ and separating the real and imaginary part we get,

$$A\beta = \frac{+j\omega^3 kR^3C^3 h_{fe}}{[1 - 4k\omega^2C^2R^2 - 6\omega^2C^2R^2] - j\omega[3k\omega^2R^3C^3 + \omega^2R^3C^3 - 5RC - kRC}$$

Dividing numerator and denominator by j ω^3 R^3 C^3 and replacing -1/j = +j

$$A\beta = \frac{kh_{fe}}{-j\left\{\frac{1}{\omega^3R^3C^3} - \frac{4k}{\omega RC} - \frac{6}{\omega RC}\right\} - \left\{3k + 1 - \frac{5}{\omega R^2C^2} - \frac{k}{\omega^2R^2C^2}\right\}}$$

Replacing 1/ωRC by α for simplicity

$$\boxed{A\beta = \frac{kh_{fe}}{[-3k-1+5\alpha^2+k\alpha^2] - j[\alpha^3 - 4k\alpha - 6\alpha]}} \text{------- } \textbf{\textit{eq. 11}}$$

To satisfy Barkhausen criterion, <Aβ = 0^0 hence imaginary part of the denominator term must be 0

$$\therefore \ \alpha^3 - 4k\alpha - 6\alpha = 0 \quad \text{i.e.} \quad \alpha(\alpha^2 - 4k - 6) = 0$$

$\therefore$ α2 = 4 k + 6 (α ≠ 0) i.e. $\boxed{\alpha = \sqrt{4k+6}}$ ------ ***eq. 12***

$\therefore$ 1/ωRC = $\sqrt{4k+6}$ i.e. $\boxed{\omega = \frac{1}{RC\sqrt{4k+6}}}$ i.e. $\boxed{f = \frac{1}{2\pi\sqrt{4k+6}}}$

This is the required frequency of oscillations.

Substituting $\alpha = \sqrt{4k+6}$ in equation 11 we get,

$$A\beta = \frac{kh_{fe}}{-3k - 1 + (4k+6)(5+k)} = \frac{kh_{fe}}{4k^2 + 23k + 29}$$

But $|A\beta| = 1$ $\quad i.e \quad |\frac{kh_{fe}}{4k^2+23k+29}| = 1$

$$\boxed{\therefore h_{fe} = 4k + 23k + \frac{29}{k}}$$

This is the required h_{fe} for the oscillations.

<u>Minimum value of h_{fe}:</u>

- For satisfying $A\beta = 1$, the expression for the value of h_{fe} of the transistor used in RC phase shift oscillator is given by,

$$\boxed{h_{fe} \geq 4\ k + 23 + \frac{29}{k} \quad \text{where } k = \frac{RC}{R}}$$

- For minimum h_{fe}, find k for minimum h_{fe} from the expression $\frac{dh_{fe}}{dk} = 0$

$\therefore \frac{d}{dk}[4k + 23 + \frac{29}{k}] = 0$ i.e. $4 - \frac{29}{k^2} = 0$ i.e. $k^2 = \frac{29}{4}$

$$\boxed{k = 2.6925 \text{ for minimum } h_{fe}}$$

using in the expression of h_{fe},

$$h_{fe}\,(\text{min}) = 4 \times 2.6925 + 23 + \frac{29}{2.6925} = \mathbf{44.54}$$

Thus for the circuit to oscillate, the transistor must be selected with h_{fe} greater than 44.54

<u>Advantages:</u>

- The circuit is simple to design
- Can produce output over audio frequency range
- Produces sinusoidal output waveform
- It is fixed frequency oscillator

<u>Disadvantages:</u>

- To vary the frequency, values of R and C of all three sections are to be varied simultaneously which is practically difficult. Hence frequency cannot be varied
- Frequency stability is poor due to changes in the values of various components due to effect temperature, aging etc.

(B) WEIN BRIDGE OSCILLATOR: (RC Oscillator)

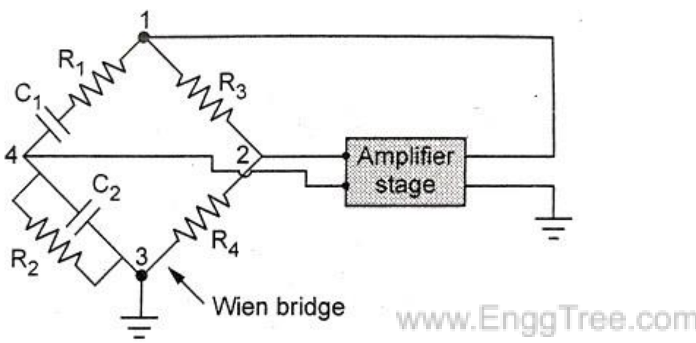
Explain the working of Wien Bridge Oscillator. Derive the expression for frequency of oscillation and condition for maintenance of oscillation.

(OR)

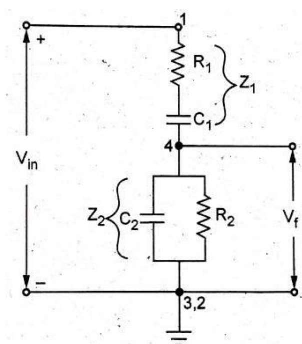
Design an oscillator to operate at a frequency of 10 KHz which gives an extremely pure sine wave output, good frequency stability and highly stabilized amplitude. Discuss the operation of this oscillator as an audio signal generator.

Construction and operation - (Wien Bridge Oscillator Circuit)

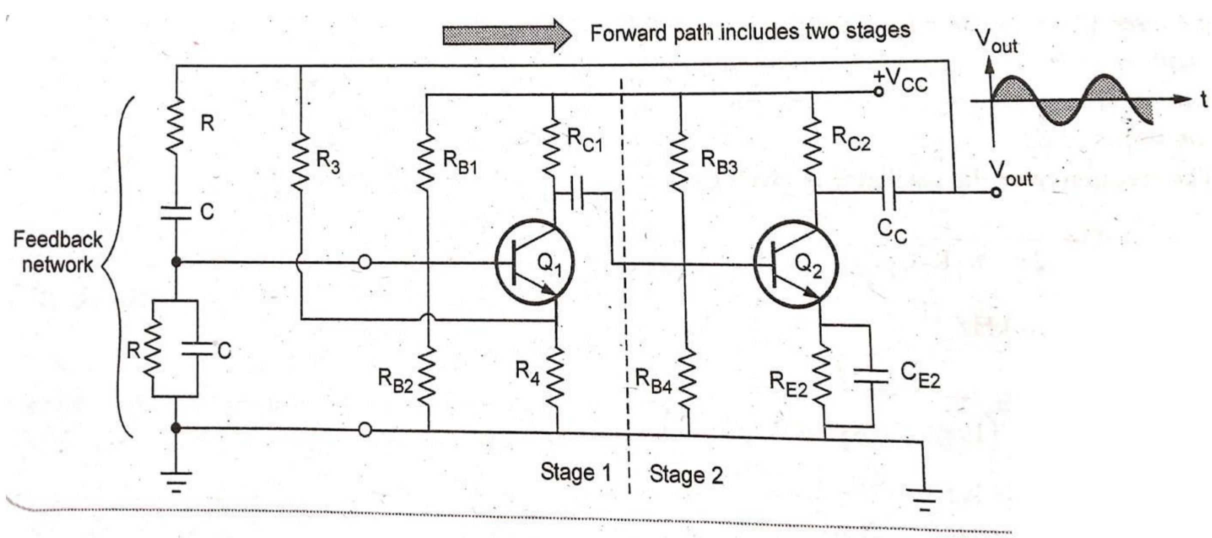
- **Two stage amplifiers (non-inverting)** and **feedback network** are used in *Wien Bridge Oscillator*.
- Both amplifier and feedback network does not introduce any phase shift i.e. 0° phase-shift around the loop in Wien Bridge Oscillator.
- R_1 & C_1 in series and R_2 & C_2 in parallel are frequency sensitive arms.
- The output of Amplifier is applied as input to Feedback Network (V_{in}) between 1 and 3.
- The output of Feedback Network (V_f) taken between 2 and 4 is given as input to amplifier.
- This Feedback Network is also known as **Lead-Lag Network**.



Basic circuit of Wien bridge oscillator



Feedback network of Wien bridge oscillator



Transistorised Wien bridge oscillator

Derive the expression for frequency of oscillation:

Analysis for frequency of oscillation:

$$Z_1 = R_1 + \frac{1}{j\omega C_1} \Rightarrow Z_1 = \frac{1 + j\omega R_1 C_1}{j\omega C_1} \qquad (1)$$

$$Z_2 = R_2 \qquad \frac{1}{j\omega C_2} \Rightarrow Z_2 = \frac{R_2 \times \frac{1}{j\omega C_2}}{R_2 + \frac{1}{j\omega C_2}} \Rightarrow Z_2 = \frac{R_2}{1 + j\omega R_2 C_2} \qquad (2)$$

$$\beta = \frac{V_f}{V_{in}} \qquad (3)$$

$$I = \frac{V_{in}}{Z_1 + Z_2} \qquad (4)$$

$$V_f = I\, Z_2 \qquad (5)$$

$$Sub\ (4) in\ (5) \Rightarrow V_f = -\frac{Z_2}{Z_1 + Z_2} V_{in} \qquad (6)$$

Sub (6) in (3)

$$\Rightarrow \quad \beta = \frac{Z_2}{Z_1 + Z_2} \qquad (7)$$

$Substitute$ (1) & (2) in (7)

$$\beta = \frac{\frac{R_2}{1 + j\omega R_2 C_2}}{\frac{1 + j\omega R_1 C_1}{j\omega C_1} + \frac{R_2}{1 + j\omega R_2 C_2}} \qquad (8)$$

Simplify the equation (8),

$$\beta = \frac{j\omega R_2 C_1}{(1 - \omega^2 R_1 R_2 C_1 C_2) + j\omega(R_1 C_1 + R_2 C_2 + R_2 C_1)} \qquad (9)$$

Rationalizing and Simplifying the equation (9),

$$\beta = \frac{\omega^2 R_2 C_1 (R_1 C_1 + R_2 C_2 + R_2 C_1) + j\omega C_1 R_2 (1 - \omega^2 R_1 R_2 C_1 C_2)}{(1 - \omega^2 R_1 R_2 C_1 C_2)^2 + \omega^2 (R_1 C_1 + R_2 C_2 + R_2 C_1)^2} \qquad (10)$$

To have zero phase shift, imaginary part of above equation must be zero.

$$(1 - \omega^2 R_1 R_2 C_1 C_2) = 0$$

$\omega\ (\omega^2 R_1 R_2 C_1 C_2) = 0$ but ω can not be zero. So,

$$\omega^2 R_1 R_2 C_1 C_2 = 0 \quad \Rightarrow \omega^2 = \frac{1}{R_1 R_2 C_1 C_2}$$

$$\Rightarrow \omega = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \qquad (11)$$

$$Frequency\ of\ Wien\ Bridge\ Oscillator,\ \boldsymbol{f = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}}\ \mathbf{Hz} \qquad (12)$$

$In\ pratice, R_1 = R_2 = R$ and $C_1 = C_2 = C$ hence,

$$Frequency\ of\ Wien\ Bridge\ Oscillator,\ \boldsymbol{f = \frac{1}{2\pi\ RC}\ Hz}$$

<u>Derive the condition for maintenance of oscillation:</u>

<u>Case (1)</u>: $If\ R_1 = R_2 = R$ and $C_1 = C_2 = C\ then\ use\ \omega = \frac{1}{RC}\ Hz$ in (10),

we get the magnitude of the feedback network as,

$$Q = \frac{3}{0 + \frac{1}{R^2C^2}(3RC)^2} = \frac{3}{9} = \boldsymbol{\frac{1}{3}} \qquad \Rightarrow \quad Q = \boldsymbol{\frac{1}{3}}$$

As $|A\beta| \geq 1\ hence\ |A| \geq 3\ for\ Wien\ Bridge\ Oscillator.$

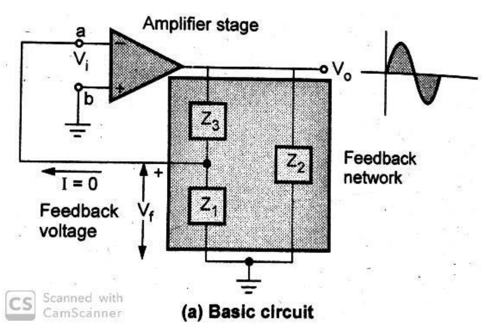
Thus, the gain of amplifier stage must be at least 3 to ensure sustained oscillations in Wien Bridge Oscillator.

<u>C</u>ase (2): If $R_1 \neq R_2$ and $C_1 \neq C_2$ then use $\omega = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}\ in\ (10)\ then$

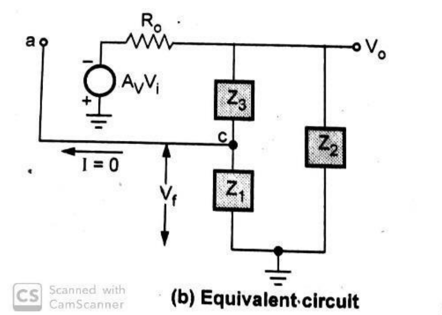
$$Q = \frac{\boldsymbol{R_2 C_1}}{\boldsymbol{R_1 C_1 + R_2 C_2 + R_2 C_1}} \qquad \Rightarrow \therefore \boldsymbol{A} \geq \frac{\boldsymbol{R_1 C_1 + R_2 C_2 + R_2 C_{12}}}{\boldsymbol{R_2 C_1}} \qquad \{\because\ |A\beta| \geq 1\}$$

<u>LC OSCILLATORS:</u>

Outline the LC tuned Oscillator and deduce expression for amplifier Gain, feedback Gain and necessary condition for LC Oscillator in general.

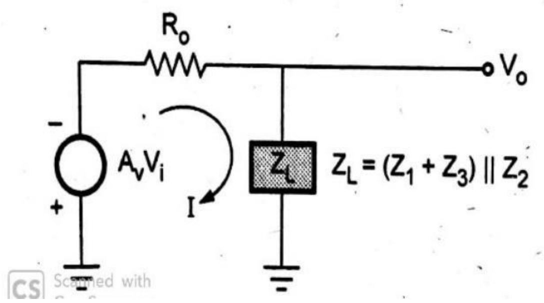


(a) Basic circuit



(b) Equivalent circuit

Analysis of Amplifier stage



R_o – Output impedance of the amplifier stage.
As, I=0 due to infinite input impedance, Z_1 and Z_3 appear in series and the combination in parallel with Z_2 as shown in figure.

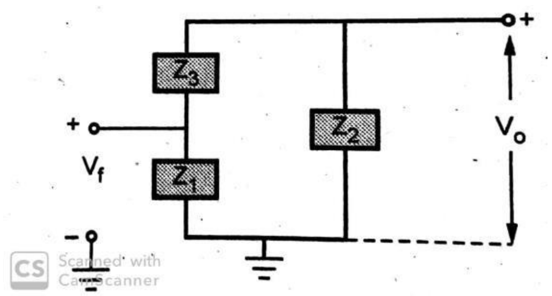
Applying KVL,

$I = -\frac{A_V V_i}{R_o + Z_L}$ and $V_O = IZ_L$

$$\boldsymbol{A = \frac{V_o}{V_i} = -\frac{A_V Z_L}{R_o + Z_L}}$$

A – Gain of amplifier stage.

Analysis of feedback stage



By voltage division in parallel circuit,

$V_f = \frac{V_o Z_1}{Z_1 + Z_3}$

i.e. $\beta = \frac{V_f}{V_o} = \frac{Z_1}{Z_1 + Z_3}$

But as feedback network introduces 180° phase-shift, use negative sign

$$\mathrm{Q} = -\frac{\boldsymbol{Z_1}}{\boldsymbol{Z_1 + Z_3}}$$

Expression of the loop gain :

- According to Barkhausen condition loop gain $-A\beta$ is,

$$-A\beta = -\frac{A_v Z_L Z_1}{(R_o + Z_L)(Z_1 + Z_3)}$$

and $$Z_L = \frac{(Z_1 + Z_3)Z_2}{Z_1 + Z_2 + Z_3}$$

$$\therefore \boxed{-A\beta = -\frac{A_v Z_1 Z_2}{R_o(Z_1 + Z_2 + Z_3) + Z_2(Z_1 + Z_3)}}$$

The impedances Z_1, Z_2, Z_3 are pure reactive elements either L or C.

$$\therefore \boxed{Z_1 = jX_1, \; Z_2 = jX_2, \; Z_3 = jX_3}$$

Thus the loop gain becomes,

$$-A\beta = -\frac{A_v (jX_1)(jX_2)}{R_o j(X_1 + X_2 + X_3) + jX_2(jX_1 + jX_3)}$$
$$= \frac{A_v X_1 X_2}{-X_2(X_1 + X_3) + jR_o(X_1 + X_2 + X_3)}$$

- To have 0° phase shift for the loop gain, the imaginary part must be zero.

$$\therefore \boxed{(X_1 + X_2 + X_3) = 0}$$

$$\therefore \quad -A\beta = \frac{-A_v X_1 X_2}{X_2(X_1 + X_3)} \quad \text{but} \quad X_1 + X_3 = -X_2$$

$$\therefore \boxed{-A\beta = A_v\left(\frac{X_1}{X_2}\right)}$$

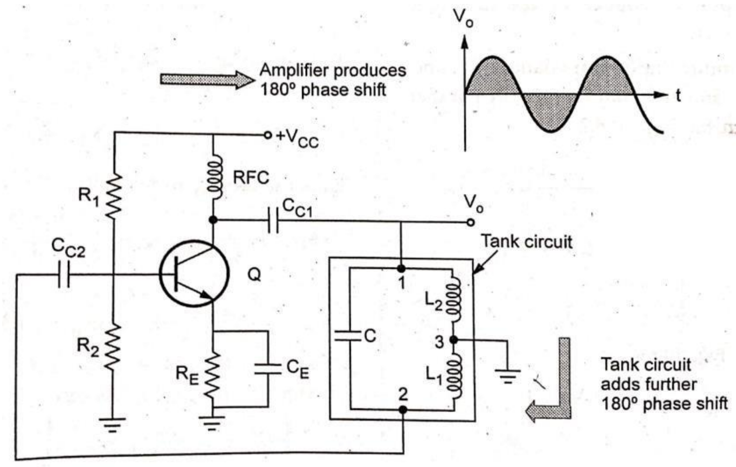
- According to Barkhausen condition $-A\beta$ must be positive and greater than equal to 1. As A_v is positive, $-A\beta$ will be positive only when X_1 and X_2 have same sign.
- Thus X_1 and X_2 must be of same type, either inductive or capacitive. And as $X_1 + X_3 = -X_2$ i.e. $X_3 = -(X_1 + X_2)$, the element X_3 must be opposite type of reactance to X_1 and X_2.

Types of LC Oscillators:

Oscillator Type	Reactance elements in the tank circuit		
	X_1	X_2	X_3
Hartley oscillator	L	L	C
Colpitts oscillator	C	C	L

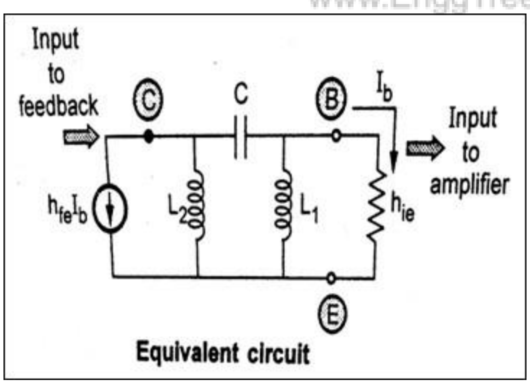
(C) ***Hartley Oscillator:***

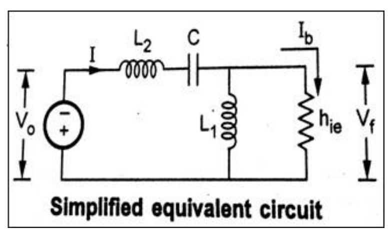
Explain the working of Hartley Oscillator. Derive the expression for frequency of oscillation and condition for maintenance of oscillation.



Transistorised Hartley oscillator

Circuit diagram





Construction:

- The Hartley oscillator circuit using BJT as an active device.
- The resistances R_1, R_2 and R_E are biasing resistors
- The RFC is radio frequency chock whose reactance value is very high and high frequency and can be treated as open circuit. While for d.c operation, it is shorted hence does not cause problems for d.c operation.
- Due to RFC, the isolation between a.c and d.c operation is achieved. The C_1 and C_2 are coupling capacitors while C_E is the emitter bypass capacitor. The CE amplifier provides phase shift of 180^0.
- In the feedback circuit, as the centre of L_1 and L_2 is grounded, it provides additional phase shift of 180^0. This satisfies Barkhausen condition. In this oscillator, $X_1 = \omega L_1$,
  $X_2 = \omega L_2$, $X_3 = -1/\omega C$

Analysis:

- For LC oscillator, $X_1+X_2+X_3=0$

$$\therefore\ \omega L_1 + \omega L_2 - \frac{1}{\omega C} = 0$$

i.e $$\omega(L_1 + L_2) = \frac{1}{\omega c}$$

$$\therefore\ \omega = \frac{1}{\sqrt{(L_1 + L_2)C}}$$ i.e $$\boxed{f = \frac{1}{2\pi\sqrt{(L_1 + L_2)C}}}$$

- The inductance L_1+L_2 is equivalent inductance denoted as L_{eq}. To satisfy $|A\beta| = 1$, then h_{fe} of the BJT used must be L_1/L_2.

$$\boxed{h_{fe} = \frac{L_1}{L_2}}$$

- Practically L1 and L2 are wound on a single core and there exists a mutual inductance M between them.

In this case, $$\boxed{L_{eq} = L_1 + L_2 + 2M}$$

$$\boxed{f = \frac{1}{2\pi\sqrt{L_{eq}C}}}$$ and $$\boxed{h_{fe} = \frac{L_1+M}{L_2+M}}$$

- If capacitor C is kept variable, frequency can be varied over wide range.

Derivation of frequency of Oscillations

- The output current is collector current which is $h_{fe}\, I_b$, where I_b is base current. Assuming coupling capacitors shorted the capacitor C gets connected between collector and base.
- As emitter is grounded for a.c analysis, L_1 is between emitter and base while L_2 is between emitter and collector.
- h_{ie} is the input impedance of the transistor. The output current is I_b while input current is $h_{fe}\, I_b$. Convert current source to voltage source.

$$\boxed{V_O = h_{fe} I_b j X_{L2} = h_{fe} I_b j\omega L_2}$$

- Total current I is,

$$I = \frac{-V_o}{[X_{L2} + X_C] + [X_{L1}||h_{ie}]}$$

- Negative sign is because direction of I is opposite to the polarities of V_o

$$X_{L2} + X_C = j\omega L_2 + \frac{1}{j\omega C} = \frac{-\omega^2 L_2 C + 1}{j\omega C}$$

$$X_{L1}||h_{ie} = \frac{j\omega L_1 h_{ie}}{j\omega L_1 + h_{ie}}$$

$$\therefore I = \frac{-h_{fe} I_b j\omega L_2}{\frac{-\omega^2 L_1 C + 1}{j\omega C} + \frac{j\omega L_1 h_{ie}}{j\omega L_1 + h_{ie}}}$$

- Using current division rule for parallel elements,

$$I_b = I \; X \; \frac{j\omega L_1}{j\omega L_1 + h_{ie}}$$

$$I_b = \frac{-h_{fe} I_b j\omega L_2}{\frac{-\omega^2 L_2 C + 1}{j\omega C} + \frac{j\omega L_1 h_{ie}}{j\omega L_1 + h_{ie}}} \; X \; \frac{j\omega L_1}{j\omega L_1 + h_{ie}}$$

$$\therefore 1 = \frac{j\omega^3 h_{fe} C L_1 L_2}{-j\omega^3 L_1 L_2 C h_{ie}(L_1 + L_2) + j\omega L_1 + h_{ie}}$$

$$\therefore 1 = \frac{j\omega^3 h_{fe} C L_1 L_2}{[h_{ie} - \omega^2 C h_{ie}(L_1 + L_2)] + j\omega L_1 (1 - \omega^2 L_2 C)}$$

- Rationalizing R.H.S of the above equation,

$$1 = \frac{\omega^4 h_{fe} L_1^2 L_2 C(1 - \omega^2 L_2 C) + j\omega^3 h_{fe} L_1 L_2 C[h_{ie} - \omega^2 C h_{ie}(L_1 + L_2)]}{[h_{ie} - \omega^2 C h_{ie}(L_1 + L_2)]^2 + \omega^2 L_1^2 (1 - \omega^2 L_2 C)^2}$$

- Imaginary part of R.H.S of above equation must be Zero

$$\therefore \; 1 - \omega^3 C(L_1 + L_2) = 0 \quad i.e \;\; \omega = \frac{1}{\sqrt{C(L_1 + L_2)}} \qquad (\omega^3 h_{fe} \, h_{ie} L_1 L_2 C \neq 0)$$

$$\boxed{f = \frac{1}{2\pi\sqrt{C(L_1 + L_2)}} = \frac{1}{2\pi\sqrt{C L_{eq}}}}$$

- Equating magnitude of both sides of the equation and using $\omega = \frac{1}{\sqrt{C(L_1+L_2)}}$ *we get*

$h_{fe} = \frac{L_1}{L_2}$ $\quad h_{fe}$ *required for oscillation*

- In practice, L_1 and L_2 may be wound on a single core so that there exists a mutual inductance between them denoted as M.
- In such a case, the mutual inductance is considered while determining the equivalent inductance L_{eq}, $\boxed{L_{eq} = L_1 + L_2 + 2M}$
- If L_1 and L_2 are assisting each other, then sign of 2M is positive while if L1 and L2 are in series opposition then sign of 2M is negative.

Advantage:

- The frequency can be easily varied by variable capacitor
- The output amplitude remains constant over the frequency range
- The feedback ratio of L1 and L2 remains constant
- It can be operated over wide range of frequency

Disadvantage:

- The output is rich in harmonics hence not suitable for pure sine wave requirement
- Poor frequency stability

Applications:

- Used as local oscillators in TV and radio receivers
- In function generators
- In radio frequency sources

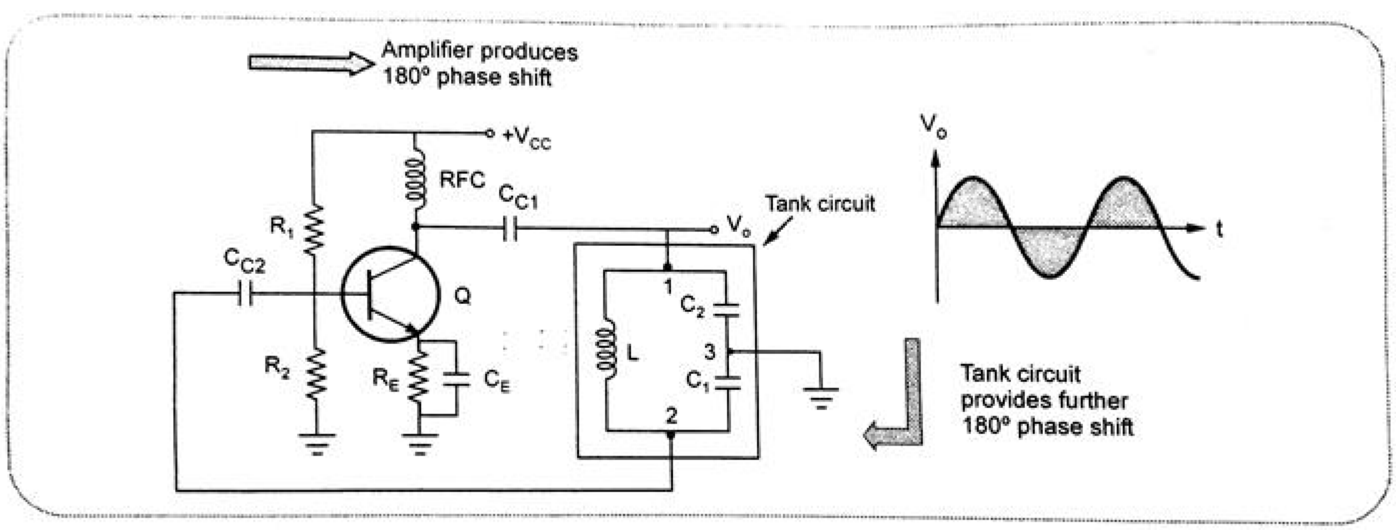
(D) COLPITTS OSCILLATOR:

Explain the working of Colpitts Oscillator. Derive the expression for frequency of oscillation and condition for maintenance of oscillation.

(OR)

With a neat circuit diagram deduce the necessary condition for oscillations and expression for oscillation frequency in the case of Colpitts Oscillator.

Construction:



Transistorised Colpitts oscillator

- It uses ***two capacitive resistances and one inductive reactance in its feedback network***.
- The amplifier stage uses BJT in common emitter configuration providing 180^o phase shift. The resistance R_1, R_2 and R_E are the biasing resistors.
- The RFC is radio frequency choke providing insulation between AC and DC operations. The C_{C1} and C_{C2} are coupling capacitors. In the feedback circuit, as the center C_1 and C_2 are grounded, it provides additional phase shift of 180^0, satisfying Barkhausen angle condition.

- In this oscillator $X_1 = \frac{-1}{\omega C_1}$ $X_2 = \frac{-1}{\omega C_2}$ $X_3 = \omega L$
- For LC oscillator, $X_1+X_2+X_3=0$

  $\therefore -\frac{1}{\omega C_1} - \frac{1}{\omega C_2} + \omega L = 0$ i.e $\omega L = \frac{1}{\omega}[\frac{1}{C_1} + \frac{1}{C_2}]$

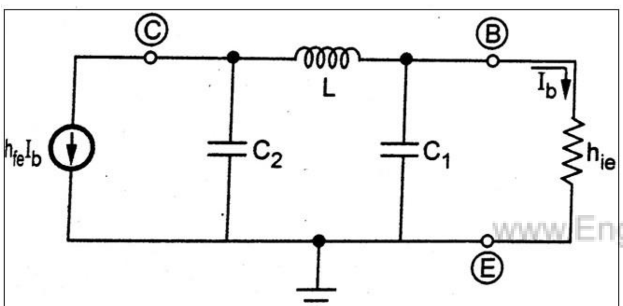
  $\therefore \omega^2 = \frac{1}{L[\frac{C_1 C_2}{C_1+C_2}]}$ where $\frac{C1C2}{C_1+C_2} = C_{eq}$

  $\therefore \omega = \frac{1}{\sqrt{LC_{eq}}}$ i.e $\boxed{f = \frac{1}{2\pi\sqrt{LC_{eq}}} \ and\ C_{eq} = \frac{C_1C_2}{C_1+C_2}}$
- To satisfy magnitude condition of Barkhausen criterion, the h_{fe} of BJT used is given by

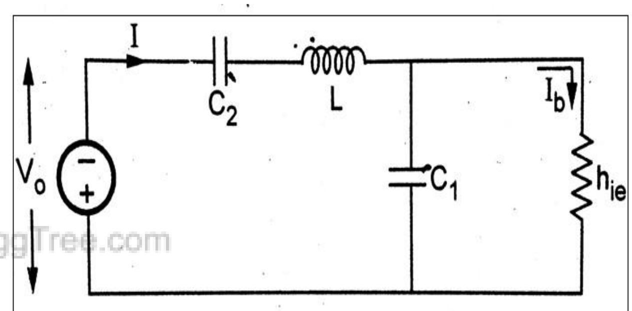
$$h_{fe} = \frac{C_2}{C_1}$$

Derivation of Frequency of oscillations

- The equivalent circuit and simplified equivalent circuit.



(a) Equivalent circuit



(b) Simplified equivalent circuit

$\boxed{V_0 = h_{fe}I_bX_{C2} = \frac{-jh_{fe}I_b}{\omega C_2}}$ ….. $X_{C2} = \frac{1}{j\omega C_2} = -\frac{j}{\omega C_2}$

- The total current drawn I is,

$$I = \frac{-V_0}{[XC_2 + X_L] + [XC_1||h_{ie}]}$$

$$XC_2 + X_L = \frac{-j}{\omega C_2} + j\omega L = \frac{-j(1-\omega^2 LC_2)}{\omega C_2}$$

$$X_{C1}||h_{ie} = \frac{-\frac{j}{\omega C_1} X h_{ie}}{-\frac{j}{\omega C_1} + h_{ie}} = \frac{-jh_{ie}}{-j + \omega C_1 h_{ie}}$$

$$I = \frac{-[-\frac{jh_{fe}I_b}{\omega C_2}]}{\frac{-j(1-\omega^2 LC_2)}{\omega C_2} - \frac{-jh_{ie}}{-j+\omega C_1 h_{ie}}}$$

- Using current division rule for parallel elements

$$I_b = I\,X\,\frac{\frac{-j}{\omega C_1}}{\frac{-j}{\omega C_1} + h_{ie}} = \frac{-jI}{-j + \omega C_1 h_{ie}}$$

$$I_b = -j\left[\frac{\frac{jh_{fe}I_b}{\omega C_2}}{\frac{-j(1-\omega^2 LC_2)}{\omega C_2}\;\frac{-jh_{ie}}{-j+\omega C_1 h_{ie}}}\right]\left[\frac{1}{-j+\omega C_1 h_{ie}}\right]$$

$$1 = \frac{-h_{fe}}{(1-\omega^2 LC_2) + j\omega h_{ie}[C_1 + C_2 - \omega^2 LC_1C_2]} \quad \text{--------------} \; 1$$

- To have imaginary part of above equation zero
  $C1+C2-\omega^2 LC_1C_2 = 0$ i.e $\omega^2 = \frac{C_1+C_2}{LC_1C_2} = \frac{1}{L\left[\frac{C_1C_2}{C_1+C_2}\right]}$

$$\boxed{\omega = \frac{1}{\sqrt{LC_{eq}}} \quad and \quad f = \frac{1}{2\pi\sqrt{LC_{eq}}} \quad where\ C_{eq} = \frac{C_1C_2}{C_1+C_2}}$$

- Substituting ω in equation 1 and equating magnitudes of both sides

$$\boxed{h_{fe} = \frac{C_2}{C_1}}$$

Advantages:

- Pure output waveform
- Good stability at high frequency
- Improved performance at high frequency
- Wide range of frequency
- Simple construction
-

Disadvantages:

- Difficult to adjust the feedback
- Poor isolation

Applications:

- Its main application is high frequency function generators.

(E) CRYSTAL OSCILLATOR:

Describe and explain the operation of the crystal oscillator.

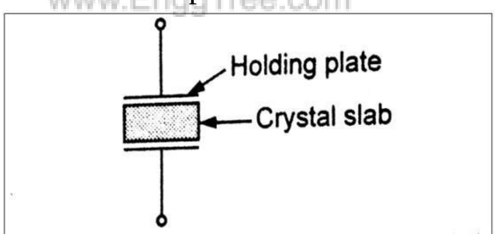
(OR)

Can you use Piezo-Electric effect for electric oscillators? If so, explain a component with such characteristics. Also draw a circuit for the same.

- The crystals are either naturally occurring or synthetically manufactured, exhibiting the piezoelectric effect
- The piezoelectric effect means under the influence of mechanical pressure, the voltage gets generated across the opposite faces of the crystal
- If the mechanical force is applied in such a way to force the crystal to vibrate the a.c voltage gets generated across it.
- Every crystal has its own resonating frequency depending on its cut. So under the influence of the mechanical vibrations, the crystal generates an electrical signal of very constant frequency
- The crystal has a greater stability in holding the constant frequency. The crystal oscillators are preferred when greater frequency stability is stability
- Quartz is a compromise between the piezoelectric activity of Rochelle salt and the strength of the tourmaline.
- Quartz is inexpensive and easily available in nature hence very commonly used in the crystal oscillators.

Constructional Details:

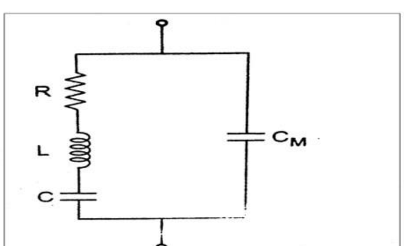
- The natural shape of quartz is a hexagonal prism. But for its practical use, it is cut to the rectangular slab. This slab is then mounted between the two metal plates.



Symbolic representation of a crystal

- The metal plates are called holding plates, as they hold the crystal slab in between them.

A.C. Equivalent circuit:



equivalent circuit of a crystal

C_M – Mounting Capacitance (due to two metal plates separated by dielectric like crystal slab).
R – Resistance (internal friction loss during vibration)
L – Inductance (indication of inertia of mass of crystal)
C – Capacitor (stiffness during vibrating)

- RLC forms a resonating circuit. The expression for the resonating frequency f_r is,

$$f_r = \frac{1}{2\pi\sqrt{LC}}\sqrt{\frac{Q^2}{1+Q^2}} \text{ where Q = Quality factor of crystal}$$

$$Q = \frac{\omega L}{R}$$

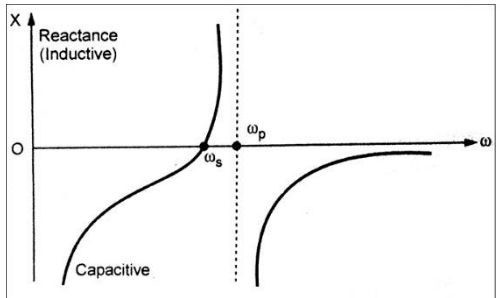
- The Q factor of the crystal is very high, typically 20,000. Value of Q up to 10^6 also can be achieved. Hence $\sqrt{\frac{Q^2}{1+Q^2}}$ factor approaches to unity and we get the resonating frequency as $f_r = \frac{1}{2\pi\sqrt{LC}}$
- The crystal frequency is in fact inversely proportional to the thickness of the crystal.
  - $\boxed{f \;\alpha\; \frac{1}{t} \text{ where t = Thickness}}$
- So to have very frequencies, thickness of the crystal should be very small
- The crystal has two resonating frequencies, series resonant frequency and parallel resonant frequency.

Applications
- Watches
- Communication transmitters and receivers

Series and Parallel resonance:

- **Series Resonance frequency**

$$\boxed{f_s = \frac{1}{2\pi\sqrt{LC}}}$$



The reactance versus frequency

- **Parallel Resonance frequency**

$$\boxed{f_P = \frac{1}{2\pi\sqrt{LC_{eq}}}}$$

-
- If we neglect the resistance R, the impedance of the crystal is a reactance jX which depends on the frequency as,

$$\boxed{jX = -\frac{j}{\omega C_M}\frac{\omega^2 - \omega_s^2}{\omega^2 - \omega_p^2}}$$

Where, ω_s = Series resonant frequency

- Reactance against frequency is shown in fig.

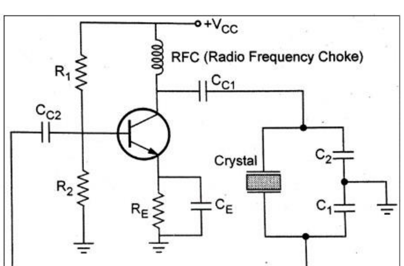
Crystal Stability:

i. Temperature stability
ii. Long term stability
iii. Short term stability

Types of Crystal Oscillator:

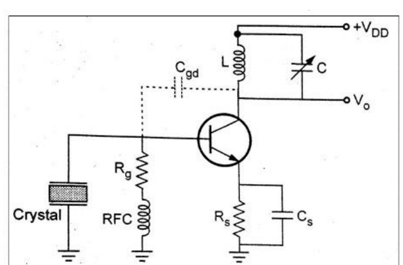
1. Pierce Crystal Oscillator:
2. Miller Crystal Oscillator:

Pierce Crystal Oscillator:



Pierce crystal oscillator

Miller Crystal Oscillator:



Miller crystal oscillator

Comparison between Crystal and LC Oscillator:

Sr. No.	LC oscillators	Crystal oscillators
1.	The separate L and C components are necessary in the tuned circuit.	The single crystal serves the purpose of tuned circuit.
2.	The Q value of LC tuned circuit is less as compared to the crystal.	The Q value is much higher than LC tuned circuit.
3.	The frequency stability is less.	Very high frequency stability.
4.	The bandwidth is more.	The bandwidth is very small.
5.	The effect of temperature on the frequency is more severe.	The effect of temperature on frequency is negligible.
6.	The frequency range which can be generated is more.	There is limit to the frequency generated due to thickness of the crystal.
7.	Used in general purpose applications like signal generators.	Used in specific applications which need high frequency stability like watches, computers, counters.

Solved Problems

1. **In a Hartley oscillator, if L_1=0.2mH, L_2=0.3mH and C=0.003µF. Calculate the frequency of oscillations. [MAY 2012]**

   Given: L_1=0.2mH, L_2=0.3mH, C=0.003µF

   To find frequency of oscillations **f=1/(2π√[(L1+L2) C)]** by substituting **f=129.949KHz**

2. **In a RC phase shift oscillator if $R_1=R_2=R_3$=200KΩ and $C_1=C_2=C_3$=100PF. Find the frequency of oscillation? (Apr/May 2018)**

   Solution:

   The frequency of an RC phase shift oscillator is given by

   $F_o = \frac{1}{2\pi RC\sqrt{6}}$ $\quad$ $F_o = \frac{1}{2\pi\times200\times10^{3}\times100\times10^{-12}\times\sqrt{6}}$ $\quad$ $\boxed{F_o = 3.248KHZ}$

3. **In a phase shift oscillator, R1=R2=R3=1 MΩ and C1=C2=C3=68 pF. At what frequency does the circuit oscillate. (Nov/Dec 2018)**

   Given that,

   For a phase shift oscillator, Resistance, $R_1 = R_2 = R_3$ = 1 MΩ; Capacitor, $C_1 = C_2 = C_3$ = 68 pF

   Frequency, f = ?

   Frequency of phase shift oscillator is given by, $f = \frac{1}{2\pi RC\sqrt{6}}$

Substituting corresponding values in above equation, $f = \frac{1}{2\pi\ X\ 1X10^{6}\ X\ 68\ X\ \sqrt{6}} = 955.9\ Hz$ $\boxed{\text{frequency, f = 955.9 Hz}}$

4. A wien bridge oscillator is used for operation at 10KHz. If the value of the resistor R is 100Kohms, what is the value of C required?

Solution:

Given: F = 10KHZ, R = 100KΩ, C= ?

The frequency of oscillation is

$F = \frac{1}{2\pi RC}$ $C = \frac{1}{2\pi RF}$ $C= \frac{1}{2\pi\times100\times10^3\times10\times10^3}$

$\boxed{\mathbf{C = 1.591\times 10^{-10}\ F}}$

5. An amplifier has a c urrent gain of 240 and input impedance of 15 k Ω without feedback. If negative current feedback (mi = 0.015) is applied, what will be the input impedance of the amplifier? (Nov/Dec 2017)

Solution. $Z'_{in} = \frac{Z_{in}}{1 + m_i A_i}$

Here $Z_{in} = 15\,\text{k}\Omega\,;\quad A_i = 240\,;\quad m_i = 0.015$

$\therefore$ $Z'_{in} = \frac{15}{1 + (0.015)(240)} = 3.26\ \text{k}\Omega$

6. Design a Wien bridge oscillator circuit to oscillate at a frequency of 20KHz. (Nov/Dec2015)

Solution:

$f = \frac{1}{2\pi Rc}$ f = 20 kHz, Let C = $0.01\mu F$

$f = \frac{1}{2\pi Rc}$, $R = \frac{1}{2\pi f C} = \frac{1}{2\times\pi\times20000\times0.01\times10^{-6}} = 80$ohms.

7. A 1 mH inductor is available. Find the capacitor values of a colpitt's oscillator so that f=1 MHz and feedback fraction=0.25 (Nov/Dec 2018)

Solution:

Given that,

For a Colpitts oscillator,

Inductance, L = 1 mH

Resonant frequency, f_0 = 1 MHz

Feedback factor, β = 0.25

The resonant frequency of Colpitts oscillator is given by,

$$f_0 = \frac{1}{2\pi\sqrt{LC_{eq}}} \qquad ----(1)$$

Where, $C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$

From equation (1),

$$C_{eq} = \frac{1}{4\pi^2 f_0^2 L} \qquad ----(2)$$

Given feedback factor, $\beta = \frac{C_1}{C_2} = 0.25$

$C_2 = 4C_1$

Substituting the given specifications in equation (2)

$$C_{eq} = \frac{1}{4\pi^2(10^6)^2 X\, 10^{-3}}$$

$$\frac{C_1C_2}{C_1 + C_2} = 2.533\ X\ 10^{-11}$$

$$\frac{4\ C_1^2}{5C_1} = \ 2.53\ X\ 10^{-11}$$

$$\boxed{\mathbf{C_1 = 3.166\ X\ 10^{-11} = 31.66\ pF}}$$

From $C_2 = 4C_1$,

$C_2 = 4\ X\ (3.166\ X\ 10^{-11})$

$$\boxed{\mathbf{C_2 = 126.65\ pF}}$$

8. The overall gain of a multistage amplifier is 140. When negative voltage feedback is applied the gain is reduced to 17.5 find the fraction of the output that is feedback to the input. (Nov/Dec 2018)

Given that,

For a multistage feedback amplifier,

Overall gain, $A_V = 140$

Feedback gain, $A_{vf} = 17.5$

Feedback fraction, β = ?

Voltage gain of negative feedback amplifier is defined as,

$$A_{vf} = \frac{A_v}{1 +\ A_v\beta} \quad 17.5 = \frac{40}{1 + 140\beta}$$

17.5 + 2450 β = 140

$$\beta = \frac{1}{20} = 0.05 \qquad \boxed{\mathbf{\beta = 0.05}}$$

9. **In colpitts oscillator C1 = 1nF and C2 = 100nF. If the frequency of oscillation is 1 kHz find the value of inductor. Also find the minimum gain required for obtaining sustained oscillations. (May / Jun 2016)**

<u>Given data:</u>

C1 = 1nF, C2 = 100nF, Frequency of oscillation f = 100 kHz.

<u>Formulae used:</u>

$$f = \frac{1}{2n}\sqrt{\frac{C1+C2}{L1C1C2}},\ A_V = \frac{C1}{C2}$$

Frequency of oscillations $\quad L = \frac{C1+C2}{4n^2 f_r^2 C1C2} = \frac{101\times10^{-6}}{4n^2\times(10\times1000)^2\times100\times10^{-12}}$

$$= \frac{101\times10^6}{4n^2\times(100000)^2} = \frac{101}{3.99}\times 10^{-5} \quad = 25.634 \times 10^{-5}H = 256.34\mu F$$

$$A_V > \frac{C1}{C2} = \frac{1}{100} = 0.01nF$$

10. Design a RC phase Shift Oscillator to generate 5KHz sine wave with 20 V peak to Peak amplitude. Assume h_{fe}=Q = 150, C = 1.5nF, hre=1.2KΩ(Nov.Dec 2016)

$$f = \frac{1}{2\pi Rc\sqrt{6}}; \qquad 5 \times 10^3 = \frac{1}{2\pi \times 1.5 \times 10^{-9}\sqrt{6} \times R} \qquad R = \frac{1}{2\pi \times 1.5 \times 10^{-9} \times \sqrt{6} \times 5 \times 10^3}$$

$$R = 8.67\ k\ \Omega$$

11. In Colpitts Oscillator, the desired frequency is 500 KHz. Find the value of L. Assume C= 1000pF. (Apr/May 2018)

$$\therefore \quad C_{eq} = \frac{C_1 C_2}{C_1 + C_2} = 500 \text{ pF}$$

The frequency is given by,

$$f = \frac{1}{2\pi\sqrt{L C_{eq}}}$$

$$\therefore \quad 500 \times 10^3 = \frac{1}{2\pi\sqrt{L \times 500 \times 10^{-12}}}$$

$$\therefore \quad (500 \times 10^3)^2 = \frac{1}{4\pi^2 [L \times 500 \times 10^{-12}]}$$

$$\therefore \quad L = 202.642\ \mu H$$

12. When negative voltage feedback is applied to an amplifier of gain 100, the overall gain falls to 50. Calculate the fraction of the output voltage fedback. If this fraction is maintained, calculate the value of the amplifier gain required if the overall stage gain is to be 75. (Nov/Dec 2017)

(*i*) Gain without feedback, $A_v = 100$

Gain with feedback, $A_{vf} = 50$

Let m_v be the fraction of the output voltage fedback.

Now $$A_{vf} = \frac{A_v}{1 + A_v m_v}$$

or $$50 = \frac{100}{1 + 100\, m_v}$$

or $$50 + 5000\, m_v = 100$$

or $$m_v = \frac{100 - 50}{5000} = 0.01$$

(*ii*) $$A_{vf} = 75; \quad m_v = 0.01; \quad A_v = ?$$

$$A_{vf} = \frac{A_v}{1 + A_v m_v}$$

or $$75 = \frac{A_v}{1 + 0.01\, A_v}$$

or $$75 + 0.75\, A_v = A_v$$

$$\therefore \quad A_v = \frac{75}{1 - 0.75} = 300$$

13. In Colpitts oscillator, C1 = C2 =C and L=100 X 10-6 H. The frequency of oscillation is 500 KHz. Determine the value of C. (Apr/May 2018)

Solution : The given values are,

$$L = 100\ \mu H, C_1 = C_2 = C \text{ and } f = 500\ kHz$$

Now $$f = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

$$\therefore \quad 500\times10^3 = \frac{1}{2\pi\sqrt{100\times10^{-6}\times C_{eq}}}$$

$$\therefore \quad (500\times10^3)^2 = \frac{1}{4\pi^2\times100\times10^{-6}\times C_{eq}}$$

$$\therefore \quad C_{eq} = 1.0132\times10^{-9}\ F$$

but $$C_{eq} = \frac{C_1 C_2}{C_1+C_2} \text{ and } C_1 = C_2 = C$$

$$\therefore \quad C_{eq} = \frac{C\times C}{C+C} = \frac{C}{2}$$

$$\therefore \quad 1.0132\times10^{-9} = \frac{C}{2}$$

$$\therefore \quad C = 2.026\times10^{-9}\ F = \mathbf{2.026\ nF}$$

14. An amplifier in required with a voltage gain of 100 which does not vary by more that 1%. If it is to use negative feedback with a basic amplifier the voltage gain of which vary by 20%, find the minimum voltage gain required and the feedback factor. (Nov/Dec 2018)

Solution:

Closed loop voltage gain of amplifier, A_f is defined as,

$$A_f = \frac{A_m}{1 + A_m\,\beta} \qquad ------(1)$$

$$100 = \frac{A_m}{1 + A_m\,\beta}$$

$$A_m = 100 + 100\,A_m\,\beta \qquad ------(2)$$

Since, feedback voltage gain, A_f does not vary more than 1% and amplifier gain varies by 20% equation (1) can be written as,

$$99 = \frac{0.8\,A_m}{1 + 0.8\,A_m\,\beta}$$

$$0.8\,A_m = 99 + 79.2\,A_m\,\beta \qquad ------(3)$$

Multiplying equation (1) with 0.792 or both sides,

$$0.792\,A_M = 79.2 + 79.2\,A_m\,\beta \qquad ------(4)$$

Subtracting equation (3) and (4),

$$0.008\ A_m = 19.8; \qquad A_n = \frac{19.8}{0.008} \qquad \boxed{\mathbf{A_m = 2475}}$$

Substituting A_m in equation (2),

$$2475 = 100 + 100 \text{ X } 2475 \text{ X } \beta$$

$$\beta = \frac{2475 - 100}{2475\ X\ 100} \qquad \boxed{\mathbf{\beta = 0.0096}}$$

$\therefore$ Feedback factor, β = 0.0096 and minimum voltage gain A_m = 2475 V.

Additional Important Questions:

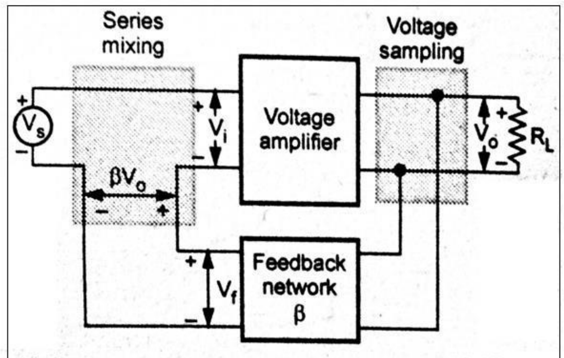
6. Discuss the effect for the following negative feedback amplifiers and derive the expression for input resistance, output resistance and voltage gain for common emitter amplifier.

A. **VOLTAGE SERIES FEEDBACK**
B. **VOLTAGE SHUNTFEEDBACK**
C. **CURRENT SERIES FEEDBACK**
D. **CURRENT SHUNT FEEDBACK**

(A) VOLTAGE SERIES FEEDBACK

Draw circuit of CE amplifier with Voltage Series feedback and obtain the expression for feedback ratio, voltage gain, input and output resistances.

Input is the feedback network is parallel with output of amplifier shunt connection to reduce output resistance R_o series connection at the input increase the input resistance.



Voltage amplifier with voltage series feedback

$$Voltage\ feedback\ factor\ \beta = \frac{V_f}{V_o}$$

Gain

Amplifier Gain $A_v = \frac{V_o}{V_i}$

$$V_o = A_v V_i \quad ---(1)$$

Feedback is connected $V_s = V_i + V_f$; $V_i = V_s - V_f$

Now $V_s = V_i + \beta V_o = V_i + \beta A_v V_i$

$$V_s = V_i(1 + A\beta) \quad ---(2)$$

$$V_i = V_s - V_f \quad \& \quad V_i = I_i R_i$$

$$\therefore V_s = V_i + V_f = I_i\ R_i + A\beta V_i$$

$$= I_i\ R_i + A\beta R_i I_i$$

$$V_s = R_i I_i(1 + A\beta)$$

Now, Input Impedance $Z_{if} = \frac{V_i}{I_i} = \frac{I_i\ R_i(1+A\beta)}{I_i}$

$$= \frac{V_i}{I_i}(1 + A\beta)$$

$$Z_{if} = Z_i(1 + A\beta)$$

Output impedance, $V_o = R_o I_o + AV_i$, $V_i = V_s - V_P$

$$V_s = 0$$

$$V_i = -V_P = \beta V_o$$

$$\therefore V_o = I_oR_o - A\,\beta V_o$$

$$V_o + A\,\beta V_o = I_oR_o$$

$$V_o(1 + A\,\beta) = I_oR_o$$

$$\frac{V_o}{I_o} = \frac{R_o}{1 + A\,\beta}$$

$$Z_o = \frac{R_o}{1 + A\,\beta}$$

$R_o \rightarrow$ *output resistance of amplifier without feedback.*

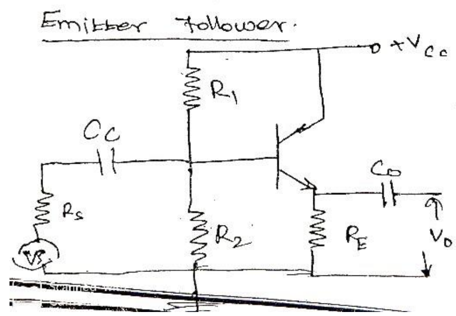
$$A_i = \frac{I_e}{I_b} = \frac{I_b + I_c}{I_b} = 1 + h_{fe}$$

$$R_i = h_{ie} + (1 + h_{fe})R_E$$

$$A_V = \frac{A_C R_L}{R_i} = \frac{(1+h_{fe})R_L}{h_{ie}+(1+h_{fe})R_L} = 1 - \frac{h_{ie}}{R_i}$$

$$R_o = \frac{h_{ie} + R_s}{1 + h_{fe}}$$

$$R_{of} = R_o \parallel R_c$$

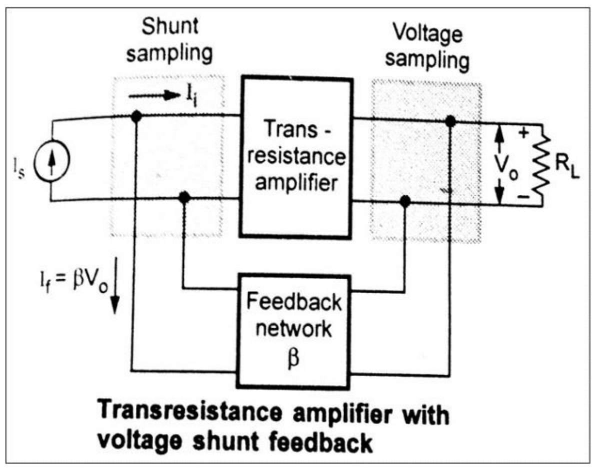


(B) VOLTAGE SHUNT FEEDBACK AMPLIFIER

Draw circuit of CE amplifier with Voltage Shunt feedback and obtain the expression for feedback ratio, voltage gain, input and output resistances. (April / May 2015 -R13)

Trans resistance Amplifier

Connection Diagram:



Transresistance amplifier with voltage shunt feedback

$$Gain: \quad A_F = \frac{V_o}{I_s} = \frac{V_o}{I_i}$$

$$I_s = I_i + I_f$$

$$= I_i + \beta\, V_o$$

$$I_s = I_i + A\,\beta I_i = I_i(1 + A\beta)$$

$$A_F = \frac{V_o}{I_s} = \frac{AI_i}{I_i(1+A\beta)} = \frac{A}{1+A\beta} \text{ without feedback.}$$

$\therefore$ The gain of the amplifier without feedback is reduced by a factor of $(1 + A\beta)$

Input Impedance:

$$Z_i = \frac{V_i}{I_s}; \quad Z_i = \frac{V_i}{I_i + I_f}; \quad Z_i = \frac{V_i}{I_i + \beta V_o}; \quad Z_i = \frac{V_i}{I_i + A\beta I_i}; \quad Z_i = \frac{V_i}{I_i(1 + A\beta)};$$

$$Z_i = \frac{Z_i}{(1 + A\beta)}$$

Input impedance is reduced by the factor $(1 + A\beta)$ for both series, shunt feedback connection.

Output Impedance

$V_o = R_o\, I_o - A\, I_i \qquad I_i = I_S - I_F\,,\ I_f\ I_s\ transferred\ to\ output\ side\ I_s = 0$

$= R_o\, I_o - A\, I_F \qquad \therefore\ I_i = -I_F$

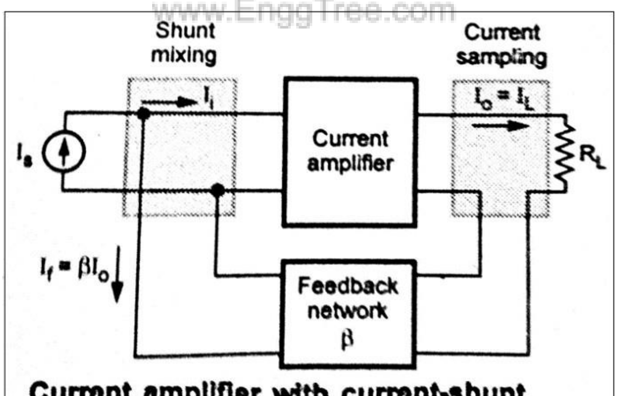
$V_o + A\beta\, V_o = R_o\, I_o \qquad V_o(1 + A\beta) = R_o\, I_o$

$\frac{V_o}{I_o} = \frac{R_o}{1+A\beta}\ Z_o = \frac{V_o}{I_o} = \frac{R_o}{1+A\beta}$

(C) CURRENT SHUNT FEEDBACK AMPLIFIER

Draw circuit of CE amplifier with Current Shunt feedback and obtain the expression for feedback ratio, voltage gain, input and output resistances. (April / May 2015 -R13)

Connection Diagram



Current amplifier with current-shunt feedback

$Amplifier\ \ Gain,\ \ A = \frac{V_o}{I_i} \qquad\qquad I_S = I_i + I_F$

$Feedback\ factor\ \beta = \frac{I_F}{I_o} \qquad\qquad I_F = \beta I_o$

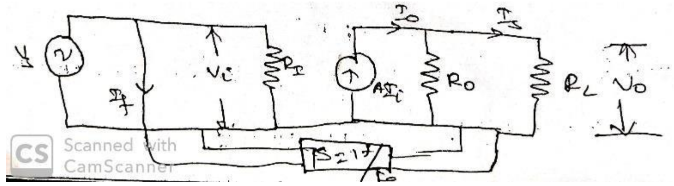
$I_o = AI_i$

Gain of the Amplifier

$$A_F = \frac{I_o}{I_s} = \frac{AI_i}{I_i+I_F} = \frac{AI_i}{I_i+\beta I_o} = \frac{AI_i}{I_i+\beta\ AI_i}$$

$$A_F = \frac{A}{1 + \beta A}$$

Input Impedance:



$$I_s = I_i + I_F$$

$$I_s = \frac{V_i}{R_i} + \beta I_o ; \quad I_s = \frac{V_i}{R_i} + A\beta I_i ; \quad I_s = \frac{V_i}{R_i} + \frac{A\beta V_i}{R_i} ; \quad I_s = \frac{V_i}{R_i}(1 + A\beta)$$

Input resistance of amplifier with feedback R_{if}

$$R_{if} = \frac{V_i}{I_s} = \frac{R_i}{1+A\beta}$$

Output Impedance:

$$I_s = I_i + I_F \qquad I_i = I_s - I_F$$

$I_s = 0,$ Source transferred to output side to calculate the output impedance.

$$I_o = A I_i + \frac{V_o}{R_o}$$

$$\frac{V_o}{R_o} = (1 + A\beta)$$

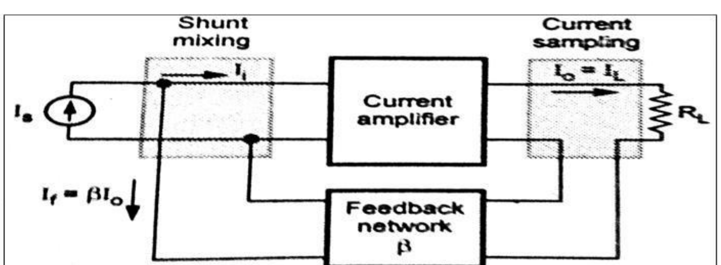
$$R_F = \frac{V_o}{R_o} = R_o(1 + A\beta)$$

Thus, output impedance increased by $(1 + A\beta)$

(D) CURRENT SERIES FEEDBACK AMPLIFIER

Draw circuit of CE amplifier with Current Series feedback and obtain the expression for feedback ratio, voltage gain, input and output resistances. (April / May 2015 -R13)

Transconductance Amplifier:



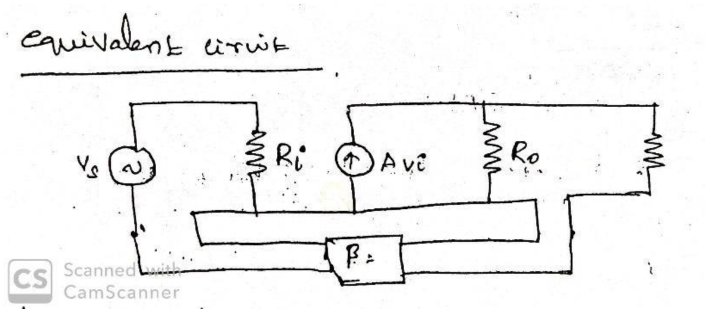
Current amplifier with current-shunt feedback

$$Gain = \frac{I_o}{V_o} = \frac{I_o}{V_i + V_F}$$

$$= \frac{AV_i}{V_i + \beta I_o} \Rightarrow \frac{AV_i}{V_i + A\beta V_i}$$

$$A_F = \frac{AV_i}{V_i(1 + A\beta)} = \frac{A}{1 + A\beta}$$

Equivalent Circuit



Input Impedance:

$V_s = I_i R_i + V_F$

$= I_i R_i + \beta I_o$

$= I_i R_i + A\beta V_i$

$= I_i R_i + A\beta I_i R_i$

$= I_i R_i(1 + A\beta)$

$$Z_i = \frac{V_s}{I_i} = R_i(1 + A\beta)$$

$\therefore$ *Input impedance increased by factor* $(1 + A\beta)$

Output Impedance:

$V_s = 0$

$V_s = V_i + V_F$

$V_i + V_F = 0; \qquad V_i = -V_F$

$$I_o = AV_i + \frac{V_o}{Z_o} = -AV_i + \frac{V_o}{Z_o}$$

$$= -A\beta I_o + \frac{V_o}{Z_o}$$

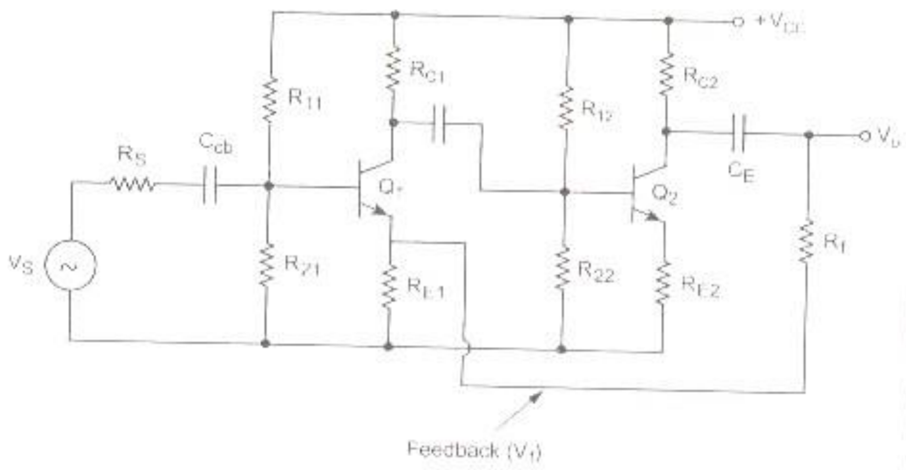
$I_o + A\boldsymbol{\beta}_o = \frac{V_o}{Z_o}; \qquad I_o(1 + A\beta) = \frac{V_o}{Z_o}$

$$Z_{OF} = \frac{V_o}{I_o} = Z_o(1 + A\beta)$$

The output impedance is increased by factor $(1 + A\beta)$

7. Sketch the circuit diagram of a two-stage capacitor coupled BJT amplifier that uses series voltage negative feedback. Briefly explain h$_{oe}$ the feedback operates (Nov/Dec 2015)

It is a shunt or nodal sampling and series mixing. Also cascading means two or more amplifier are connected in series using coupling capacitor or coupling elements. This is shown in fig.



Above fig shows cascaded voltage series amplifier. This analysis of cascaded amplifiers is as follows.

Step 1:

RF and RE1 acts as feedback. The,

i) ß network is directly taken from V_0. Therefore, it is called voltage sampled.
ii) Also βnetwork is not directly connected to base hence it is not shunt mixing and therefore it is series feedback.

Therefore, the voltage series feedback X_0, X_S, X_i, X_f are voltages. Then its analysis is as followings.

Step 2 :

$$\beta = \frac{V_f}{V_0}$$

$$Where V_f = \left(\frac{V_0}{R_f + R_{E1}}\right) R_{E1}$$

$$Also, \beta = \frac{\left(\frac{V_0}{R_f + R_{E1}}\right) R_{E1}}{V_0}$$

$$\therefore \beta = \frac{R_{E1}}{R_f + R_{E1}}$$

Step 3 : $Drawing basic amplifier. =$

$$(i) For the input circuit go to output and put X_0 = 0; i.e., V_0 = 0$$

$$(ii) For output circuit go to input and put I_i = 0$$

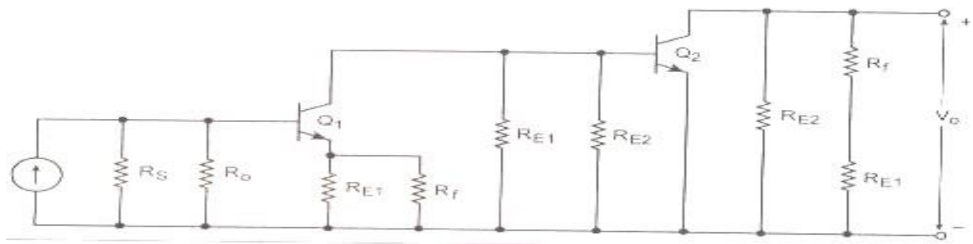
$$Anyhow, \quad R_E = R_{E1} \parallel R_f \quad (or)$$

$$R_E = \frac{R_{E1}\, R_f}{R_{E1} + R_f}$$

$$Also, \quad R_{L2} = R_{C2} \parallel (R_f + R_{E1})$$

$$R_{L2} = \frac{R_{C2} \times (R_f + R_{E1})}{R_{C2} + R_f + R_{E1}}$$

This is the basic amplifier equivalent circuit is as in figure 3.40



Here, the first stage is common emitter connection with feedback resistor $R_f and R_{E1}$ is also called ***global feedback.***

Step 4 : Analysis gives the following results in short,

$i.e.,\qquad D = 1 + A_V\beta$

$$A_{Vf} = \frac{A_V}{D} \text{ or } \frac{A_V}{(1 + A_V\beta)}$$

$$R_{if} = R_i \times D \text{ or } R_i(1 + A_V\beta)$$

$$R_{0f} = \frac{R_0}{D} \text{ or } \frac{R_0}{(1 + A_V\beta)}$$

From the above analysis voltage gain with feedback A_{VF} and output resistance R_{0f} is reduced by $(1 + A\beta)$ times, and input resistance (R_{if}) with feedback is increased by $(1 + A\beta)$ times.