MOHAMED SATHAK AJ COLLEGE OF ENGINEERING

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Sub/ Code : Digital System Design / EC3352

QUESTION BANK

Part – A

UNIT-I

BASIC CONCEPTS

1. **DEMORGAN'S THEOREM [Nov/Dec 2013 R-08] [May/June 2014 R-2013,May/June 2013, R-08],[Nov/Dec2010, April/May2010 R-08], [Nov/Dec 2009],[May 2007]**

   a. **Simplify the following Boolean expression into one literal [Nov/Dec 2014 R-13]**

   W'X(Z'+YZ)+X(W+Y'Z)
   =W'XZ' +W'XYZ+XW+XY'Z
   = W'XZ' + XW+XY'Z+XZW (A+A'B) = A+B
   =W'X(Z+Z')+XW+XY'Z
   = W'X+XW+XY'Z
   =X(W+W') +XY'Z
   = X(1+ZY')
   =X

   b. **Apply De-Morgan's theorem to [(A + B) + C]' [May/June 2014 R-2013]**

   =(A+B)'+C'
   =A'B'+C'

   c. **State Distributive Law. [Nov/Dec 2013 R-08]**

   The distributive law states that ANDing several variables and ORing the result with a single variable is equivalent to Oring the single variable with each of the several variables and then ANDing the sums. The distributive law is

   A+BC = (A+B)(A+C)

   d. **Map the standard SOP expression on a Karnaugh map : (AB)'C + A'BC' + A(BC)' + ABC . [Nov/Dec 2011 R-10]**

   (AB)'C + A'BC' + A(BC)' + ABC = (A'+B')C + A'BC' + A(B'+C') + ABC
   =A'C+B'C+A'BC'+AB'+AC'+ABC

   =A'C(B+B')+B'C(A+A')+A'BC'+AC'(B+B')+AB
   =A'BC+A'B'C+AB'C+A'B'C+A'BC'+ABC'+AB'C'+ABC
   =A'BC+A'B'C+AB'C+A'BC'+ABC'+AB'C'+ABC
   =m3+m1+m5+m2+m6+m4+m7
   =∑m(1,2,3,4,5,6,7)

K map

A \ BC	00	01	11	10
0	0	1	1	1
1	1	1	1	1

e. What is a totem output? [April/May 2011 R-08]

A type of output structure used with integrated circuits in which one transistor drives the output high while another transistor connected below it pulls the output low.

f. **What is the significance of high impedance state in tri-state gates? [Nov/Dec2010 R-08]**

i)Logic behaves like an open circuit.

ii)Circuit connected to three-state gate is not affected by inputs to the gate.

g. What are Don't care terms? [May/June 2013, R-08]

Don't-care term is an input-sequence (a series of bits) to a function that the designer does not care about, in that input would not result in any changes to the output. it may also be called an X value.

e. State DeMorgan's theorem. [May/June 2013, R-08] [April/May2011 R-08], [Nov/Dec2010 R-08], [April/May2010 R-08], [Nov/Dec 2009],[May 2007]

(i) (A+B)'=A'.B'

(ii)(A.B)'=A'+B'

f. Mention any two applications of Demorgan's theorem. (May 2007)

Simplification of Boolean expression and to convert AND to OR and vice versa

Very high impedance, high-Z, or more commonly Hi-Z.

Advantages

The high impedence state of a tristate allows the possibility of making the direct wire connection from many outputs to a common bus line, in which only one output line will be enabled while all other outputs are disabled by their respective control inputs.

g. What are the disadvantages of Karnaugh mapping technique? [Nov/Dec2010]

(i) As the number of variables increases it is difficult to make judgements about which combinations from the minimum expression.In case of complex problem with 7,8, or even 10 variables it is almost an impossible task to simplify expression by the mapping method.

(ii) K-map simplification is manual techniques and simplification process is heavily depends on the human abilities

a. **is Prime Implicant? [Nov/Dec 2013 R-08]**
Prime implicant is a product term obtained by combining the maximum possible number of adjacent squares in the map

2. **BINARY CONVERSION** [**May/June 2014 R-2013**] ,**[Nov/Dec2010], [April/May2010], [Nov/Dec 2009]**

a. Convert 0.35 to equivalent hexadecimal number [**May/June 2014 R-2013**]

0.35x16=5.6
0.6x16=9.6
0.6x16=9.6
$=0.599_{16}$

b. What is the gray code for 9?Represent 9 in 2421 coding?[Nov/Dec2010]
Gray code is 1101 and 2421 code is 1111.

c. An 8 bit transistor register stores decimal 240.What is the binary output of the register?[April/May2010]

2	240
2	120-0
2	60 -0
2	30 -0
2	15 -0
2	7 -1
2	3 -1
	1 -1

Binary output of the register is 11110000

d. Convert $(11001011)_2$ into gray code. [Nov/Dec 2009]
$(11001011)_2$ =10101110

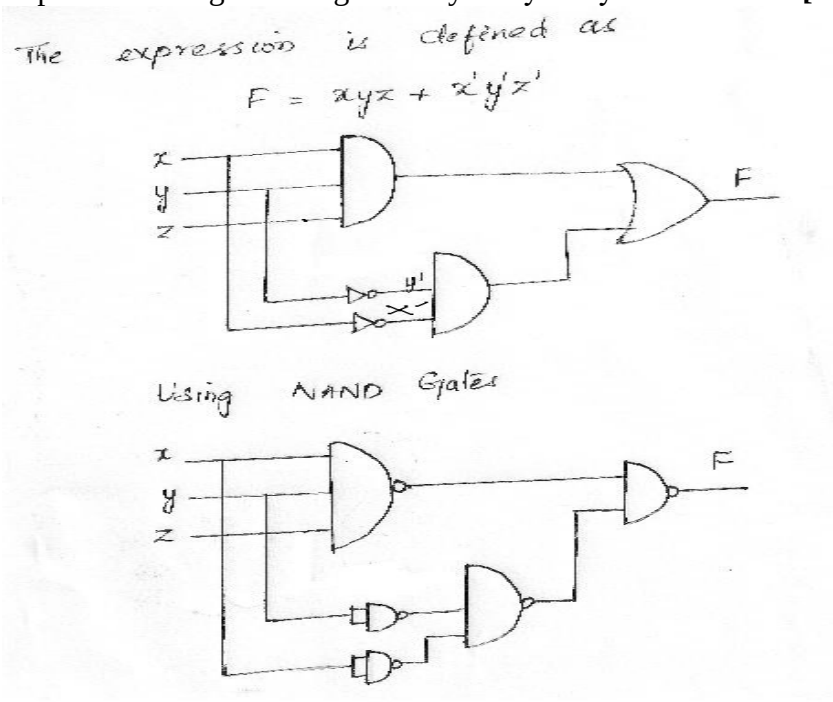
e. Subtract using 2s complement method: $(74)_{10}$-$(85)_{10}$. [April/May2010]
$(85)_{10}$=1010101
$(74)_{10}$=1001010
2s complement of 1010101 is 0101011

```
  0101011
(+) 1001010
 ----------
  1110101
```

There is no carry,Answer is a negative number.2s complement of result is 0001011.

3. **IMPLEMENTATION USING GATES. [Nov/Dec 2011 R 10] [April/May2010],[Nov 2007]**

a. Implement Using NAND gates only F=xyz+x'y' **[May/June 2012 R-08]**

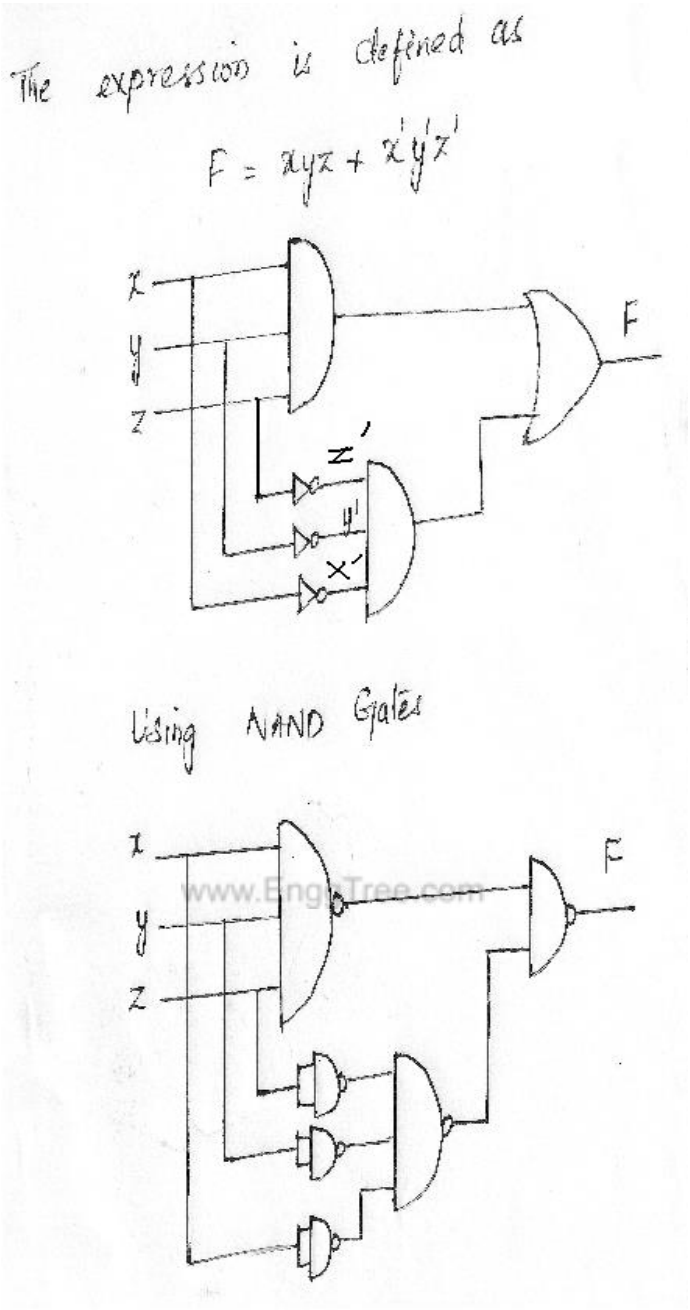


b. **Implement the given function using NAND gates F(x,y,z) =∑(0,6).** **[Nov/Dec 2012, R-08]**

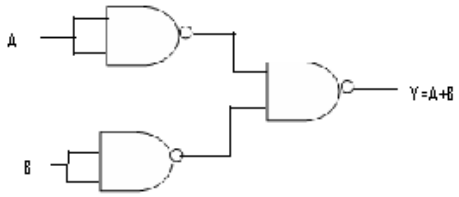
K map

Z \ xy	00	01	11	10
0	1			
1				1

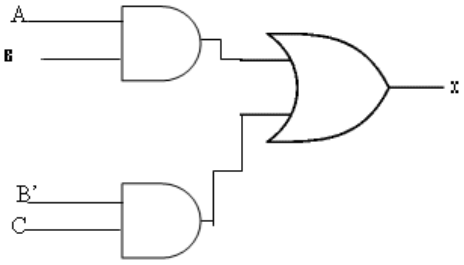
= xyz+x'y'z'



c. **Draw the logic diagram of OR gate using universal gates. (or)Implement OR gate using NAND gates [Nov/Dec 2011 R 10] [April/May2010]**



d. **Draw the logic diagram for X=AB +B'C. (Nov 2007)**



e. **Implement F = (AB' + A'B)(C+D') with only NOR gate.(Nov 2007)**

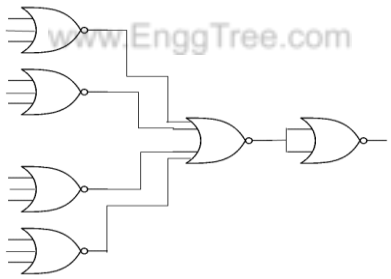
F = (AB' + A'B)(C+D')

F = AB'C +A'BC +AB'D'+A'BD'

F' = (AB'C +A'BC +AB'D'+A'BD')'

= (AB'C)'(A'BC)'(AB'D')'(A'BD')'

F ' = (A'+B+C')(A+B'+C')(A'+B+D)(A+B'+D)



f. **Show that positive logic NAND gate is a negative logic NOR gate. [Nov/Dec 2009 R-08]**

Truth Table for NAND Gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

≡

Truth Table for + ive logic NAND gate

A	B	Y
LOW	LOW	HIGH
LOW	HIGH	HIGH
HIGH	LOW	HIGH
HIGH	HIGH	LOW

Positive logic

HIGH=Logic 1

LOW= Logic 0

4. SIMPLIFICATION OF BOOLEAN FUNCTION [April/May 2011 R-08],[Nov/Dec 2009 R-08],[Nov 2007],[May 2007],[May 2006]

a. Simplify the given boolean expression F=x'+xy+xz'+xy'z'
[Nov/Dec 2012, R-08]

F=x'+xy+xz'+xy'z'
= x'+ x(y+z'+y'z')
= x'+x(y+z'(1+y'))
= x'+x(y+z')
=x'+xy+xz'
= x'+y+xz' Since x'+xy = x'+y
=x'+y+z' x'+xz' = x'+z'

b. Simplify the following Boolean expression to a minimum number of literals (BC'+A'D) (AB' + CD'). [April/May 2011 R-08]

(BC'+A'D) (AB' + CD') = AB'.BC'+BC'.CD'+AD'.AB'+A'D.CD'=0
(X.X'=0)

c. **Prove that the logical sum of all minterms of a Boolean function of 2 variables is 1. [Nov/Dec 2009 R-08]**

For two variables A and B minterms are: A'B',A'B,AB',AB.
The logical sum of these minterms is,
F= A'B'+A'B+AB'+AB
=A'(B'+B)+A(B'+B)
=A'+A =1

d. (a)Express F= A+B'C as sum of minterms. (Nov 2007)
(b) Find the standard sum for the following function
f = x1x2x3 x1 x3 x4 + x1 x2 x4.
(May 2006)

Ans:
(a)F= A+B'C
The function has three variables A,B,C . The first term A is missing two variables B and C.The second term is missing one variable so
F= A(B+B')(C+C')+(A+A')B'C
= ABC+ABC'+AB'C'+AB'C+A'B'C+AB'C
= ABC+ABC'+AB'C'+AB'C+A'B'C since (x+x = x)
= m7 +m6+m4 + m5+m1 (arrange in ascending order)
= m1+m4+m5+m6+m7
(b)f = x1 x2 x3 + x1 x3 x4 + x1 x2 x4.
f = x1 x2 x3 + x1 x3 x4 + x1 x2 x4
= x1 x2 x3(x4+x4') + x1(x2+x2') x3x4+x1x2(x3+x3') x4
= x1x2x3x4 +x1x2x3x4'+x1x2'x3x4 + x1x2x3'x4

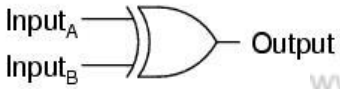
e. Simply the following Boolean function: (May 2007)

(a) x(x'+y)
(b) xy + x'z +yz
(c) f = x(y+w'z)+wxz
(d) x1 + x1x2 (May 2006)
Ans:
(a) x(x'+y)
= xx' + xy (xx' =0)
= xy
(b) xy + x'z + yz (by consensus theorem)
= xy + x'z
(c) F = x(y+w'z) + wxz
= xy + xw'z + wxz
= xy +xz(w' + w)
= xy +xz
(d) x1 + x1x2
= x1(1+x2)=x1

5. <u>GATES</u> [Nov 2008], [May 2008]

a. Write the Boolean function of an XOR gate ,give its truth table. [Nov 2008].

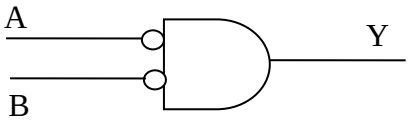
Exclusive-OR gate



A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

Y=A'B+AB'

b. Find the relation between the I/Ps and O/P, shown in figure. Name the operation performed. [May 2008]



Y = A'.B' =(A+B)'
This gate performs the NOR operation.

c. Define Fan-out of a Digital IC. [April/May 2011 R-08] (Nov 2007)

Fan-out is defined as the maximum number of input of the same IC family that the gate can drive maintaining its output level within the specified limits

d. What is propagation delay of a gate? (May 2007),[Nov 2006]

Propagation delay is the average transition delay time for a signal to propagate from input to output when the binary signals change in value. The signal through a gate take a certain amount of time to propagate from input to the output. This interval of time is defined as the propagation delay of the gate, It is expressed in nanoseconds.

e. A certain gate draws 2 mA when its output is high and 3.6 mA when its output is low.
What is the average power dissipation if Vcc is 5V and it is operated on a 50% duty
cycle? (Nov 2006)

Given

I_{CCH} = 2 mA,I_{CCL} = 3.6 mA

The average Icc is given as

$I_{CC(avg)} = I_{CCH} + I_{CCL} / 2$

= (2+3.6)/2

= 2.8 mA

Then average power dissipation is given as

$P_{D(avg)} = I_{CC(avg)}$ X Vcc

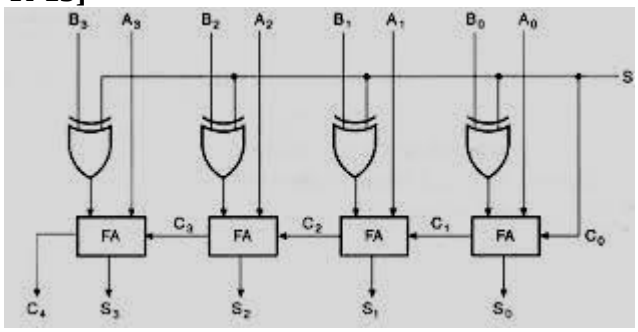
= 2.8 mA X 5V

= 14 mW

UNIT –II
COMBINATIONAL LOGIC CIRCUITS

1. **ADDER AND SUBTRACTOR [Nov/Dec2014 R-13] [Nov/Dec2013 R-08]** [**May/June 2014 R-2013**] **[May/June 2013 R-08] [Nov/Dec2011 R-10], [Nov/Dec2011 R-08],[April/May2011 R-08] ,[Nov/Dec2010 R-08], [April/May2010 R-08], [Nov/Dec 2009 R-08], [May2006\May2007]**

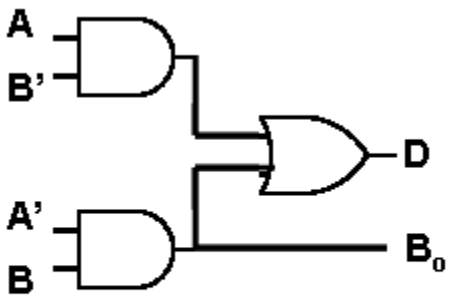
a. Construct 4-bit parellel adder/subtractor using Full adders and XOR gates **[Nov/Dec2014 R-13]**



b. Enumerate some of the combinational circuits [Nov/Dec2013 R-08]
a) Comparator b) Multiplexer c) Demultiplexer/Decoder d) Full adder
e) Shifter

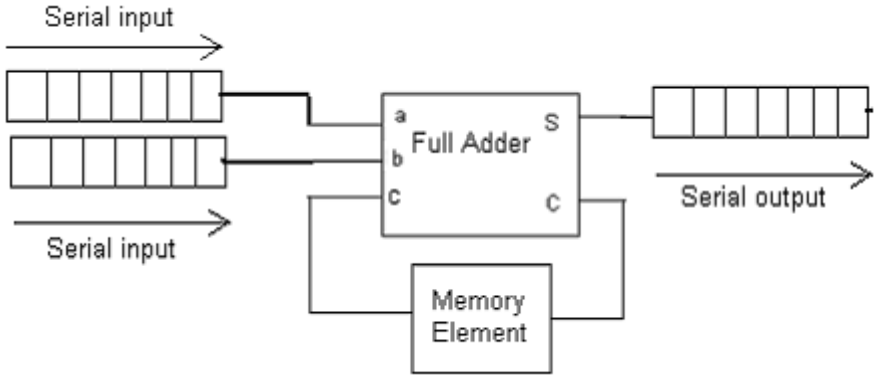
c. Design a halfsubtractor using basic gates [May/June 2013 R-08]

x	y	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0



Half Subtractor implementation using AND-OR

d. Draw the logic diagram of serial adder [Nov/Dec 2012, R-08]



e. Give the logical expression for sum output and carry output of a full adder . [Nov/Dec2011 R-10]

Sum :

$$S = A \oplus [B \oplus C_{IN}]$$

Carry:

$$C_{OUT} = BC_{IN} + AC_{IN} + AB$$

f. What is meant by look ahead carry? [Nov/Dec2011 R-08]

g. Compare the performance of binary serial adder and parallel adders . [Nov/Dec2011 R-08]

Parallel adders	Serial adder
1.Parallel bit addition 2.high speed of operation 3.requires large amount of logic circuitry that increases in direct proportion with number of bits	1.Bit by bit addition 2.low speed of operation 3.requires simpler circuitry

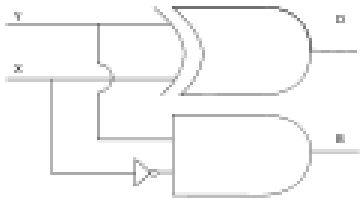
h. Write the logic expressions for the difference and borrow of a half subtractor. [April/May2011 R-08]

$$D = y \oplus x$$
$$B = \overline{x} \cdot y$$

i. Design a half-subtractor combinational circuit to produce the outputs Difference and Borrow. [Nov/Dec2010 R-08]

x	y	D	B

0 0 1 1	0 1 0 1	0 1 1 0	0 1 0 0



j. Relate Carry generate, Carry Propagate, Sum and Carry-out of a Carry look ahead adder. [Nov/Dec2010 R-08]

Carry generate $G_i=A_iB_i$
Carry Propagate $P_i=A_i$ Ex-or B_i
Sum $S_i= P_i$ Ex-or C_i
Carry $C_i+1=G_i+P_iC_i$

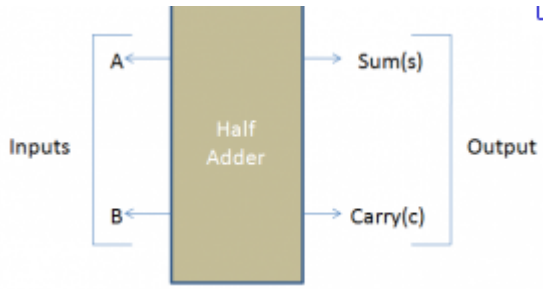
k. **Write an expression for borrow and difference in a full subtractor circuit. [April/May2010 R-08]**

$$D = X \oplus Y \oplus Z$$
$$B = Z \cdot (\overline{X \oplus Y}) + \overline{X} \cdot Y$$

l. Suggest a solution to overcome the limitation on the speed of an adder. [Nov/Dec 2009 R-08]

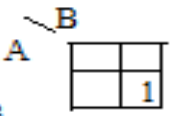
Look Ahead-Carry generator(Fast adder) with look ahead –carry addition is used to overcome the limitation of an adder.It speeding up the addition process by eliminating inter stage carry delay.

m. Represent a half adder in block diagram form and also its logic implementation. (May2006\May2007)



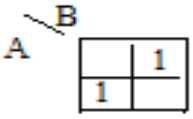
Inputs		Y = A+ B	
A	B	carry	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Carry



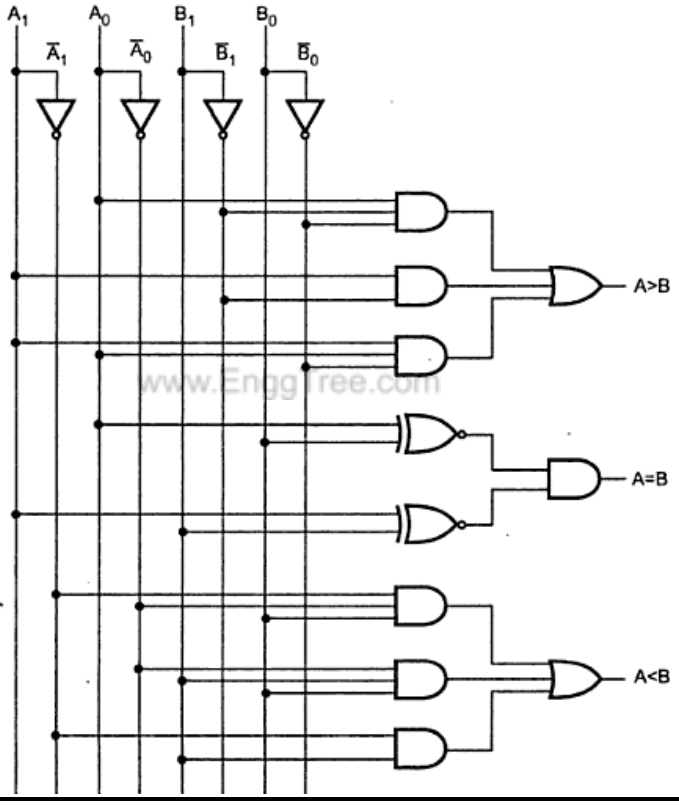
Carry = AB

Sum



Sum = A'B+AB'

n. Draw the logic, circuit of a 2 bitcomparator [May/June 2014 R-2013]

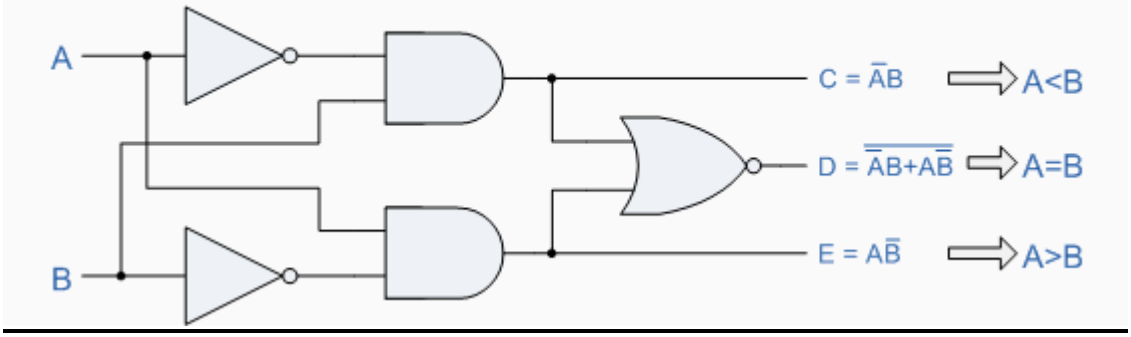


o. Design a single bit magnitude comparator to compare two words A and B. [April/May2011 R-08]

Truth table

Inputs		Outputs		
B	A	A > B	A = B	A < B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

1-bit Comparator



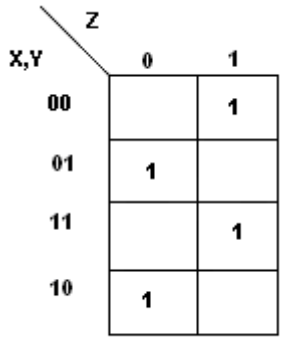
2. **PARITY GENERATOR/CHECKER [Nov/Dec2010], [April/May2010 R-08], (May 2006)**

a. Design a three bit even parity generator [Nov/Dec 2012, R-08]

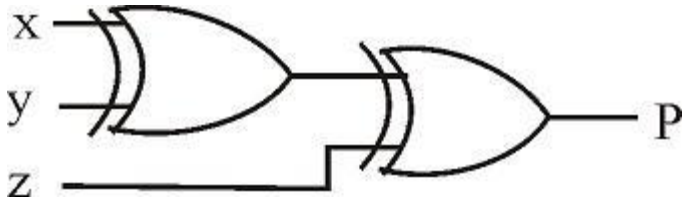
Truth table:

Message X Y Z	Even parity bit P	Checker bit C
0 0 0	0	0
0 0 1	1	0
0 1 0	1	0
0 1 1	0	0
1 0 0	1	0
1 0 1	0	0
1 1 0	0	0
1 1 1	1	0

K-map

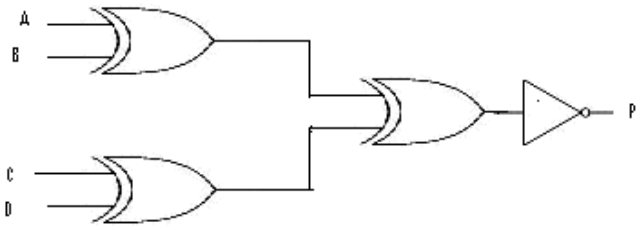


$$P = \overline{X}\overline{Y}Z + \overline{X}Y\overline{Z} + XYZ + X\overline{Y}\overline{Z} = X \oplus Y \oplus Z$$

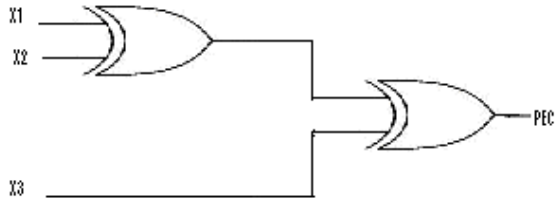


b. **What is PARITY bit?How is checking done? [Nov/Dec2010]**
A parity bit is an extra bit included with a binary message to make the number of 1s either odd or even.
In even parity checking, an additional bit is added to the number of set bits to make the total number of 1's in the data (including the parity bit) an even number. Also, for **the odd parity checking**, an additional bit is added to make the total number of binary 1 in the set of bits an odd number.

c. **Draw the circuit diagram for 4 bit Odd parity generator. [April/May2010 R-08]**

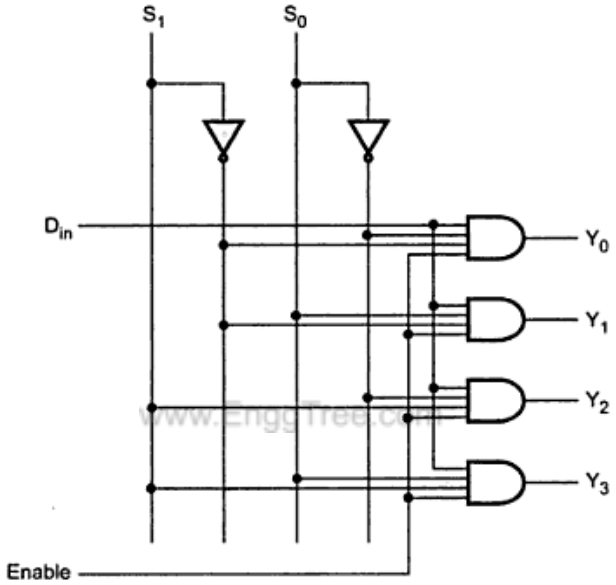


d. Draw a parity checker circuit for 3 bit binary word x1 x2 x3. (May 2006)

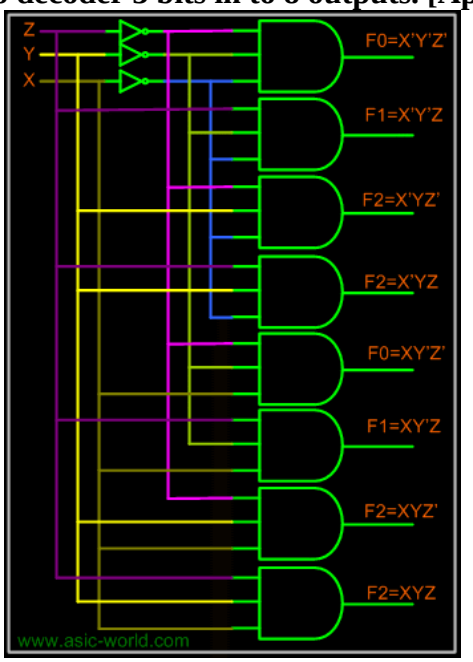


3. <u>DECODER AND DEMULTIPLEXER</u> [Nov/Dec2014 R-13] [April/May2010], [Nov/Dec 2009 R-08], (Nov 2006)

a. Convert a 2 to 4 line decoder with enable input to 1x 4 demultiplexer [Nov/Dec2014 R-13]



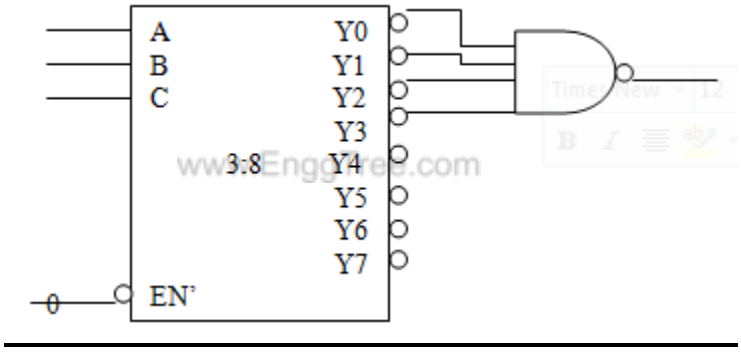
b. Sketch decoder circuit to decoder 3 bits in to 8 outputs. [April/May2010]



c. Differentiate a decoder from a demultiplexer. [Nov/Dec 2009 R-08]

S. No	Decoder	Demultiplexer
1	Decoder is a many inputs to many outputs device	It is a one input to many outputs device.
2	There are no selection lines	The selection of specific output line is controlled by the value if selection lines.

d. Realize S(X,Y,Z) =∑(1,2,3,4) using an appropriate decoder and an external logic gate. (Nov 2006)



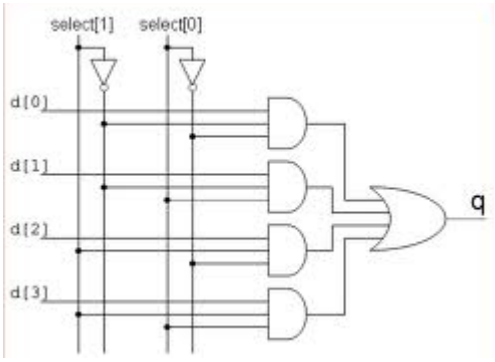
a. **<u>MULTIPLEXER</u> [Nov/Dec 2013 R-08][May/June 2013 R-08] [May/June 2012 R-08][Nov/Dec 2011 R-08] [Nov/Dec 2009], (May 2008), (Nov 2007), (May 2007)**

b. **List out various applications of Multiplexer][Nov/Dec 2013 R-08]**

Multiplexer are used in various fields where multiple data need to be transmitted using a single line. Following are some of the applications of multiplexers.

1. Communication system 2.Telephone network 3.Computer memory 4. Transmission from the computer system of a satellite

c. **Draw the Logic diagram of 4x 1 Mux [May/June 2013 R-08]**

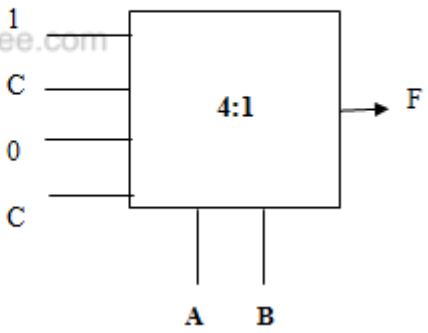


b. List few applications of multiplexer? [May/June 2012 R-08]

a. Data routing
b. Logic function generator
c. Control sequencer
d. Parallel-to-serial converter

c. Realize the Boolean function using appropriate multiplexer F(A,B,C) = Σ(0,1,3,7).[Nov/Dec 2011 R-08]

	C'	C
1	0	1
C	2	3
0	4	5
C	6	7

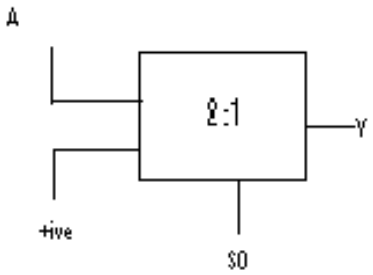


d. Realize an OR gate using 2:1 MUX. [Nov/Dec 2009],

Truth table of OR gate

A	B	Y=A+B
0	0	0
0	1	1
1	0	1
1	1	1

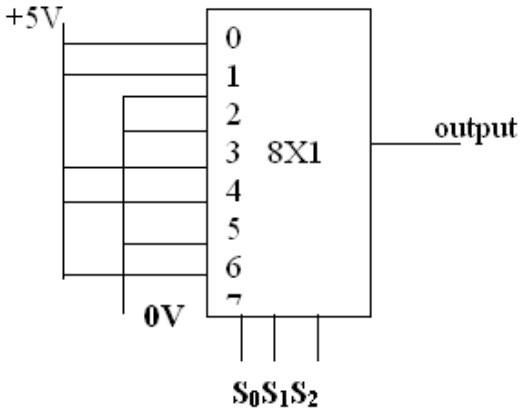
	I_0	I_1
A'	0	1
A	2	3
	A	1



e. **Write the truth table of a 4:1 multiplexer. (May 2008)**

S_0 S_1	Output
00	I_0
01	I_1
10	I_2
11	I_3

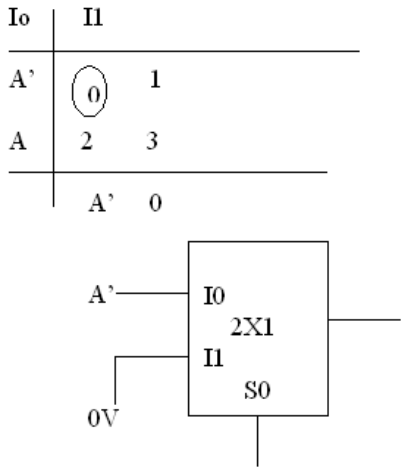
f. **Implement the function f = ∑ m(0,1,4,5,7) using 8:1 MUX . (Nov 2007)**



g. Design a 2 input NAND gate using 2: 1 multiplexer. (May 2007)

A	B	Y

0	0	1
0	1	0
1	0	0
1	1	0



4. <u>CODE CONVERSION</u> (Nov 2008)

a. Convert 0.35 to equivalent hexadecimal number. [**May/June 2014 R-2013**]

b. Express Gray code 10111 into binary numbers. (Nov 2008)

$10111 – (11010)_2$

c. Convert $(367)_{10}$ into Excess -3 code. (Nov 2008)

367 BCD 0011 0110 0111 to excess-3 0110 1001 1010

d. What are the major categories of logic circuits? (May 2007)

The major categories of logic circuits are combinational logic circuit and sequential logic circuit.

e. Define priority encoder. [**May/June 2014 R-2013**] **(Nov 2006)**

Encoders establish an input priority to ensure that only the highest-priority input line is encoded. If priority is given to an input with higher subscript number over one with lower subscript number, then if both D2 and D5 are logic-1 simultaneously, the output will be 101 because D5 has a higher priority over D2.

Inputs								Outputs		
D0	D1	D2	D3	D4	D5	D6	D7	X	y	z
1	0	0	0	0	0	0	0	0	0	0
X	1	0	0	0	0	0	0	0	0	1
X	X	1	0	0	0	0	0	0	1	0
X	X	X	1	0	0	0	0	0	1	1
X	X	X	X	1	0	0	0	1	0	0
X	X	X	X	X	1	0	0	1	0	1
X	X	X	X	X	X	1	0	1	1	0
X	X	X	X	X	X	X	1	1	1	1

UNIT –III
SYNCHRONOUS SEQUENTIAL CIRCUITS

1. RACE AROUND CONDITION [Nov/Dec2013 R-08] [May/June 2012 R-08] [Nov/Dec2010 R-08], [Nov/Dec 2009], [May 2008]

a. Define: Latches [Nov/Dec2013 R-08]

Latches and flip-flops are the basic elements for storing information. One latch can store one bit of information. In latches, outputs are constantly affected by their inputs as long as the enable signal is asserted. In other words, when they are enabled, their content changes immediately when their inputs change. Flip-flops, on the other hand, have their content change only either at the rising or falling edge of the enable signal. This enable signal is usually the controlling clock signal. After the rising or falling edge of the clock, the flip-flop content remains constant even if the input changes.

b. Difference Between Edge triggering and Level triggering [May/June 2012 R-08] [April/May2010 R-08]

Edge triggering	Level triggering
1The input signal is sampled at the rising edge or falling edge of the clock signal. 2) It is not-sensitive to Glitches. Example: Flipflop	1the input signal is sampled when the clock signal is either high or low. 2) it is sensitive to glitches. example: latch.

c. How do you eliminate the race around condition in a JK flip-flop? [Nov/Dec2010 R-08]

Race around condition can be eliminated by using a master-slave JK flipflop.Master flip-flop is loaded with input data when clock=0 and slave flip-flop transfers the data to output when clock=1.

d. What is race around condition? [Nov/Dec 2009], [May 2008]

If output is feedback to the input and therefore change in the output results change in the input. Due to this in the positive half of the clock pulse if j and k are both high then output toggles continuously. This condition is known as race around condition

e. Draw the state table and excitation table of T flip-flop. [Nov/Dec2010 R-08], [April/May2010]

CharacteristicTable Excitation Table

T	Q(t+1)
0	Q(t) No Change
1	Q'(t) Complement

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

f. What is meant by parallel and serial data communication? [Nov/Dec2010]

Serial data Communication-Information is transferred one bit at a time while the registers are shifted in the same direction during one clock pulse.

Parallel data Communication-Information is available from all bits of a register and all bits can be transferred simultaneously.

g. What is special about state diagram? [Nov/Dec2010]

State diagram is a pictorial representation of a behavior of a sequential circuit.Here the state is represented by the circle, and the transition between states is indicated by directed lines connecting the circles.A directed line connecting a circle with itself indicates that next stat is same is same as present state.

h. What do you understand by refreshing with reference to memory devices?[Nov/Dec2010]

The dynamic RAM stores the binary information in the form of electric charges on capacitor. The capacitors are provided inside the chip by MOS transistors. The stored charge on the capacitors tends to discharge with time and the capacitors must be peiodically recharged by refreshing the dynamic memory.

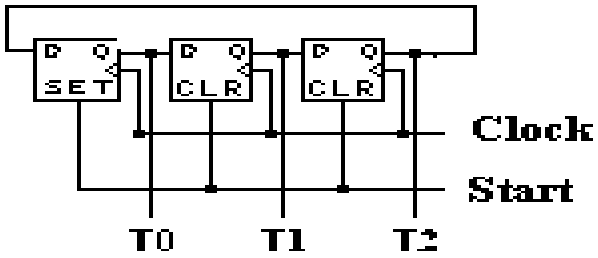
2. <u>COUNTERS</u> [May/June 2014 R-2013, [Nov/Dec2014 R-13] Nov/Dec 2011 R-08] [April/May2010 R-08], [April/May2010], [Nov/Dec 2009],[Nov 2008], (Nov 2006)

a. **How does a ripple counter differ from synchrounous counter [Nov/Dec2014 R-13] Compare the logics of synchronous counter and ripple counter [May/June 2014 R- 2013]**

The ripple counter (Asynchrounous counter) differs from synchrounous counter in such a way that

Asynchrounous counter	Synchrounous counter
1. In this type of counter Flip flops are connected in such a way that output of first flip flop drives the clock for the next flip-flop.	1. In this type there is no connection between output of first flip-flop and clock input of the next flip-flop.
2. All the flip-flops are not clocked simultaneously.	2. All the flip-flops are clocked simultaneously.
3. Logic circuit is very simple even for more number of states.	3. Design involves complex logic circuit as number of states increases.

b. Design a 3- bit ring counter and find the mod of the designed counter [Nov/Dec 2012, R-08]



The designed counter is Mod-8 counter.

c. A 4 bit binary ripple counter is operated with clock frequency of 1 KHz. What is the output frequency of its third Flipflop? [Nov/Dec 2011 R-08]

Frequency of third flipflop is $f_o/2^3 = f_o/8 = 1$ KHz/8 =125 Hz

d. **What is meant by Programmable counter?Mention its application.**
[April/May2010R-08]

In most synchronous counters can also be pre-located with a binary number in parallel from prior to count operation.This prelocating capability makes it possible to begin a count sequence from 0 to any other number.Such counters are said to be programmable.

Applications: Counters are used a frequency dividers in digital time pieces, such as electronic digital clocks,automobile digital clock and wrist watches,frequency counters,oscilloscope ans television receivers.

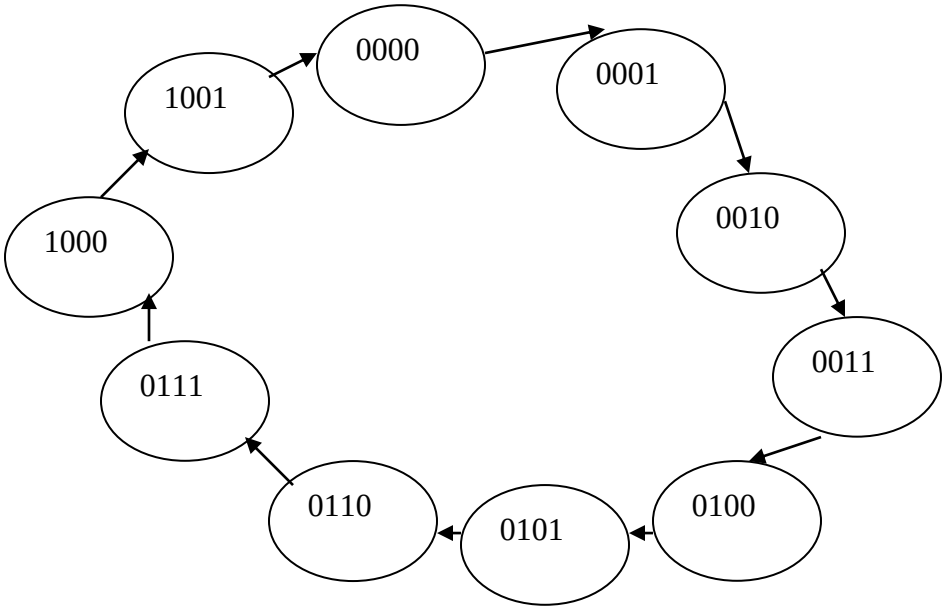
e. What is ring counter? [April/May2010]

The Q output of each stage is connected to the D input of the next stage and the output of last stage is fed back to the input of first stage.The CLR' followed by PRE' makes the output of first stage to '1' and remaining outputs are zero.The ring counter can be used for counting the number of pulses.

f. A binary ripple counter uses 7 flipflops.How many distinct states does the counter have? What is the largest binary number that can be stored in the ripple counter? [Nov/Dec 2009]

127 states and the largest binary number is $128(2^n)$

g. Draw the state diagram of MOD-10 counter. (Nov 2008).

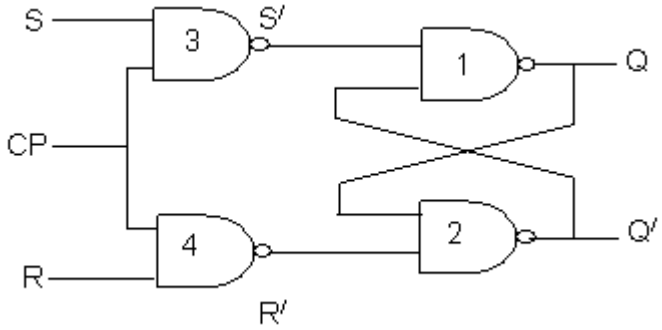


h. Define synchronous counter. (Nov 2006)

A counter is a register capable of counting the number of clock pulses arriving at its clock input. Count represents the number of clock pulses arrived. Two types of counter synchronous and asynchronous .In synchronous counter the common clock input is connected to all of the flip-flop and thus they are clocked simultaneously

3. JK FLIP-FLOP [May/June 2014 R-2013, Nov/Dec 2013 R-08] [Nov/Dec2014 R-13] [May/June 2013 R-08] [May/June 2012 R-08] [Nov/Dec 2011 R-08] ,[April/May 2011 R-08], [Nov/Dec 2009 R-08],[Nov 2007],[May 2007], (Nov 2006),[May 2006]

a. Sketch the logic 'diagram of a clocked SR flip flop ?[May/June 2014 R-2013]



b. Write short notes on Digital Clock. [Nov/Dec 2013 R-08]

A digital clock is a type of clock that displays the time digitally. Digital clocks typically use the 50 or 60 hertz oscillation of AC power or a 32,768 hertz crystal oscillator as in a quartz clock to keep time. To represent the time, most digital clocks use a seven-segment LED, VFD, or LCD display for each of four digits. digital clocks can be very small and inexpensive devices and they are often incorporated into all kinds of devices such as cars, radios, televisions, microwave ovens, etc

c. How many flip flops are required to build a binary counter that counts from 0 to 1023? [May/June 2013 R-08]

The number of flip flops required is given by

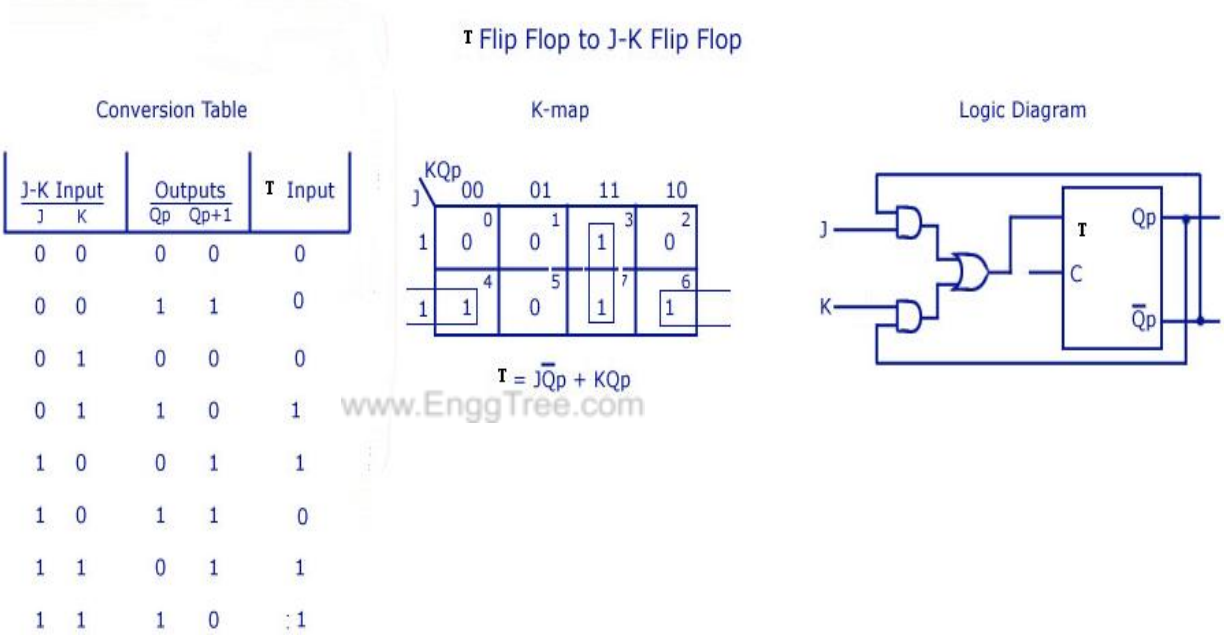
2^n >= Count

n = no of flip flops

2^n >= 1023

n = 10

d. **Realise JK Flip flops [Nov/Dec2014 R-13]**
Realise T flip flop to JK flip flop [May/June 2012 R-08]

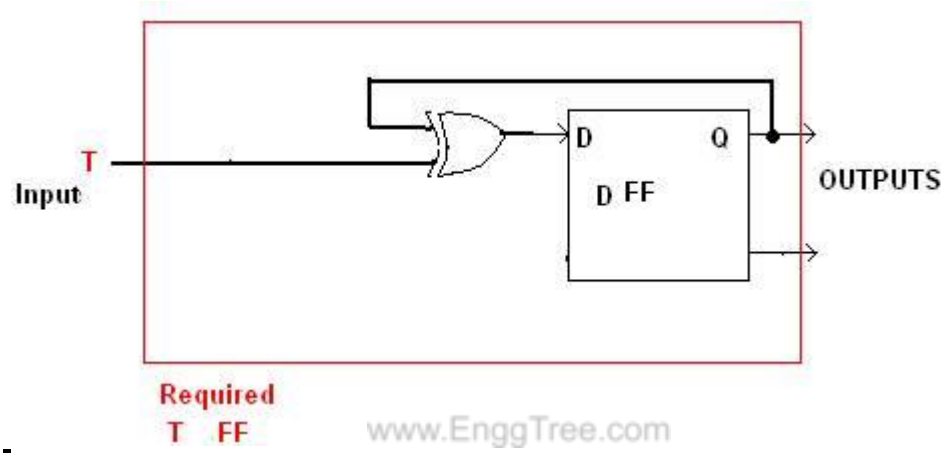


e. How D flip flop converted into T flip flop. [Nov/Dec 2012, R-08] [May/June 2013 R-08]

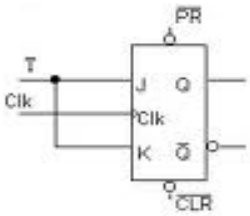
Q	Q(n+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

Q	Q(n+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

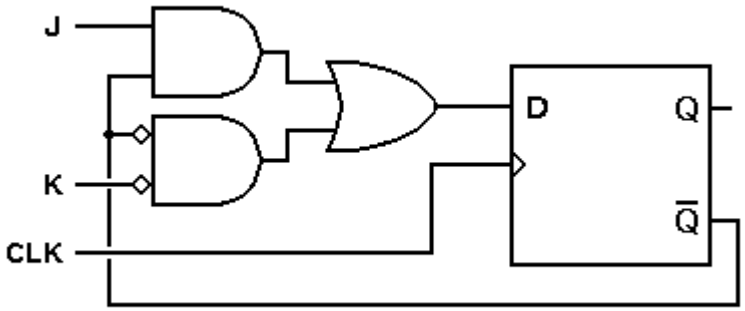
D= T xor Q = T Q_n' + T'Q_n



f. **Draw the logic diagram of T flip flop using JK flip flop. [Nov/Dec 2011 R-10]**



g. **Realize JK flipflop using D Flipflop. [Nov/Dec 2011 R-08]**



h. Write down the characteristic equation for JK flipflop.[April/May 2011 R-08], [Nov/Dec 2009 R-08],[Nov 2007], (Nov 2006)
What are the next state equations of RS and JK FFs?
$Q_{n+1}=JQ_n'+K'Q_n$
$Q_{(n+1)} = S +R'Q$

i. Write the excitation tables of JK and D flip flop. [Nov 2007]

Q	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

Q	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

j. How does a J-K flip-flop differ from an S-R flip flop in its basic operation? (May 2007),[Nov 2006]
A JK flip-flop is a refinement of the RS flip-flop in that the indeterminate state of the RS is defined in the JK type. Inputs J and K behave like inputs S and R to set

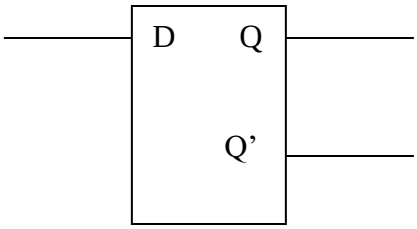
and clear the flip-flop When inputs are applied to both J and K simultaneously, the flip-flop switches to its complement state, that is ,if Q = 1 it switches to Q = 0 and vise versa .

k. What is a flip –flop? (May 2006)

A flip-flop circuit can maintain a binary state indefinitely (as log as power is delivered to the circuit) until directed by an input signal to switch states. The major differences among various types of flip-flops are in the number of inputs they possess and in the manner in which the input affect the binary state.

l. Draw the logic symbol and truth table of a D flip flop. (May 2008)

Q	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

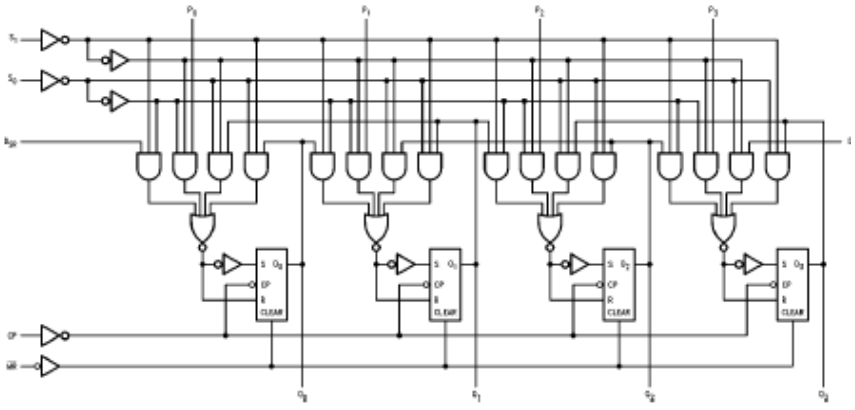


4. <u>SHIFT REGISTER</u> [Nov/Dec 2011 R-10],(May 2007)

c. How can a SIPO register be used as a SISO register? [Nov/Dec 2011 R-10]

Output of each flip flop must be connected to the input of immediate next flip flop.The output must be taken from the last flip flop.

d. Draw the logic diagram of 4 bit universal shift register. (May 2007)



e. Classify the register with respect to serial and parallel input output. (May 2007)

The shift register can be classified in to (i) Serial in serial out (ii) Serial in parallel out (iii)parallel in serial out (iv) Parallel in parallel out

UNIT – IV
ASYNCHRONOUS SEQUENTIAL CIRCUITS

1. **VERILOG AND ASM CHART [Nov/Dec2014 R-13] [May/June 2014 R-2013], [Nov/Dec 2012, R-08] [April/May 2011 R-08] [Nov/Dec2010 R-08]**

   a. Define ASM Chart. List its three basic elements.[Nov/Dec2014 R-13]

   An **ASM chart** is a method of describing the sequential operations of a digital system.

   The three basic elements are

   1. State Box
   2. Decision Box
   3. Conditional Box

   b. Write the VHDL code for a half adder. [May/June 2014 R-2013]

```
entity half_adder_df is
port (      A,B : in bit; --input ports
            Sum, Carry : out bit); --output ports
end half_adder_df;

begin
Sum <= (not A and B) or (A and not B) after 20 ns;
Carry <= A and B after 10 ns;
end data_flow_view;
```

   c. Design a 3-input AND gate using verilog [Nov/Dec 2012, R-08]

```
module three_and_gate(a, out) ;
 input [2:0] a ;
output out ;
wire out ;
assign out = a[0]&a[1]&a[2] ;
endmodule
```

   d. What are the basic building blocks of a Algorithmic state machine chart?[April/May 2011 R-08]

   The basic building blocks of a ASM chart are State box,Decision box and exit path.

   e. Write a Verilog model of a full subtractor circuit. [Nov/Dec2010 R-08]

```
Module full sub(D,B,x,y,z);
input x,y,z;
output D,B;
assign D=x ⊕ y ⊕ z
assign B=(y&z)|(~x&y)|(~x&z)
endmodule
```

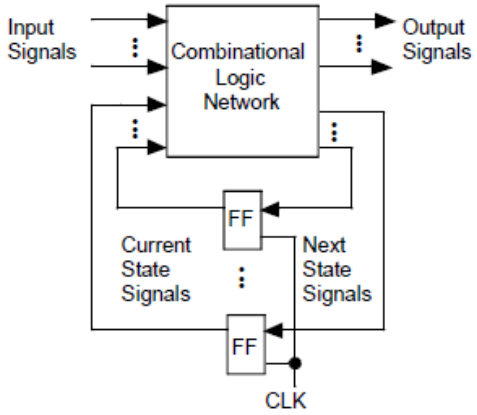
2. MOORE AND MEALY MODEL [April/May2010 R-08],[Nov/Dec2010 R-08], [April/May2010 R-08],[Nov 2007]

a. Differentiate Moore machine from Mealy machine. [May/June 2012 R-8] [April/May2011 R-08 [Nov/Dec2010 R-08]

Mealy model-output is a function of present state and input.

Moore model-Output is a function of present state only.

b. Draw the block diagram for Moore model. [May/June 2012 R-8] [April/May2010 R-08]



c. What is Moore machine? .[Nov 2007]

Output depends only on the present state of the flip flop.

3. HAZARDS [Nov/Dec 2013 R-08] [April/May2010 R-08], [April/May2010], [Nov/Dec 2009 R-08],[Nov 2008] (May 2008), (May 2007)

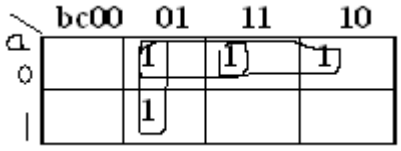
a. Write short notes on Hazards [Nov/Dec 2013 R-08]

The unwanted switching transients(glitches)that may appear at the output of a circuit are called Hazards. Hazards can be avoided by adding redundant terms. Types of hazards (i) static-0 (ii) static-1 (ii) Dynamic Hazard.

b. What is meant by hazard and how it could be avoided? [Nov/Dec 2011 R-10]

The unwanted switching transients(glitches)that may appear at the output of a circuit are called Hazards. Hazards can be avoided by adding redundant terms.

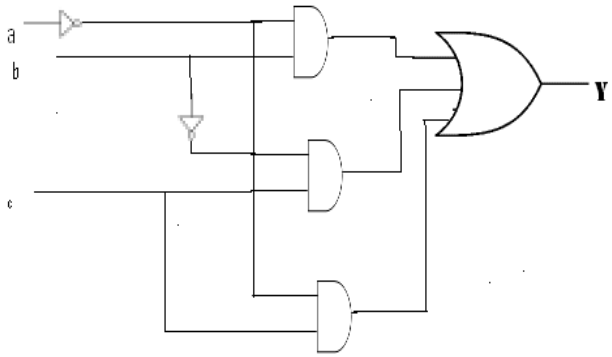
c. What are hazard free digital circuits? [April/May2010 R-08], [April/May2010], [Nov 2008]



K-map with redundant data

Y=b'c+a'b+a'c where a'c is redundant term

Since the expression y contains the redundant term,hazard is avoided. However, we have to add extra gate to get this benefit.



Hazard free logic circuit

d. Explain Dynamic hazard. [April/May2010], [Nov 2008]

Dynamic hazard in which output changes tree or more times when it should change from 1 to 0 or from 0 to 1.

e. What is Hazards?Why do they occur? [May/June 2013 R-08][Nov/Dec 2009 R-08], (May 2008), (May 2007)

The unwanted switching transients(glitches)that may appear at the output of a circuit are called Hazards.The main cause of hazards is the different propagation delays at different paths.

4. RACES AND CYCLES [Nov/Dec2014 R-13][Nov/Dec 2013 R-08] [April/May2010] [Nov/Dec 2009] [Nov 2008, Nov 2007, May 2007,Nov 2006, May 2006]

a. What is critical race condition in asynchrounous sequqential circuits. Give an example. [Nov/Dec2014 R-13]

The race condition is said to exist in an asynchrounous sequential circuit when two or more binary statements chenage the value in response to the change in the input value.

Example

00	**11**
	01
	11
	10

b. What is Synchronous Sequential Circuit? [Nov/Dec 2013 R-08]

In synchronous sequential circuits, change in output signals can affecct memory element upon the activation of clock signals. signals can affect the memory elements only at discrete instant of time. It is easier to design**.**

c. Why do races occur in asynchronous sequential circuit?, What is race? [April/May2010] [Nov 2008, Nov 2007, May 2007,Nov 2006, May 2006]

When two or more binary state variables change their value in response to a change in an input variable race condition occurs in an asynchronous sequential circuit.

d. **Name two techniques used for making a critical race free state assignment. [Nov/Dec 2009]**
   - Shared-row state assignment
   - One-hot state assignment

e. **Define cycle in asynchronous sequential circuits. (Nov 2007)**
   Races can be avoided by directing the circuit through intermediate unstable states with a unique state-variable change. When a circuit goes through a unique sequence of unstable states, it is said to have a cycle.

f. **What are the different types of races that occur in fundamental mode cicuits.(Nov 2007)**
   The different types of races that occur in fundamental mode circuits are non critical race and critical race.

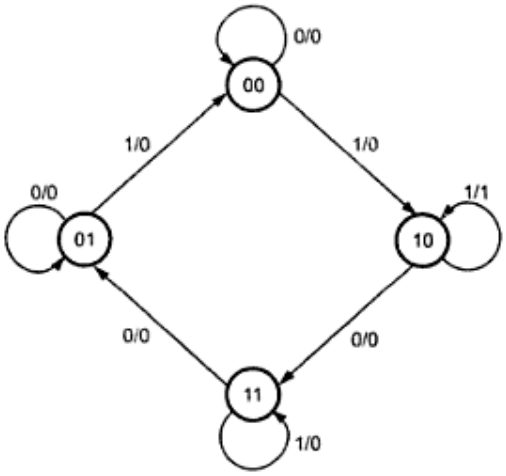
g. **Compare the ASM chart with a conventional flow chart. [May/June 2013 R-08] [Nov/Dec 2009 R-08]**
   ASM chart- A special flow chart that has been developed specifically to define digital hardware algorithms.
   Conventional flowchart-Convenient way to specify the sequence of procedural steps and decision paths for an algorithm.

5. ASYNCHRONOUS SEQUENTIAL CIRCUITS

[May/June 2014 R-2013, May/June 2012 R-8] [**Nov/Dec 2012, R-08] [Nov/Dec 2011 R-11],[Nov/Dec 2011 R-08] ,[April/May 2011 R-08],[Nov/Dec 2009 R-08], (Nov 2006),[May 2006]**

a. What is a state diagram? [May/June 2014 R-2013]

State diagram is a pictorial representation of a behaviour of a sequential circuit. The state is represented by a circle and the transition between states is indicated by directed lines connecting the circles. A directed line connecting a circle with itself indicated that next state is same as present state. The binary number inside each circle identifies the state represented by the circle.



b. what is state table [May/June 2012 R-8]

The state table representation of a sequential circuit consists of three sections labelled present state, next state and output. The present state designates the state of flip-flops before the occurrence of a clock pulse. The next state shows the states of flip-flops after the clock pulse, and the output section lists the value of the output variables during the present state.

c. Difference between Fundamental mode and Pulse mode [Nov/Dec 2012 R-08]

Fundamental mode	Pulse mode
1.Inputs and outputs are represented by levels rather than pulses. 2.It is assumed that the time difference between two successive input changes is larger than duration of internal changes.	1.Inputs and outputs are represented by pulses rather than levels. 2.Minimum pulse width duration is based on propagation delay through the next state logic.

d. Under what circumstances asynchronous circuits are preferred. [Nov/Dec 2011 R-08]

Asynchronous circuits are preferred in systems where synchronization is performed without a global clock.It is also used in systems in which noise must be reduced.

e. What are the two types of Asynchronous sequential circuits? [April/May 2011 R-08],(May 2006)

There are two types of classes, fundamental asynchronous sequential circuits and pulse mode asynchronous sequential circuits

f. Distinguish between synchronous and asynchronous sequential circuits. [Nov/Dec 2009 R-08]

S.No	Synchronous sequential circuits	Asynchronous sequential circuits
1	In synchronous circuits,memory elements are clocked flip-flops	In Asynchronous sequential circuits, memory elements are clocked flip-flops or time delay elements.
2	The change in input signals can affect memory element upon	The change in input signals can affect memory element at any instant of time.

	activation of clock signal.	
3	The maximum operating speed of clock depends on time delays involved.	Because of ansence of clock,asynchronous circuits can operate faster.
4	Easier to design.	More difficult to design.

g. **Define equivalence of two states in asynchronous sequential circuits. (Nov 2006)**
When the input change occurs,present=Next state,called as stable state.

h. **What is an asynchronous sequential circuit? (May 2006)**
Asynchronous sequential circuit memory elements are either unclocked flip-flops or time delay elements. In asynchronous sequential circuit change in input signal can affect memory element at any instant of time. They are difficult to design .

i. **What is excitation table? (May 2008)**
Excitation table contains present and next state from which we can find the input of the flip flop.

j. **What is flow table? .(Nov 2007)**
Flow table in the asynchronous sequential circuit is same as that of state table in the synchronous sequential circuit. In asynchronous sequential circuit state table is known as flow table because of the behavior of asynchronous sequential circuit. The state changes occur independent of a clock based on the logic propagation delay and cause the states to flow from one to another.

UNIT –V
LOGIC FAMILIES &PROGRAMMABLE LOGIC DEVICES

1. **PLD [Nov/Dec2014 R-13] [May/June 2014 R-2013,May/June 2013 R-08] [May/June 2012 R-8] [Nov/Dec2011 R-10],[Nov/Dec2011 R-08] ,[Nov/Dec 2010], [April/May2010], [Nov/Dec2009 R-08],**
(Nov 2008),(Nov 2007)
   a. **What is Field Programmable Gate Arrays (FPGA) [Nov/Dec2014 R-13]**
   FPGA provide the next generation in the programmable logic devices. The word **field** in the name refers to the ability of the gate arrays to be programmed for a specific function by the user instead of by the manufacturer of the device. The word **array** is used to indicate a series of columns and rows of gates that can be programmed by the end user.
   b. **What are the different types of programmable logic devices?**
   [May/June 2013 R-08]
      1. **ROM**
      2. **PAL**
      3. **PLA.**

   c. **Mention the few Applications of PLA and PAL [May/June 2012 R-8]**

PLAs are used to replace ROMs in many applications. They are used for implementing combinational logic functions, and this results in compact circuitry and high switching speed.

c. How the memories are classified? [Nov/Dec 2012, R-08]

a) RAM(static and dynamic)
b) ROM (PLA,PAL,FPGA)

d. What is the need for output buffer in a PLA system? [Nov/Dec2011 R-10]

Output buffer is used to store the information.

e. What is the difference between PLA and PAL. [May/June 2013 R-08] [Nov/Dec2011 R-08] ,[April/May2011 R-08] [Nov/Dec 2010], [April/May2010], [Nov/Dec2009 R-08],

S.No	PLA	PAL
1	Both AND and OR arrays are programmable	OR array is fixed and AND array is programmable.
2	Costliest and complex than PAL and PROMs.	Cheaper and Simpler.
3	AND array can be programmable to get desired minterms.	AND array can be programmed to get desired minterms.
4	Any Boolean functions in SOP form can be implemented using PLA.	Any Boolean functions in SOP form can be implemented using PLA.

f. What are advantages of PLD's? (May/June 2014 R-08 , Nov 2008)

ii. in requirement of space
iii. Reduction in requirement of power
iv. Compactness in design
v. High chip density
vi. Higher switching speed

g. What is a combinational PLD? .(Nov 2007)

PLD is an integrated circuit with internal logic gates that are connected through electronic path that behave similar to fuses.

b. **Draw the TTL inverter (NOT) circuit [May/June 2012 R-08]**

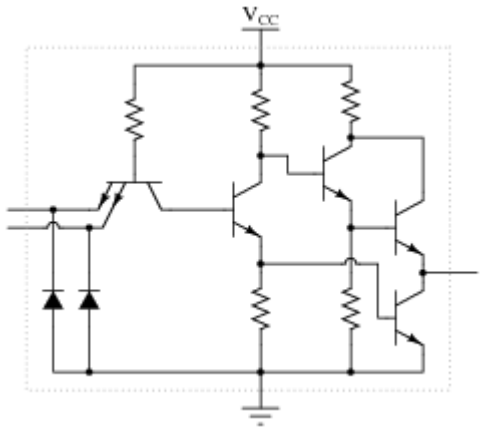
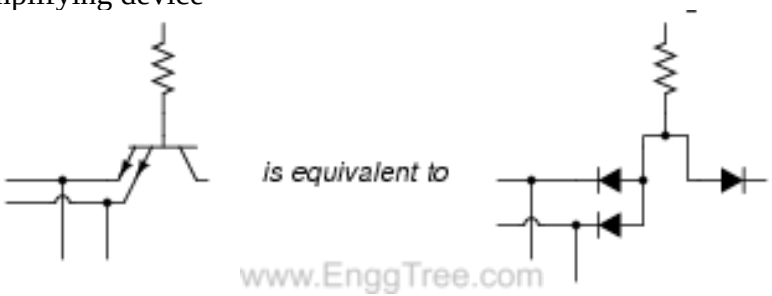


Fig 1. TTL Inverter circuit

The double emitter transistor is being used a pair of diodes, and not as an amplifying device



c. **What are the characteristics of TTL logic? [Nov/Dec2010]**

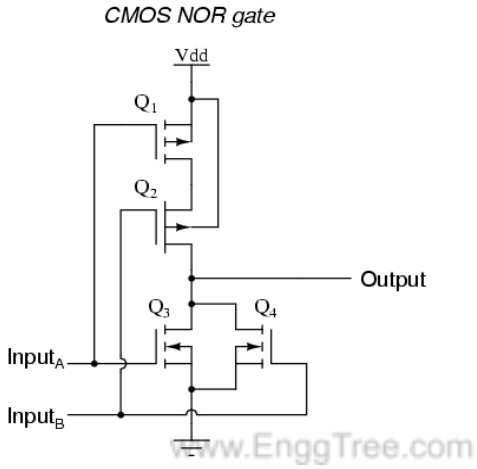
characteristics	Values
Supply voltage	For 74 series-(4.75 to 5.25)units For 54 series-(4.5 to 5.5)units
Temperature range	For 74 series-(0^o to 70^oC) For 54 series-(-55^oC to 125^oC)
Voltage levels	$V_{OL(max)}$ –0.4V $V_{OH(min)}$ –2.4V $V_{IL(max)}$ –0.8V $V_{IH(min)}$ -2.0V
Noise margin	0.4V
Power dissipation	10mW per gate
Propagation delay	Typically 10 ns
Fan-out	10

c. State two advantages of CMOS logic. [April/May2010], [Nov/Dec 2009]

(i)The main advantage of a CMOS gate is its remarkable low static Power dissipation. These circuits take advantage of the fact that NMOS and PMOS Transistors can be fabricated on the same substrate.
(ii)It has lowest packaging density and high speed.
(iii)Improved noise immunity.

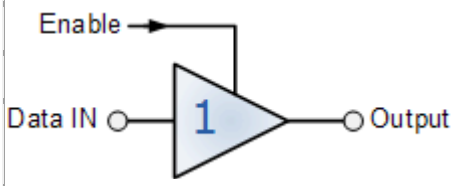
d. **What is the advantage of using schottky TTL gate? (May 2007)**
The advantage of using schottky transistor is it decreases the propagation delay without a sacrifice of power dissipation

h. **Draw two input CMOS NOR gate. (Nov 2007)**



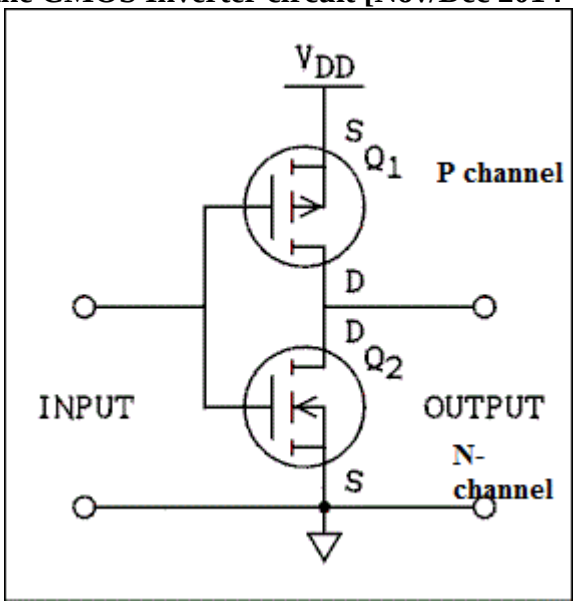
i. **What does LS in 74LS00 indicate? (Nov 2006)**
Low power schhottky TTL

h. Draw a tristate logic.What are its advantages? [Nov/Dec2010](or)
Draw an active-high tri-state buffer and write its truth table.
[April/May2010 R-08]

Symbol	Truth Table		
 **Tri-state Buffer**	Enable	A	Q
	1	0	0
	1	1	1
	0	0	Hi-Z
	0	1	Hi-Z
Read as Output = Input if Enable is equal to "1"			

6. **TTL and CMOS [Nov/Dec 2013 R-08] [May/June 2012 R-08] [Nov/Dec2010],[April/May2010], [Nov/Dec 2009]}, (May 2007),[Nov 2007](Nov 2006)**

d. **Draw the CMOS Inverter circuit [Nov/Dec 2014 R-13]**

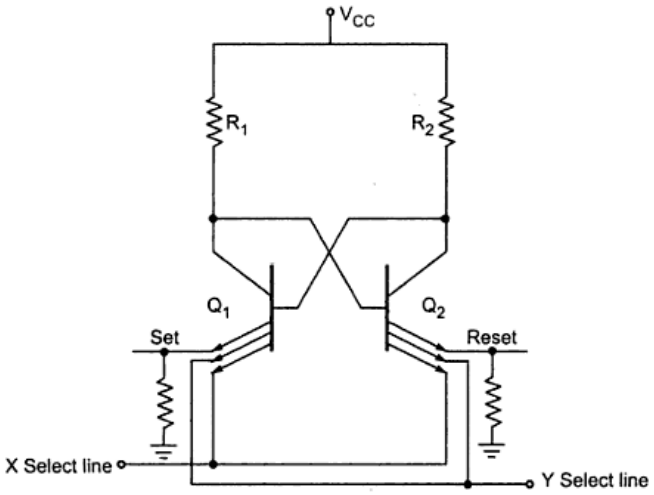


2. **ROM [Nov/Dec2014 R-13][May/June 2014 R-2013, Nov/Dec2013 R-08][May/June 2012 R-8] [Nov/Dec2011 R-10],[April/May 2011 R-08] [Nov/Dec 2009] , (May 2007),(Nov 2006), (May 2006)**

a. **Compare and contrast EEPROM and flash memory [Nov/Dec2014 R-13]**

FLASH MEMORY	EEPROM
Flash is just one type of EEPROM	EEPROM is the type of logic gates
Flash uses NAND type memory	EEPROM uses NOR type
Flash is block-wise erasable	EEPROM is byte-wise erasable
Flash is constantly rewritten	EEPROMs are seldom rewritten
It ranges from Giga Bytes to hundreds of Giga Bytes	It ranges from Kilo Bytes to Mega Bytes

b. **Draw the structure of a static RAM [May/June 2014 R-2013]**



c. **What is Volatile and Non-Volatile memory? [Nov/Dec2013 R-08]**

RAM are called volatile memories because RAM lose stored data when the power is turned off. ROM is a non-volatile memory i.e. it's contents are not lost when it's power supply is switched off. ROM contents are written at the time of it's IC fabrication.

d. **Give the advantages of RAM. [Nov/Dec2013 R-08]**

e. Compare Dynamic RAM and Static Ram **[May/June 2012 R-8]**

Dynamic RAM	Static ROM
1. four transistors are required for a Dynamic RAM **2.** Dynamic RAM memory can be deleted and refreshed while running the program **3.** Data is stored as a charge in a capacitor in Dynamic RAM **4.** Dynamic RAM is used to create larger RAM space system	1. six to eight MOS transistors are necessary for a Static RAM. 2. Static RAM it is not possible to refresh programs **3.** data is stored in flip flop level in Static RAM 4. Static RAM create speed- sensitive cache.

f. **Give the difference between RAM and ROM.[Nov/Dec2011 R-10]**

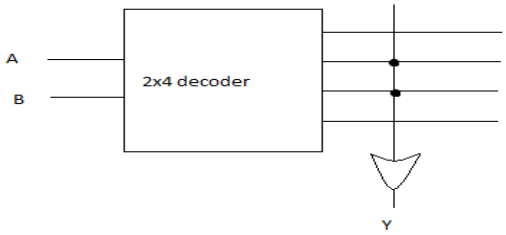
RAM	ROM
5. any memory location can be accessed in a random way **6.** It is volatile memory i.e. it store information as long as power is supplied to it. It's contents are lost when power supply is switched off. **7.** Its contents can be changed. **8.** It is further classified into Static RAM (SRAM) and Dynamic RAM (DRAM)	**1.** ROM is not accessible to user and hence user can't write anything into it **2.** It is a non-volatile memory i.e. it's contents are not lost when it's power supply is switched off. **3.** ROM contents are written at the time of it's IC fabrication. **4.** ROM is further classified into Masked ROM, Programmable ROM, Erasable Programmable ROM and Electrical Erasable Programmable ROM.

g. **Implement the exclusive-or function using ROM.[April/May 2011 R-08]**

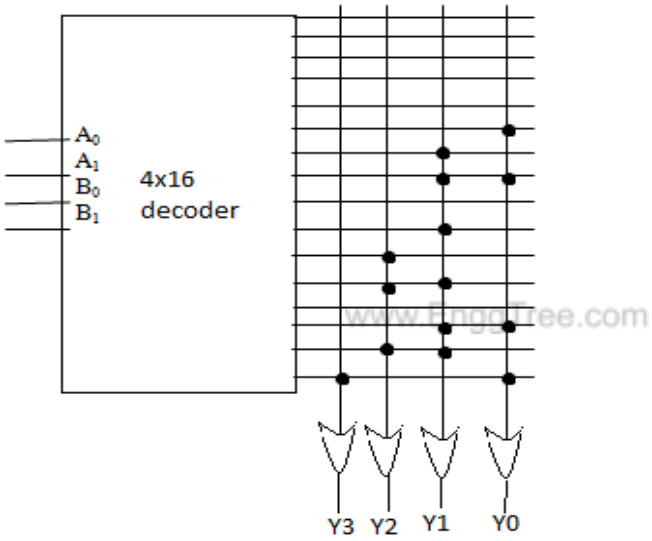
Truth table

A	B	Y
0	**0**	**0**
0	**1**	**1**
1	**0**	**1**

1	**1**	**0**



h. **Implement a 2-bit multiplier using ROM. [Nov/Dec2010 R-08]**



B_1	B_0	A_1	A_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0

1 0 1 1	0 1 1 0
1 1 0 0	0 0 0 0
1 1 0 1	0 0 1 1
1 1 1 0	0 1 1 0
1 1 1 1	1 0 0 1

i. **What is EAROM? [Nov/Dec 2009]**

It is similar to EPROM except that the previously programmed connections can be erased with an electrical signal instead of ultraviolet signal. The advantages in that the device can be erased without removing it from its socket.

j. **Write the advantage of EPROM over a PROM. (May 2007)**

In EPROM the program can be erased by ultra violet rays while in PROM it not possible. PROM uses bipolar or MOS technology but EPROM uses only MOS technology.

k. **Whether ROM is classified as a nonvolatile storage device? why? (May 2007)**

It stores data that are used repeatedly in a system applications such as tables , conversions or programmed instruction for system initialization and operations.ROM retain stored data when power is off and are therefore nonvolatile memories.

l. **Mention the two types of erasable PROM.(Nov 2006)**

Two types of erasable PROM are EPROM(Erasable programmable Read only memory) and EEPROM (Electrical Erasable programmable Read only memory)

m. **How is individual location in a EEPROM programmed or erased? (May 2006)**

Data is stored as charge or no charge on an insulated layer . The insulating layer is made very thin therefore a voltage as low as 20 to 25V can be used to move charges across the thin barrier in either direction for programming or erased. EEPROM allows selective erasing at the register level.

n. **What is access time and cycle time of a memory? [Nov/Dec2010 R-08]**

Access time-Time required to select a word and read.

Cycle time-Time required to complete a write operation

o. **Explain 'write operation' with an example. (Nov 2008)**

Apply the binary address of the desired word to the address lines. Apply the data bits that is to be stored in the memory to the data lines. Activate the write input i.e make R/W' line low.

3. DYNAMIC MEMORY [Nov 2008], (May 2007/Nov 2006),[May 2006]

a. Draw the logic diagram of static RAM and Bipolar RAM cell [**Nov/Dec 2012, R-08]**

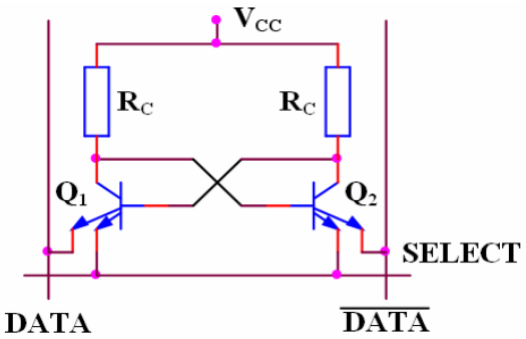


Fig.Bipolar RAM cell

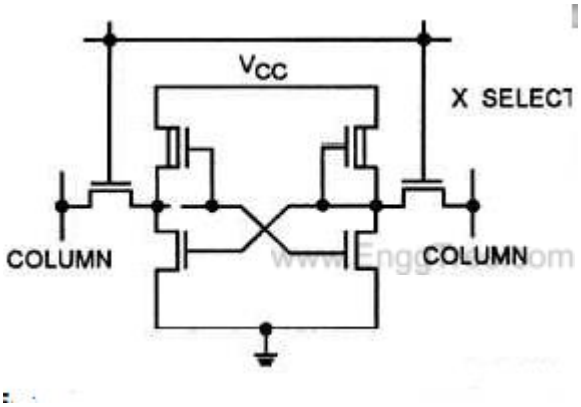
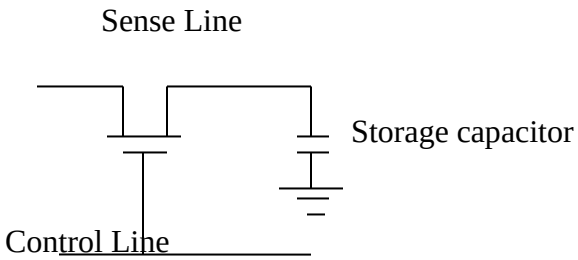


Fig. Static RAM cell

b. **Draw the basic dynamic memory cell.[Nov 2008]**



c. **Explain static memory. Define Dynamic memory. (May 2007/Nov 2006),[May 2006]**

Memories that consists of circuits capable of retaining their state as long as power is applied are known as static memories. Eg RAM Dynamic RAM stores the data as a charge in capacitor.

d. **What is write cycle time ? (May 2008)**

It is the minimum time for which an address must be held stable on the address bus in the write cycle

e. **What is RAM? (Nov 2006)**

We can read from and write into the RAM,so it is called as read/write memory.It is a volatile memory, i.e it cannot hold data when power is turned off.

Part – B

UNIT –I

1. **IMPLEMENTATION USING GATES [Nov/Dec2014 R-13]** [**May/June 2014 R-2013**],**[Nov/Dec 2013 R-08],[[Nov/Dec 2011 R-08],[Nov/Dec2010 R-08] ,[Nov/Dec2010], [April-May 2010 R-08], [Nov/Dec 2009], [Nov 2007] (Nov 2006), (May 2006)**

a. Draw the multiple-level two input NAND circuit for the following expression : F=(AB'+CD')E+BC(A+B). **[Nov/Dec2014 R-13]**

b. Implement the expression Y(A,B,C) = πM(0,2,4,5,6) using only NOR-NOR logic. [**May/June 2014 R-2013**]

c. Implement EXOR gate using only NAND gates. [**May/June 2014 R-2013**]

d. Simplify the following function using Tabulation method Y(A,B,C,D) = ∑m(0,1,2,5,6,7,8,9,10,14) and implement using only NAND gates. [**May/June 2014 R-2013**]

e. Simplify xy + x' z + yz. (6) (6m) **[Nov/Dec2013 R-08]**

f. Draw the multiple level NAND circuit for the following expression.
W(X+YZ)+XY. (6m) **[Nov/Dec2011 R-08]**

g. Draw a NAND logic diagram that implements the complement of the following function.
F (*A*,*B*,*C*,*D*)=∑ (0,1,2,3, 4,8,9,12) (8m) **[Nov/Dec2010 R-08]**

h. Implement the following logic functions using only NAND gates
F=(AB+CD)+C(A+B'D)
T=D(A+B'DC)+A'B+D'). **[Nov/Dec2010]**

i. Multilevel implememtation may be most common procedure in developing digital circuits.Justify your answer implementing the function
F=A(CD+B)+BC. **[Nov/Dec2010]**

j. Implement the following function usin NOR gates.
Output=1 when the inputs are ∑m(0,1,2,3,4) =0 when the inputs are ∑m(5,6,7).(8m) **[April-May 2010 R-08]**

k. Implement the function F=AB+(CD)' using NAND gates only. **[Nov/Dec 2009]**

l. Implement a two input AND gate using NOR gates only. **[Nov/Dec 2009]**

h. Implement the Boolean expression using gates X= (AB+C)'D +E. **[Nov 2007**]

i. Draw the logic symbol of a XNOR gate and give its truth table**.** **[Nov 2007]**

j. Sketch a NAND-NAND logic circuit for the boolean expression.
Y = AB' +AC +BD**.** **[Nov 2007]**

k. Implement the expression
(a) AB+BCD+EFGH
(b) (A+B)(C+D+E)(F+G+H+I) with logic gates. **(Nov 2006)**

l. Realize XOR function using four NAND gates only. **(May 2006)**

K-MAP SIMPLIFICATION [Nov/Dec2014 R-13] [**May/June 2014 R-2013**] **[Nov/Dec2013 R-08] [Nov/Dec2011 R-08] ,[Nov/Dec2010 R-08], [April/May2010],[Nov/Dec 2009 R-08], (Nov 2008), (May 2008) , (Nov 2007),(May 2007), (Nov 2006),(May 2006)**

a. Convert the following function into Product of Max-terms
F(A,B,C) = (A+B')(B+C)(A+C') **[Nov/Dec2014 R-13]**

b. Given Y(A,B,C,D) = πM(0,1,3,5,6,7,10,14,15), draw the K map and obtain the simplified expression. Realise the minimum expressions the basic gates. [**May/June 2014 R-2013**]

c. Simplify the following expression using K-Map method
Y = ∑ (7,9,10,i 1,12,13,14,15). (10)
Write short notes on don't care conditions. (6) **[Nov/Dec2013 R-08]**

d. Simplify the following Boolean function using K Map.
F(A,B,C,D,E) = Σ(0, 1, 4, 5, 16, 17, 21, 25, 29). **[Nov/Dec2011 R-08]**

e. Simplify the Boolean function using K-map
F (*w*, *x* , *y*, *z*) = ∑(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14).(10m) **[April/May2011 R-08]**

f. Simplify the following Boolean function using 4-variable map
F (*w*, *x*, *y*, *z*) = ∑ (2,3,10,11,12,13,14,15)(8m) **[Nov/Dec2010 R-08]**

g. Use K-map to obtain the POS form for
F=A'B'D'+A'CD+A'BC+A'BC'D+ACD+AB'D' **[April/May2010]**

h. Reduce the following function using K-map technique
f(A,B,C,D)=∏(0,3,4,7,8,10,12,14)+d(2,6). (10m) **[Nov/Dec 2009 R-08]**

i. Using K-map method obtain the minimal SOP and POS expressions for the function
F(x,y,z,w)= ∑(1,3,4,5,6,7,912,13).(Nov 2008)

j. Minimize the four variable logic function using K map. **(May 2008)**

k. Simplify the following using Kmap X = A'B +A'B'C +ABC' + AB'C'. **(Nov 2007)**

l. Find the minimum sum of product expression using K-map for the function F=Σm(7,9,10,11,12,13,14,15) and realize the minimized function using only NANDgates. **(May 2007)**

m. Obtain simplified POS using K-map for F(a,b,c,d) = ∑(0,2,3,4,8,10,12,13,14) **(Nov 2006)**

n. Find the minimal sum of product form for the following switching function
F(x1,x2,x3,x4,x5) =∑ m(1,2,3,6,8,9,14,17,24,25,26,27,30,31) +∑ d (4,5) **(May 2006)**

o. Reduce the following function using K map: f = ABC' +A'B'C+ABC+AB'C and realize using NAND gates only. **(May 2006)**

2. TABULATION METHOD [May/June 2013 R-08] [May/June 2012 R-08]

[Nov/Dec 2013 R-8] [Nov/Dec 2012 R-8] [Nov/Dec 2011 R-10],[Nov/Dec 2011 R-08],[April/May2011 R- 08] ,[Nov-Dec 2010 R-08], [April-May 2010 R-08], [April/May2010], [Nov/Dec 2009 R-08], (Nov 2007)[Nov/Dec2014 R-13]

a. Using Quine Mc Cluskey method simplify the given function **[Nov/Dec2014 R-13]**

$$f(A, B, C,D) = \sum m(0,2,3,5,7,9,11,13,14)$$

b. Minimise the given switching function, using Quine-McCluskey method

$$F(x_1, x_2, x_3, x_4) = \sum(0,5,7,8,9,10,11,14,15)$$ **[May/June 2013 R-08]**

c. Explain about NAND and NOR implementations.(10)**[Nov/Dec2013 R-08]**

d. Minimise the function, F using Quine-McCluskey method **[May/June 2012 R-08]**

$$F = \sum(0,1,2,8,10,11,14,15)$$

e. Simplfy the given boolean function using tabulation method **[Nov/Dec 2012 R-8]**

$$f(A, B, C,D) = \sum m(1,2,3,5,7,9,10,11,13,15)$$

f. Simplify the logic function using Quine-McCluskey method and realize using NAND gates.

$$f(A, B, C,D) = \sum m(1,3, 4,5,9, 10,11)+ \sum d(6,8).$$ **[Nov/Dec 2011 R-10]**

g. Simplify the following function using Quine Mc Clusky method.

$$F(A,B,C,D,E,F,G) = \Sigma(20, 28, 52, 60).$$ **[Nov-Dec 2011 R-08]**

h. Simplify the following Boolean function by using aQuine-McCluskey method.

$F(A, B, C, D) = \Sigma m(0, 2, 3, 6, 7, 8, 10, 12, 13)$. (8m) **[April/May2011 R-08]**

i. Using QM method simplify the Boolean expression

$$F(X_1,X_2,X_3,X_4,X_5)=\sum(0,1,4,5,16,17,21,25,29)$$(16m) **[Nov-Dec 2010 R-08]**

j. Minimize the given terms $\pi M(0,1,4,11,13,15)+\pi d(5,7,8)$using Quine-McClusky methods and verify the results using K-map methods.(12m) **[April-May 2010 R-08]**

i. Simplify using tabulation method

$$F(A,B,C,D,E)=\sum(0,2,4,6,9,11,13,15,17,21,25,27,29,31)$$ **[April/May2010]**

j. Simplify the following Boolean function by using Quine-Mcclusky method $F(A,B,C,D)=\sum(0,2,3,4,6,7,8,10,12,13)$ (16m) **[Nov/Dec 2009 R-08]**

k. For the given functions $g(w,x,y,z) = \sum m(0,3,4,5,8,11,12,13,14,15)$. List all the prime implicants and find the minimum product of sum expression. **(Nov 2007)**

l. Write on binary coding. Why to convert from one to another? Discuss Excess 3 code and gray coding.Code your Nation's name,University you belong to, the President of India and the new USA President elected using ASCII. Are all error detection codes correct the errors? Name any error correction code you are familiar with. **[Nov/Dec2010]**

m. State De-Morgan's theorems and Boolean's Postulates.Prove at least four of them.(or) List out the basic rules that are used in Boolean algebra. **[Nov/Dec2010], (May 2008), (Nov 2007) , (May 2007)**

3. POS and SOP FORM [May/June 2013 R-08] [May/June 2012 R-08] ([April/May 2011 R-08] ,[Nov/Dec 2009 R-08], [Nov/Dec 2009], (Nov 2008), (Nov 2007)

a. **Simplify the given Boolean function into**
(I) Sum of products for
(II) Product of sum form and implement if using basic gates
F(A,B,C,D)=∑m(0,1,2,5,8,9,10) [**May/June 2013 R-08]**

b. Differentiate between Min term and Max term.

c. Using K-Map simplify the following exp[ressionsand implement using basic gates
a) F=∑m(1,3,4,6)
b) F=∑m(1,3,7,11,15) + d(0,2,5) [**May/June 2012 R-08]**

d. Express the Boolean function $F = A + B'C$ in a sum of minterms.(6m) **[April/May 2011 R-08]**

e. Express the Boolean function F=XY+X'Z in product of Maxterm.(6m) **[Nov/Dec 2009 R-08]**

f. Obtain the minimum SOP and POS for the function given below
F=∑m(1,3,4,5,6,7,9,12,13) **[Nov/Dec 2009]**

g. Obtain the canonical POS for F(A,B,C)=(A+B')(B+C)(A+C') **(Nov 2008)**

h. (a)Convert (A+B)(A+C)(B+C') into standard POS form.
(b)Convert SOP to equivalent POS.
A'B'C + A'B'C +A'BC +AB'C +ABC. **(Nov 2007)**

i. Show that excess-3 code is a self complementing code. **[Nov/Dec 2009]**
(i)Perform the following decimal addition $(589)_{10}+(199)_{10}$ in BCD.

j. Perform $(51)_{10}-(37)_{10}$ using 1's complement and 2's complement arithmetic. **[Nov/Dec 2009]**

k. Convert $(110A.AB)_{16}$ to decimal,binary and octal**.[Nov/Dec 2009]**

l. (i)Explain weighted BCD+2421 codes. **(Nov 2008).**
(ii) Find the complement of A+BC+AB. **(Nov 2008).**

4. SIMPLIFICATION OF BOOLEAN EXPRESSION
[May/June 2012 R-08](Nov 2008), (Nov 2007), (May 2006)

a. State and Verify Demorgan's Law **[May/June 2012 R-08]**

b. Simplify the Boolean expression **[May/June 2012 R-08]**

F =x'y'z' +x'yz + xy'z' + xyz'

c. Apply Demorgan theorem for the function (A+B+C+D)D. **(Nov 2008).**

d. Prove the following using Demorgan's theorem
AB + CD = {(AB)'.(CD)'}' **(Nov 2007)**

e. Apply Demorgan's theorem to the following expression.
((A+B+C)D)' **(Nov 2007)**

f. Using boolean laws and rules simplify the logic expression
Z = (A'+B)(A+B). (or) Simplify the following Boolean expression (x1+x2)(x1'x3'+x3)(x2'+x1x3)'. **(Nov 2007)**

g. Simplify and draw the logic diagram for the expression shown below.
Y =c'b'a' + c' b a + c b' a **(May 2006)**

h. Prove by perfect indication:
(a) A+AB = A
(b) A(A+B) = A
(C) A+A'B = A+B and
(d) A(A'+B) = AB **(May 2006)**

i. Write the steps for simplifying a logic expression using a Karnaugh map. **(May 2007), (Nov 2006)**

UNIT II

1. Adder and Multiplier

a. Design a 4-bit decimal adder using 4-bit binary adders **[Nov/Dec2014 R-13]**

b. Implement the following Boolean functions using Multiplexers. **[Nov/Dec2014 R-13]**

$$F(A,B,C,D)= \sum m(0,1,3,4,8,9,15)$$

c. Design a 3:8 decoder using basic gates [**May/June 2014 R-2013**]

d. Explain the working of carry-look ahead adder. [**May/June 2014 R-2013**]

e. Draw the circuit of BCD adder and explain. **[Nov/Dec 2011 R-10], (Apr/May 2011 R-08),(Nov 2007**)

f. What is priority encoder? How is it different from encoder? Draw the circuit of 4-bit priority encoder and explain. **[Nov/Dec 2011 R-10]**

g. (i)Design a multiple circuit to multiply the following binary number A0A1A2A3 and B0B1B2B3 using required number of binary parallel adders. (10m)
(ii)Construct a 5 to 32 line decoder with four 3 to 8 line decoder with enable input and a 2 to 4 line decoder. Use block diagrams for the components. (6m**)**
[Nov/Dec 2011 R-08]

h. Design a 4 to 1 line encoder with inputs D1, D2 , D3 , D4 and decreasing order of priority from D3 to D0. **[Nov/Dec 2011 R-08]**

i. Draw the logic diagram of a 2-bit by 2-bit binary multiplier and explain its operation.[**Apr/May 2011 R-08]**

j. Design a combinational circuit that generates the 9's complement of a BCD digit.(8m)**[Nov-Dec 2010 R-08]**

k. Design a carry look ahead adder with necessary diagrams.(or) Explain the operation of carry look ahead adder with neat diagram(8m)
[Nov-Dec-2010 R-08][April-May 2010 R-08] [Nov/Dec 2009 R-08], (Nov 2008)

l. (i)Define Fan-in,Fan-out and Noise Margin.and propagation delay(6m)

[Nov-Dec-2010 R-08], .(May 2006)

(ii)Design an combinational system that produces the product of 2 binary number *A □□□A1, A0) X B □□□B 1,B2 ,B0*)(10m) **[Nov-Dec-2010 R-08]**

2. MAGNITUDE COMPARATOR [Nov/Dec2014 R-13] [Nov-Dec-2013 R-08], [May/June 2013 R-08] [May/June 2012 R-08] [Nov/Dec 2011 R-10],[Nov/Dec2010], (Nov 2008), (May 2007)}, [April/May2010], [Nov/Dec 2009], [May 2008]

a. Draw the block schematic of Magnitude Comparator and explain its operations. **[Nov-Dec-2013 R-08]**

b. Design a 4-bit magnitude comparator and draw the circuit with three outputs: A>B, A=B, A<B **[Nov/Dec2014 R-13] [May/June 2013 R-08]**

c. Design a 4 bit magnitude comparator so that the output follows in Table 1

Table 1

Word	Output
A=B	100
A>B	010
A<B	001

[May/June 2012 R-08]

d. Design a 2-bit magnitude comparator and explain its operation in detail. **[Nov/Dec 2011 R-10],[Nov/Dec 2009]**

e. Discusss the operation of a 4 bit magnitude comparator.What IC is widely used for it. **[Nov/Dec2010], (Nov 2008), (May 2007)**

f. Design a 3 bit magnitude comparator. **[April/May2010]**

g. Design a 5 bit comparator using single 7485 and a gate **.[May 2008]**

CODE CONVERTERS [**May/June 2014 R-2013**] **[Nov/Dec 2013 R-08][Nov/Dec 2012 R-08],[April-May 2010 R-08],{ [April/May2010], (Nov 2007)}, (May 2008)**

a. Design a binary to gray code converter [**May/June 2014 R-2013**]

b. Draw the logic diagram of BCD —. Decimal decoder and explain its operations(16) **[Nov/Dec 2013 R-08]**

c. Design a four bit BCD to excess 3 code converter .Draw the logic diagram. **[Nov/Dec 2012 R-08]**

d. Design and implement the conversion circuits for binary code to gray code.(8m) **[April-May 2010 R-08]**

e. Design a BCD to Excess 3 code converter. **[April/May2010], (Nov 2007)**

f. Design an one digit BCD to binary converter using 74184. **(May 2008)**

g. `Draw and explain the block diagram of a 4-bit serial adder to add the contents of two registers.(10m) **[April-May 2010 R-08]**

h. Multiply $(1011)_2$ by $(1101)_2$ using addition and shifting operation also draw block diagram of the 4-bit by 4 bit parallel multiplier.(8m) **[April-May R-08]**

i. Design a BCD to seven segment decoder circuit.Assume don't cares. **[April/May2010]**
Implement full subtractor using demultiplexer. (10m) **[Nov/Dec 2009 R-08]**

3. IMPLEMENTATION USING MULTIPLEXER [May/June 2014 R-2013] [Apr/May 2011 R-08],[Nov/Dec 2009 R-08], [Nov/Dec 2009],[Nov 2008]

a. Design a full subractor using demultiplexer. [**May/June 2014 R-2013**]
b. Implement the following function using suitable multiplexer
F(A, B, C, D)= Σ1(, 3, 4, 11, 12, 13, 14, 15) **[Apr/May 2011 R-08]**
c. Implement the given Boolean function using 8:1 multiplexer F(A,B,C)=∑(1,3,5,6). **[Nov/Dec 2009 R-08**]
d. Implement the function F(A,B,C,D)= ∑m(0,1,3,5,8,9,15) using a 8:1 Multiplexer. **[Nov/Dec 2009]**
e. Implement the function with a multiplexer F(A,B,C,D)= ∑(0,1,3,4,8,9,15 **(Nov 2008)**

4. ADDER AND SUBTRACTOR: [May/June 2013 R-08] [**Nov/Dec 2012 R-08], [May/June 2012 R-08],[[Apr/May 2011 R-08], [Nov/Dec 2009] ,(Nov 2007)**

a. Construct a 4-bit even parity generator circuit using gates**[Nov/Dec2014 R-13]**
b. Design a 4 bit parallel subractor adder/subractor and draw the logic diagram (8) **[Nov/Dec 2012 R-08]**,
c. Draw the logic diagram of BCD adder and explain its operation (8) **[Nov/Dec 2012 R-08], [May/June 2013 R-08]**

d. Design a combinational circuit of 2-digit BCD adder (16) **[May/June 2012 R-08]**
e. Design a serial binary adder. **[Apr/May 2011 R-08]**
f. Design a full Adder using two half adders and an OR gate. **[Apr/May 2011 R-08]**
g. Implement Full adder using two half adders. **(Nov 2007)**
h. Write down the truth table of a half subtractor and draw its logic circuit. **[Nov/Dec 2009]**
i. Explain even parity checker**.(Nov 2008)**
j. Design a 4:1 multiplexer using transmission gate and explain its operation.**(Nov 2007)**
J. Design a 4 bit ripple carry adder. **(Nov 2007)**
k. Draw the diagram and explain 1 to 16 Demultiplexer circuit. **(May 2007)**
l. Construct a 5X32 decoder with four 3X5 decoders and a 2X4 decoder. Use block diagrams. **(Nov 2006)**

UNIT-III

1. **State Table Redution**

a. Reduce the number of states in the following state table and tabulate the reduced state stable.(6m)

Present state	Next state		Output	
	x = 0	x = 1	x =0	x =1
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

b. Design a sequential circuit with two D Flipflops A and B and an input x. When x = 0 the state of the circuit remains the same. When x =1 the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00 and repeats.(10 m)

[Nov/Dec 2011 R-08]

2. COUNTERS . [Nov/Dec2014 R-13] [**May/June 2014 R-2013**] **[Nov/Dec 2013 R-08] [May/June 2013 R-08], [May/June 2012 R-08],[Nov/Dec 2012 R-08] [Nov/Dec 2011 R-10] ,[Nov/Dec 2011 R-08],[April-May 2011 R-08] [Nov-Dec 2010 R-08], [Nov/Dec2010], [April-May 2010 R-08], [April/May2010], [Nov-Dec 2009 R-08], [Nov/Dec 2009], (May 2008), (Nov 2007),(May 2007), (Nov 2006) ,(May 2006)**

a. Design 3 bit binary synchronous counter with JK Flipflops **[Nov/Dec2014 R-13]**

b. Draw the block schematic of up-down counter and explain its operation.(16)

[Nov/Dec 2013 R-08]

c. Design a counter to count the sequence 0,1,2,4,5,6 using SRFFs

[May/June 2013 R-08]

d. Design a 4 bit Asynchrounous ripple counter and explain its operation with timing diagrams **[May/June 2013 R-08]**

e. Design a Moore Type sequence detector to detect a serial input sequence of 101 **[May/June 2014 R-13]**

f. Explain the design steps of Mod n counter (8)[**May/June 2012 R-08]**

g. Design a 3 bit Johnson counter and explain its operation (8) **[Nov/Dec 2012 R-08]**

h. Draw the logic diagram of 4-bit binary UP/DOWN synchronous counter and explain with its truth table. Also draw the timing diagram. **[Nov/Dec 2011 R-10]**

i. Design Johnson counter and state its advantages and disadvantages.

[Nov-Dec 2011 R-08]

j. Design 3 bit binary synchronous counter with T Flipflops**. [Nov-Dec 2011 R-08]**

k. Explain the operation of a BCD ripple counter with JK flip flops.

[April-May 2011 R-08]

l. With a neat state diagram and logic diagram,design and explain the sequence of states of BCD counter(16m) **[Nov-Dec 2010 R-08]**

m. What are the applications of counters?Design a counter to count the following sequence 0-1-2-3-4-0. **[Nov/Dec2010]**

n. Design a synchronous up/down counter that will count up from zero to one to two to three, and will repeat whenever an external input x is logic 0,and will count down from three to two to one to zero ans will repeat whenever the external input x is logic (viii).Implement your circuit with one TTL SN74LS76 device and one TTL SN74LS)) device.(12m)[**April-May 2010 R-08]**

o. Design a counter with count sequence 0,2,4,6,1,3,5,7,0,2,4,6,1,3,….. using JK flipflops **[April/May2010]**

p. Design a 3 bit binary counter and write the truth table and O/P waveform.(or) Design a 3 bit binary counter using T flip flop that has a repeated sequence of six states.000-001-010-100-101-110.Give the state table, state diagram and logic diagram. **[Nov-Dec 2009 R-08](May 2008), (Nov 2007)**

q. Explain in detail the operation of a 4 bit binary ripple counter.(16m) **[Nov/Dec 2009 R-08]**

r. Design a MOD-5 synchronous counter using JK flipflop. **[Nov/Dec 2009]**

s. Design a synchronous counter which counts in sequence 0,2,6,1,7,5,0….. using D FFs.Draw the logic diagram and state diagram**.(May 2007)**

t. Design a counter with binary sequence 0,2,4,6,7 and repeate.Use TFFs and don't cares for unspecified states. **(Nov 2006)**

u. Draw a 3 bit reversible counter and explain its operation. **(May 2006)**

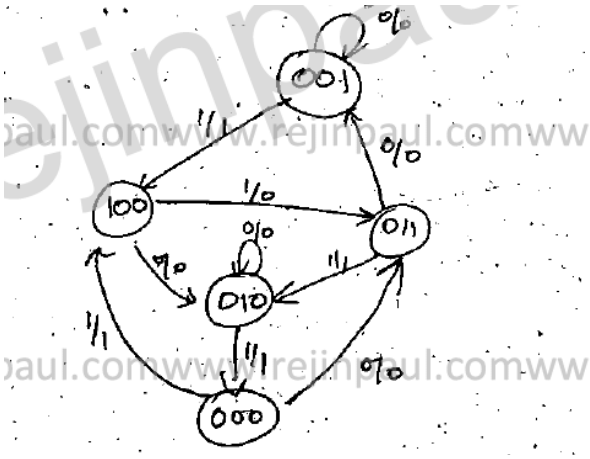
v. Draw an asynchronous decade counter and explain its operation drawing neat waveforms**.(May 2006)**

w. Design and explain the working of a mod-9 counter. **(May 2006**)

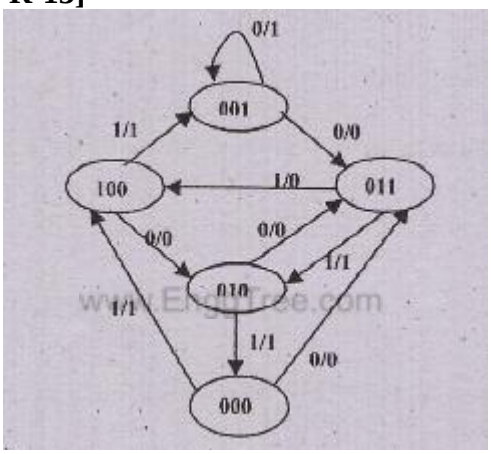
3. FLIP FLOP . [Nov/Dec2014 R-13] [**May/June 2014 R-2013**]**[Nov/Dec 2013R-08][Nov/Dec 2012 R-08] [May/June 2012 R-08],[Nov/Dec 2011 R-10] ,[Apr/May 2011 R-08],[Nov-Dec 2010 R-08],{ [Nov/Dec2010], [April/May2010], [Nov/Dec 2009 R-08], [April-May 2010 R-08]**

a. Explain the differences between a state table, a characteristic table `and an excitation table. **. [Nov/Dec2014 R-13]**

b. Design a sequential circuit that has 3 flip-flops A,B,C, one input x and one output y. The circuit is to be designed by treating the unused states as don't care conditions. Use JK flip-flops in the design. State diagram of the circuit is as given below. [**May/June 2014 R-2013**]



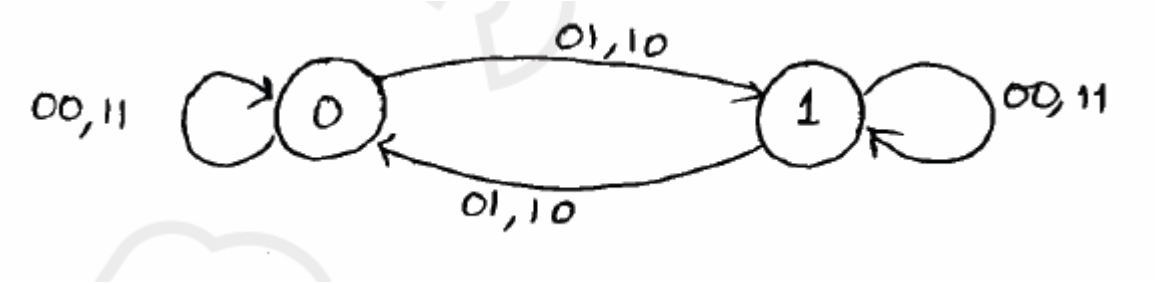
c. Design the sequential circuit specified by the following state diagram using T flip-flops. Check whether your design is self correctable. **. [Nov/Dec2014 R-13]**



Draw the block diagram of SR—FF and explain. (6) **[Nov/Dec 2013R-08]**

d. Explain about triggering of flip-flops. (10) **[Nov/Dec 2013R-08]**
e. Design and draw the output waveform of UP/DOWN Counter using JKFF **[May/June 2012 R-08]**
f. Design a sequence detector which detects the sequence '01110' using D flip flops (one bit overlapping) **[Nov/Dec 2012 R-08]**
g. A sequential circuit has three D flip flops. A, B and C and one input x. It is desired by the following flip flop input functions
D_A= (BC'+B'C)x +(BC+ B'C')x'
D_B=A, D_C=B
h. Derive the state table for the circuit and draw two state diagrams for x = 0, and other for x = **[Nov/Dec 2011 R-10]**

f. Draw the logic diagram of master-slave SR flip flop and explain its working with truth table. (10m)[**Nov/Dec 2011 R-10]**
g. Design a D flip flop using J-K flip flop and explain with its truth table.(6m) **[Nov/Dec 2011 R-10]**
h. Design the following synchronous sequential circuit using D flip flop and logic gates**.[Apr/May 2011 R-08].**

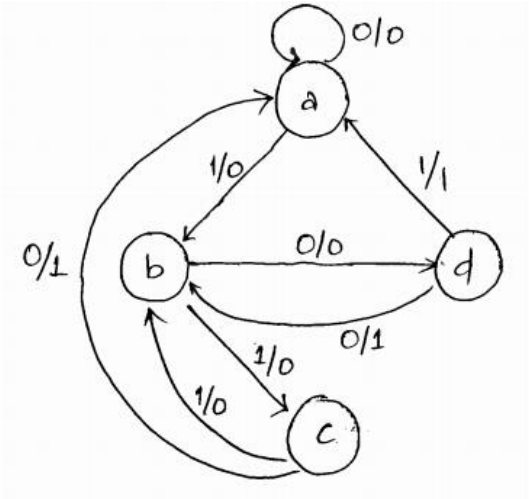


i. Convert D flip flop to T flip flop**.[Apr/May 2011 R-08]**
j. Provide the characteristic table, characteristic equation and excitation table of D-flip-flop and JK flip-flop (6m)[**Nov-Dec 2010 R-08]**
k. What is meant by triggering ?What are the various types of triggering? How to implement a Basic RSFF? What are its limitations? How to solve it? What is meant by master clock and clock pulse? Draw the master slave JK FF. Explain its operation and its advantages?(or) Explain the working of a master slave JK flip flop. State its advantage.
[Nov/Dec2010], [April/May2010], [Nov/Dec 2009 R-08]
l. Write down the characteristic table for the JK flip flop with NOR gates.(4m) **[April-May 2010 R-08]**
m. Construct a clocked JK flip flop which is triggered at the positive edge of the clock pulse from a clocked SR flip flop consisting of NOR gates. (4m)
[April-May 2010 R-08]

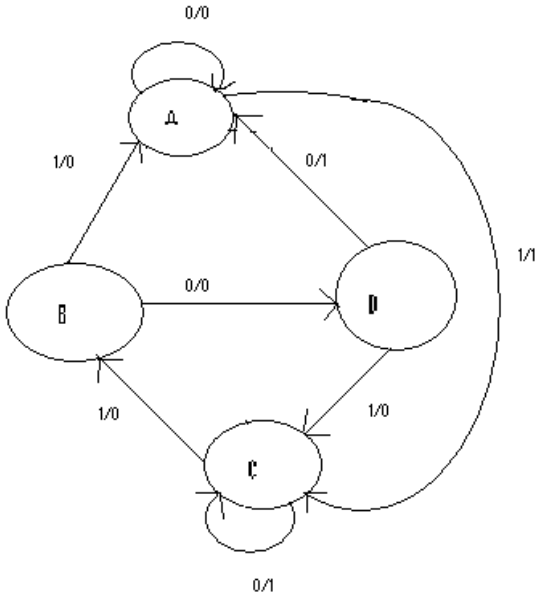
4. SHIFT REGISTER {[Nov/Dec 2012 R-08] [May/June 2012 R-08],[Nov-dec 2010 R-08],(Nov 2008)}, [April-May 2010 R-08], [April/May2010], (May 2008), [May 2007], (Nov 2006), (May 2006)

a. Design a 4 bit bi-directional shift register (8) **[Nov/Dec 2012 R-08]**
b. Explain the operation of shift and ring counters(8)[**May/June 2012 R-08]**
c. Explain the operation of universal shift register with neat block diagram.(10m) **[Nov-dec 2010 R-08], (Nov 2008)**
d. What is meant by universal Shift register?Explain the principle of operation of 4-bit Universal shift register.(12m)[**April-May 2010 R-08]**
e. Design a 4 bit shift register [**April/May2010]**
f. Design a 5 bit shift register using 5 master – slave S-R FF. **(May 2008)**
g. Draw the logic diagram for a 5-bit serial load shift right register using D flip flop and explain.**[May 2007]**
h. Draw the logic diagram of a 4 bit parallel load recirculating shift register and explain. **(May 2007)**
i. Draw the eight bit serial in-parallel out shift register and explain its operation. **(Nov 2006)**
j. Draw the four bit parallel in- serial out shift register and explain its operation
(May 2006)
k. Draw a four bit serial in serial out shift register and explain **(May 2006)**

l. Design a clocked sequential machine using T flip-flops for the following state diagram. (use straight binary assignment). **[April-May 2011 R-08]**



m. Design a BCD up/down counter using S-R flip flops. **[April/May 2010]**
n. Design a negative-edge triggered 'T flipflop'(16m) **[Nov/Dec 2009-R-08]**
o. (i)How will you convert a D flipflop into JK flipflop?(8m)
[Nov/Dec 2009 R-08], (Nov 2008)
p. Draw the circuit for a D Latch using NAND gates only **[Nov/Dec 2009]**
q. Convert a T-flipflop to a D flip flop. **[Nov/Dec 2009]**
r. A state diagram of a sequential circuit is given below. The circuit has one input and one output. Design sequential circuit using T flipflps.
[Nov/Dec 2009]



s. Design a sequential circuit with JK flip flop to satisfy the following state equations**.(Nov 2008)**
A(t+1)=A'B'CD+A'B'C+ACD+AC'D'
B(t+1)=A'C+CD'+A'BC'
C(t+1)=B
D(t+1)=D'

t. Design the sequential circuit whose state table is given as**(Nov 2007)**

Present State		Input	Next State		Output
A1	A2	X	A1	A2	Y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	0	0	1
1	0	0	1	0	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1

u. Draw the four bit Johnson counter and explain the operation.
(Nov 2006/May 2007)

v. Draw the clocked RS flip flop and explain with truth table**.(May 2007)**

w. Reduce the state table using implication chart method.(**Nov 2006)**

Present state	a	b	c	d	e	f	g
Next State X = 0	a	c	a	e	a	g	a
Next state X = 1	b	d	d	f	f	f	f
Output	0	0	0	1	1	1	1

UNIT-IV

1. Classification of Memories

a. Discuss in detail about the classifications of memories. (16) **[Nov-Dec 2013 R-08],**

b. i. Describe the two dimensional address decoding scheme of typical DRAM in detail. (8)
ii.Given the 32 × 8 ROM chip with enable input, show the external connection necessary to construct a 128 × 8 ROM with four chips and a decoder.(8m) **[Nov/Dec 2011 R-08]**

c. Design a combinational circuit using a ROM. The circuit accepts a 3-bit number and generates an output binary number equal to the square of the input number.(10m)

d. Briefly explain the EPROM and EEPROM technology. **[Apr/May 2011 R-08]**

e. With logic diagram, explain the basic macrocell. **[Apr/May 2011 R-08]**

f. What are the advantages of FPGA? **[Nov/Dec 2011 R-10]**

2. RAM [Nov/Dec 2014 R-13] [May/June 2014 R-13] [May/June 2012 R-08] [May/June 2013 R-08], [[May/June 2012 R-08], [Nov/Dec 2011 R-10], [Nov-Dec 2010 R-08], [April/May2010], [Nov-Dec 2010 R-08] (Nov 2007), [May2006]

a. Using eight 64x8 ROM chips with an enable input and a decoder, construct a 512x8 ROM **[Nov/Dec 2014 R-13]**

b. Write short notes on EAPROM and static RAM cell using MOSFET **[Nov/Dec 2014 R-13]**

c. Explain the read cycle and write cycle timing parameters of a RAM with the help of timing diagram **[May/June 2014 R-13]**

d. Draw the Dynamic RAM cell and explain its operation **[May/June 2014 R-13]**

e. Design and explain a 32 x 8 ROM **[May/June 2013 R-08]**

f. Write short notes on
(a) Memory decoding (8) (b) Memory expansion (8)
[Nov/Dec 2012 R-08] [May/June 2012 R-08]

c. Discuss the classification of ROM and ROM memories (8) **[May/June 2012 R-08]**

d. Explain the operation of static and dynamic MOS RAM cell with necessary diagrams. [Nov/Dec 2011 R-10]

e. Explain the Read and Write cycles of RAM (or) Explain read and write operation of memory with timing waveforms.(8m)
[Nov-Dec 2010 R-08], [April/May2010]

f. Write short notes on :
a.MemoryDecoding. **[May 2006]**
b.RAM. .(8m) [**Nov-Dec 2010 R-08] (Nov 2007), [May 2006]**

3. <u>IMPLEMENTATION USING PLA, PAL</u>[May/June 2014 R-13] [Nov/Dec 2013 R-08] [May/June 2013 R-08] [Nov/Dec 2012 R-08] [Nov/Dec 2011 R-10] ,[[Nov/Dec 2011 R-08] [Apr/May 2011 R-08], [Nov-Dec 2010 R-08], [April/May 2010 R-08], [Nov/Dec 2009 R-08], [Nov 2008] , (Nov 2007)

a. Use PLA with 3 inputs,4 AND terms and two outputs to implement the following two Boolean functions
$F_1(A,B,C)= \sum m(3,5,6,7)$ $F_2(A,B,C)= \sum m(1,2,3,4)$ **[Nov/Dec 2014 R-13]**

b. Compare and contrast PLA and PAL. **[Nov/Dec 2014 R-13]**

c. Design a BCD to Excess # Code convertor using a PLA **[May/June 2014 R-13]**

d. Discuss in detail about the FPGA with suitable diagrams. (16) **[Nov/Dec 2013 R-08]**

e. Design using PAL the following Boolean functions
$W(A,B,C,D) = \Sigma (2,12, 13)$
$X(A,B,C,D) = \Sigma (7,8,9,10,11,12,13,14,15)$
$Y(A,B,C,D) = \Sigma (0,2,3,4,5,6,7,8,10,11,15)$
$Z(A,B,C,D) = \Sigma (1,2,8,12, 13)$ **[May/June 2013 R-08]**

c. Write short notes on
(a) FPGA and its application
(b)Programmable logic array **[May/June 2012 R-08]**

d. Implement a 3bit up/down counter using PAL devices **[Nov/Dec 2012 R-08]**

e. Implement Binary to gray code converter using PROM devices **[Nov/Dec 2012 R-08]**

f. Draw the basic block diagram of PLA device and explain each block. List out its application. Implement a combinational circuit using PLA by taking a suitable boolean function. **[Nov/Dec 2011 R-10]**

g. Obtain the PLA programming table for the combinational circuit with following function.
$A (x, y, z) = \Sigma (1, 2, 4, 6)$
$B (x, y, z) = \Sigma (0, 1, 6, 7)$
$C (x, y, z) = \Sigma (2, 6)$
$D (x, y, z) = \Sigma (1, 2, 3, 5, 7)$ **[Nov/Dec 2011 R-08]**

h. Implement the following functions using 3 input, 4 product term and 2 output PLA
F = AB' + AC + A'BC'
F = (AC + BC)' **[Apr/May 2011 R-08]**

i. Draw a PLA circuit to implement the functions
$F_1 = A'B + AC' + A'BC'$; $F_2 = (AC + AB + BC)'$.(8m**)**
[Nov-Dec 2010 R-08]

j. A combinationa circuit is defined as the functions F1=AB'C'+AB'C+ABC; f2=A'BC+AB'C+ABC.Implement the digital circuit with a PLA having 3 inputs,3 product terms and 2 outputs(8m)[**April/May 2010 R-08]**

k. Implement the following Boolean functions with a PLA
$F_1(A,B,C)=\sum(0,1,2,4)$
$F_2(A,B,C)=\sum(0,5,6,7)$
$F_3(A,B,C)=\sum(0,3,5,7)$ **[Nov/Dec 2009 R-08]**

l. A combinational circuit is defined by the functions.
$F_1(A,B,C)= \sum(3,5,6,7)$
$F_2(A,B,C)= \sum(0,2,4,7)$.
Implement the circuit with a PLA having three inputs, four product terms and two outputs. **[Nov 2008]**

m. Implement the following two Boolean function with a PLA.
F1(A,B,C) = ∑ (0,1,2,4)
F2(A,B,C) = ∑ (0,5,6,7) **(Nov 2007)**

n. F1=AB'+AC+A'BC ; F2=(AC+BC)'. Using PLA implement it. Discuss about FPGA,EEPOM and PAL.
(or) Write notes on FPGA and PLA.[Nov/Dec2010 R-08], [April/May2010 R-08], **[Nov/Dec 2009], (Nov 2008), (May 2008)**

o. Why is chip select signal pin available in RAM and when can one read or write using RAM IC? Explain dynamic RAM cell. How is it different from static cell? Discuss memory cycle and timing diagram. How is ROM organized for storing permanent data? (or) Sketch the 1 bit static RAM cell and dynamic cell and explain their operation.(or) Draw a circuit for MOS based static RAM cell and explain its operation.(or)
Draw a dynamic RAM cell and explain its operation. Compare its simplicity with that of NMOS static RAM cell, by way of diagram and operation. **[Nov/Dec2010], [April/May2010],[Nov/Dec 2009],(May 2006)**

p. (i)We can expand the word size of a RAM by combining two or more RAM chips. For instance, we can use 32x8 memory chips where the number 32 represents the number of words and 8 represents the number of bits per word, to obtain a 32x16 RAM. In this case the number of words remains the same but the length of each word will two bytes long.Draw a block diagram to show how we can use two 16x4 memory chips to obtain a 16x8 RAM.(8m)
[April/May 2010-R-08]
(ii) Explain the principle of operation of Bipolar SRAM cell.(8m)
[April/May 2010-R-08]

q. Explain the following in detail
(1)PROM)

(2)EPROM(Nov 2006)
(3)EEPROM(Nov 2006)
(4)EAPROM

(or) Explain in detail the various classification of memories.(or) Categories RAM and ROM and explain in detail.

[April/May2010], [Nov/Dec 2009], [Nov 2008] , [Nov 2007], (May 2007)

r. Design a combinational circuit using ROM. The circuit accepts a three bit number and outputs a binary number equal to the square of the input number.(16m) **[Nov/Dec 2009 R-08]**

s. Design a 16 bit ROM array and explain the operation. **(May 2008)**

t. Design the given function using PAL and PROM
F1 = ∑m(0,1,4,5,7,9,11,13)
F2 = ∑m(1,3,5,6,9,11,14,15**)** **(Nov 2007)**

u. Explain the basic structure of 256X 4 static RAM with neat sketch.
(May 2007), (Nov 2006)

v. Explain the following terms:
(i)Dynamic memory
(ii)Volatile storage
(iii)Field programmable memory.
(iv)Mask programmable memory. **(Nov 2006)**

w. Elaborate the single fused PROM cell with clear sketch. **Nov 2006)**

x. (i)Illustrate the concept of 16 X 8 bit ROM arrange with diagram.
(ii) Describe the typical ROM internal organization with necessary diagram.
(Nov 2006)

y. (i) How can one make 64X8 ROM using four 32X4 ROMs? Draw such a circuit and explain.
(ii) Implement binary to excess 3 code converter using ROM**.(May 2006)**

UNIT-V

1. **TTL and CMOS [Nov/Dec2014 R-13] [Nov/Dec 2012 R-8] [Nov/Dec 2011 R-08],[Nov/Dec 2011 R-08],[April-May 2011 R-08], [Nov/Dec2010],[April-May2010 R-08].[April/May2010], [Nov/Dec 2009],(May 2008) ,(Nov 2007), (May 2007), {(May 2007), (Nov 2006/May 2006)**

a. Draw and explain Tri-state TTL inverter circuit diagram and explain its operation. **[Nov/Dec2014 R-13]**

b. Draw the circuit diagram of two input TTL NAND gate with tri state output and explain its action clearly showing Logic and voltage levels [**Nov/Dec 2012 R-8**]

c. Draw a TTL circuit with totem pole output and explain its working. **[Nov/Dec 2011 R-10]**

a. With neat diagram, explain the operation of CMOS NAND and NOR gates . **[Nov/Dec 2011 R-10]**

b. Explain the operation of open collector output TTL NAND gate in detail. **[Nov/Dec2010 R-08]**

e. Draw the schematic and explain the operation of a CMOS inverter. Also explain its characteristics.(8m) **[April-May 2011 R-08]**

f. Name the five important characteristics based on which the different logic families are compared. Give the ranges for the above in the case of TTL and CMOS families. **[Nov/Dec2010]**

g. Discuss the general characteristic of TTL and CMOS logic families.(8m) **[April-May 2010 R-08]**

a. Draw the circuit of 2 input CMOS NAND gate and explain its operation (or) Explain the operation of CMOS NAND and NOR gate with the circuit and truth table. **[April/May2010], [Nov/Dec 2009](May 2008)**

b. Draw a 2 input NAND gate using schottky TTL logic and explain its operation. **(Nov 2007)**

j. What are the different types of TTL gates available? Explain their operation taking suitable example. **(May 2007)**

k. Draw the circuit diagram of 2 input CMOS NAND gate using CMOS logic and explain their operation.**(May 2007)**

l. Analyse the performance characteristics of TTL and CMOS logic. **(May 2007), (Nov 2006/May 2006)**

m. Explain the operation of tristate inverter.[April/May2010]

1. RACES [Nov-Dec 2010 R-08], [April/May2010], (May 2007),(Nov 2006)

a. (i)Differentiate critical races from non critical races.(6m)[Nov-Dec 2010 R-08]

(ii)Explain the problem of non critical and critical races in asynchronous sequential circuits with suitable examples.(or) Define the following terms:

(a) Critical race

(b) Non critical race

(c)Hazard

(d)Flow table **[April/May2010], (May 2007),(Nov 2006)**

b.Discuss a method used for race free assignment with example **(May 2007), (Nov 2006)**

c.Explain the involved in the reduction of state table.(10m)[**Nov-Dec 2010 R-08]**

2. **HAZARDS . [Nov/Dec 2014 R-13] [Nov/Dec 2014 R-13] [May/June 2014 R-13] ,[Nov/Dec 2013 R-08] [May/June 2013 R-08], [May/June 2012 R-08], [Nov/Dec 2012 R-08], [Nov/Dec 2011 R-10],[Nov/Dec 2011 R-08],[April/May 2011 R-08],[April-May 2010 R-08],[Nov/Dec2010],[Apr'10],[Nov/Dec 2009],[Nov 2008],[Nov 2007][May 2007],[Nov 2006], [Nov/Dec2010], [Nov/Dec2009]**

a. What is a hazard in an asynchronous sequential circuits? Define static hazard, dynamic hazard and essential hazard. **[Nov/Dec 2014 R-13]**

b. Design a asynchronous sequential circuit that has 2 input's x_1 and x_2 and one output z. When x_1 = 0, output is 0. The change-in x_2 that occurs while x_1 is 1 will cause output **z-=** 1 . The output z will remain 1 until x_1 returns to 0 **[May/June 2014 R-13]**

c. List out various problems arises in asynchronous circuits. Explain any two problems in detail. (16) **[Nov/Dec 2013 R-08]**

d. Design a azard free asynchronous circuit that changes state whenever the inout goes from logic 1 to logic 0 **[May/June 2013 R-08]**

e. Write short notes on
(a) Incompletely specified state machines
(b) Hazard free switching circuits **[May/June 2012 R-08]**

f. Write short notes on races and hazards that occurs in asynchronous circuits . Discuss a method used for race free assignment with example
 [Nov/Dec 2012 R-08]

d. (a)Explain the method to eliminate static hazard in an asynchronous circuit with an example. (10)
b) Write short notes on VERILOG.(6) **[Nov/Dec 2011 R-10]**

e. \Explain the following with an example circuit

(a) Race condition in asynchronous sequential circuits (6)

(b) Hazards in asynchronous sequential circuits. (6)

(c) Guidelines for Hazard free circuit Design. (4) **[Nov/Dec 2011 R-08]**

f. What is an Hazard? What are the types of hazards? Check whether the following circuit contains an hazard or not

$$Y = x_1 x_2 + x_2' x_3$$

If the hazard is present, demonstrate its removal**.[Apr/May 2011 R-08]**

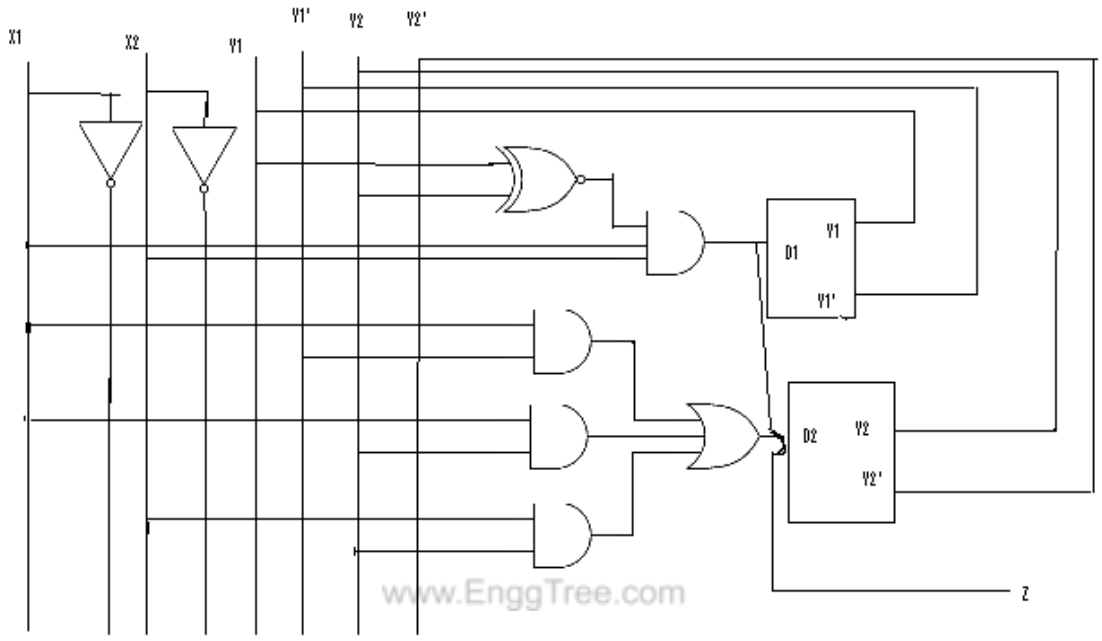
g. What are called as essential hazards? How does the hazard occur in sequential circuits? How can the same be eliminated using SR latches .Dive an example(16m**)[April-May 2010 R-08]**

h. What is Hazard? What are its types? How to minimize and eliminate the hazards based on their types? (or)Explain the term 'Hazard' with reference to combinational circuit with appropriate example. (or) Explain in detail static, dynamic and essential hazards in a digital circuit **[Nov/Dec2010] [Apr'10], [Nov/Dec 2009] ,[Nov 2008],[Nov 2007][May 2007],[Nov 2006]**

i. Describe the fundamental mode asynchronous sequential circuits and its design problem**. [Nov/Dec2010]**

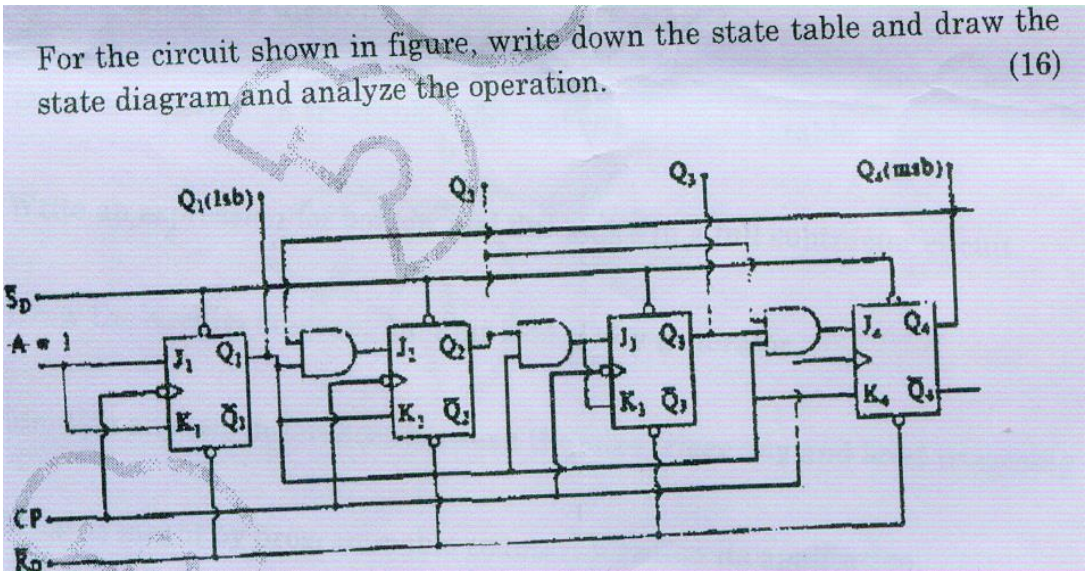
j. Give the hazard free realization for the Boolean equation
F(A,B,C,D)= ∑m(1,3,6,7,13,15).[**Nov/Dec 2009]**

k. Analyse the following circuit right from the primitive state/flow table,state assignment and excitation table. **[Nov/Dec2010]**



l. Design an asynchronous sequential circuit with inputs A and B and an output Y. Initially and at any time if both the inputs are 0, the output, Y is equal to 0. When A or B becomes 1, Y becomes 1. When the other input also becomes 1, Y becomes 0. The output stays at 0 until circuit goes back to initial state. **[Nov/Dec 2014 R-13]**

m. An asynchronous sequential circuit is described by the following excitation and output functions: $Y=X_1X'_2+(X_1+X'_2)_y$,$Z=Y$ .Draw a logic diagram of the circuit. Derive the transition table and output map. **[April/May2010], [Nov/Dec 2009][Nov-Dec-2009 R-08]**



n. Differentiate between Moore Machine and Mealy Machine.(4m). **[Nov/Dec 2009]**

o. Design an asynchronous circuit that will O/P only the first pulse received whenever a control I/P is asserted from low to high state. Any fourth pulses will be ignored. **(May 2008)**

p. Design an asynchronous circuit using JK FF that will O/P only the first pulse received and will ignore any other pulses. **(May 2008)**

q. Design a T-FF giving the flow table, state table, state assignment, excitation table and excitation map. **(Nov 2008)**

r. Write short notes on:
   (i)Race free assignments.
   (ii)Pulse mode circuits**. (Nov 2007)**

s. The circuit has two inputs T(toggle) and C(clock) and one output Q.The output state is completed if T = 1 and clock c changes from 1 to 0 (negative edge triggering) otherwise ,under any other input condition , the output Q remains unchanged.Derive the Primitive flow table and Implication table. **(Nov 2007)**

t. Draw the fundamental mode and pulse mode asynchronous circuit and explain in detail. **(May 2007), (Nov 2006)**

u. Obtain the primitive flow table for an asynchronous circuit with two inputs (T and P)and one output (Z) . The output toggles when T=1 and P input goes from 1 to 0 .For all other conditions, output change, Assume initially Z =0. **(Nov 2006)**

v. Design a circuit with primary input A and B to give an output Z equal to 1 when A becomes 1 if B is already 1. Once Z = 1 it will remain so until A goes to 0.Draw waveform diagram, total state diagram, primitive flow table for designing this circuit**.(May 2006)**

w. Design a circuit with inputs A and B to give an output Z =1 when AB = 11 but only if A becomes 1 before B, by drawing total state diagram, primitive flow table and output map in which transient state is included. **(May 2006)**