UNIT-I : CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS AND ARCHITECTURES

CMOS: Introduction to MOSFET physics - Noise: Thermal, shot, flicker, popcorn noise - Transceiver specifications: Two port Noise theory, Noise figure, THD, IP2, IP3, sensitivity, SFDR - phase noise - Transceiver Architecture: Receiver: Homodyne, Heterodyne, Image reject, Low-IF Architecture - Transmitter: Direct-up conversion, Two-step up conversion schemes.

MOSFET Physics - Introduction

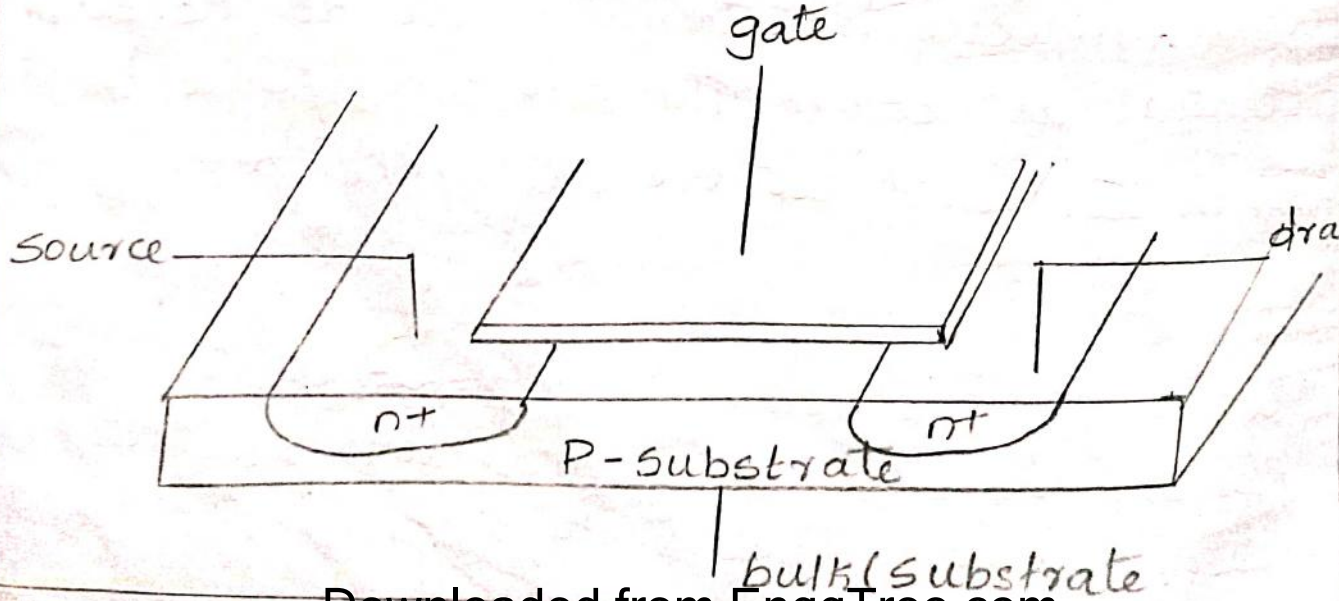
A basic n-channel MOSFET consist of two heavily doped n-type regions, the source and drain that forms the main terminals of the devices the gate is lightly doped. The substrate terminal is at the same potential as source. The substrate forms the fourth terminal whose influence cannot be ignored

when positive Voltage is applied at the gate holes are repelled away from the substrate At, some point of gate Voltage (Threshold Voltage)

V_t, the surface becomes charge depleted. Further increase in gate voltage induce inversion layer of electrons supplied by source or drain that constitute a conductive path or channel between drain and source. When gate-source voltage is above V_t, the device is said to be in strong inversion.

with assumption of drain to zero voltage is zero, the induced inversion charge is proportional to the gate voltage above the threshold, and the induced charge density is constant along the channel.

If we apply a positive drain voltage V, the channel potential must increase from 0 at the source to V at drain end. The net voltage there to induce an inversion layer decreases when reaches the drain end of the channel. The induced channel charge density will vary from max at source to min at drain of the channel.



Thus the channel charge density be

$$Q_n(y) = -C_{ox}\{[V_{gs} - V(y)] - V_t\}$$

where $Q_n(y)$ is the charge density at y Position

C_{ox} is ε_{ox}/t_{ox}.

$V(y)$ is channel potential at y Position

as we follow y-direction along the channel.

C_{ox} is capacitance per unit Area.

The negative sign implies the charges are made of electrons in NMOS.

DRAIN CURRENT IN LINEAR (TRIODE REGION)

The linear or triode region is defined as one in which V_{gs} is large enough for the formation of inversion layer from the distance from source to drain.

$$[V_{gs} - V(y)] - V_t = 0$$

The charge density becomes zero at drain at some voltage. Thus the boundary for triode region is

$$[V_{gs} - V_{ds}] - V_t = 0 \Rightarrow V_{gs} - V_t = V_{ds} \cong V_{dsat}$$

As long as $V_{ds} < V_{dsat}$, the device is in linear region of operation

The expression of the devices current in terms of variable

$$I_D = -W Q_n(y) v(y)$$

The velocity at low fields at is simply the product of mobility and electric field

$$I_D = -W Q_n(y) \mu_n E.$$

where W is width of device.

Substituting for charge density

$$I_D = -W C_{ox} [V_{gs} - V(y) - V_t] \mu_n E$$

The y directed electric field E is simply the gradient of voltage along the channel.

$$\therefore I_D = \mu_n C_{ox} W [V_{gs} - V(y) - V_t] \frac{dV}{dy}$$

so that

$$I_D dy = \mu_n C_{ox} W [V_{gs} - V(y) - V_t] dV.$$

on integration

$$\int_0^L I_D dy = I_D L = \int_0^{V_{ds}} \mu_n C_{ox} W [V_{gs} - V(y) - V_t] dV$$

∴ The expression for drain current in triode region

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

Thus MOSFET in triode region behaves as voltage controlled resistor.

DRAIN CURRENT IN SATURATION

when Vds is high, the inversion layer does not extend from source to drain so the channel is said to be 'pinched off'. In this condition, the field in channel charges increase causing total current to remain constant despite of increase in Vds.

to calculate current easily substitute Vdsat for Vds.

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{gs}-V_t)V_{dsat} - \frac{V_{dsat}^2}{2}\right]$$

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{gs}-V_t)^2$$

In saturation, the drain current has square dependent on gate source voltage and is independent on drain voltage. As Vaccum tube pentodes exhibit a similar insensitivity This regime is called the pentode region of operation

The transconductance in saturation for drain current by differentiating be

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{gs}-V_t)$$

Also expressed as

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}$$

with bipolar devices, a long channel MOSFET's transconductance depends on the square root of bias current.

CHANNEL-LENGTH MODULATION

So far we have assumed the drain current is independent of drain source voltage in saturation. The primary mechanism responsible for non-zero output conductance in long channel device is channel length Modulation (CLM)

The drain current in both triode and saturation is

$$I_D = (1 + \lambda V_{ds}) I_{DO}.$$

λ - Early voltage
I_{DO} - I_D when CLM are ignored

OPERATION IN WEAK INVERSION

The MOSFET devices conducts no current until inversion layer forms. The mobile carriers don't disappear the moment the gate voltage drops below V_t.

As V_{gs} drops below threshold the current decreases in exponential fashion much like BJT.

NOISE

The sensitivity of communication system is limited by noise. The fundamental noise source exist was identified in vacuum tube amplifier. Engineers had access to gain to make the noise sources. There were no improvement in further cascading amplifies as a mysterious noise exists along with signal. In audio system this as continuous hiss while, in video as characteristics 'snow' of analog TV signals.

THERMAL NOISE

Thermally agitated charge carriers in a conductor has varying current that rises random voltage. Thermal noise is also called as johnson noise, less frequency noise and nyquist noise.

Due to noise in random, we cannot identify a specific value of voltage at any particular time and only way to identify the noise is by statistical measures like mean square or root mean square values. Due to thermal, there is dependence on absolute temperature, where the thermal noise power is exactly proportional to T. a quantity called available noise power and is given by

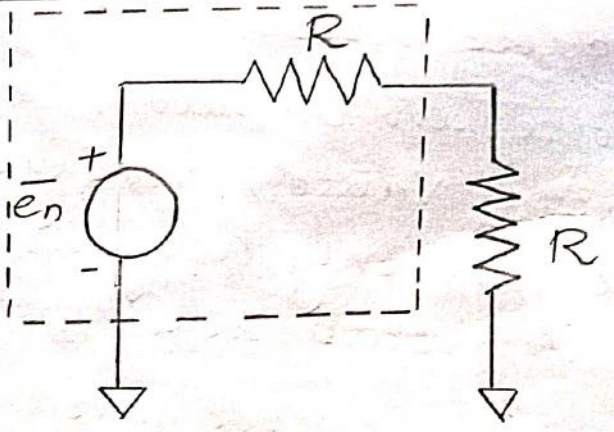
$$P_{NA} = KTAf.$$

Where K is Boltzmann's constant (1.38×10^{-23} J/k). T is absolute temperature in k Δf is noise bandwidth in hertz.

The available noise power is not dependent of frequency and grows (ie) the total power grows as with bandwidth without limit.

The noise power over 1-Hz bandwidth is about 4×10^{-21} W (or -174 dBm)[5] at room temperature. The noise power is same in interval between 1 MHz and 2 MHz to 1 GHz and 1.001 GHz as noise power is same over any bandwidth. Thermal noise is often called as 'white' by analogy with white light.

THERMAL NOISE OF RESISTOR



The noise voltage generator in series with resistor. The power delivered by this noisy resistor to another resistor of equal value is given by definition of available noise power

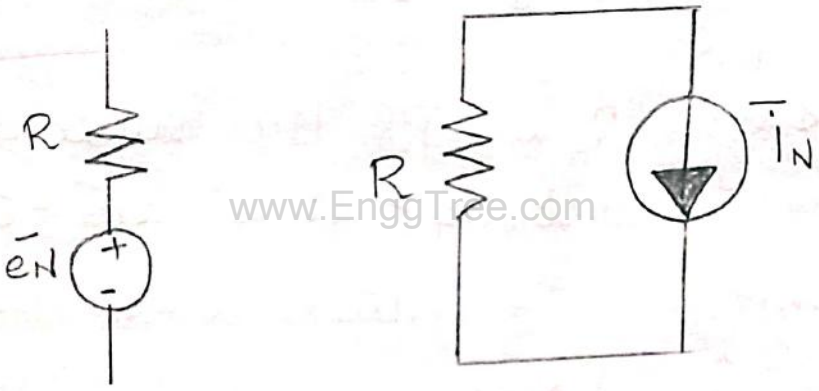
$$P_{NA} = KT\Delta f = \frac{\overline{e_n^2}}{4R}$$

where e_n is open circuit rms noise voltage generated by resistor R over bandwidth Δf at given temperature. The mean square open circuit noise voltage is given by

$$\overline{e_n^2} = 4KTR\Delta f.$$

At room temperature a 1 kΩ resistor generates 4nV of rms noise over bandwidth of 1Hz, while 50Ω generates 0.9nV of rms noise over same bandwidth.

RESISTOR THERMAL NOISE MODELS



$$\overline{e_n^2} = 4KTR\Delta f \qquad \overline{i_n^2} = \frac{\overline{e_n^2}}{R^2} = \frac{4KT\Delta f}{R}$$

$$= 4KT\Delta f$$

The noise bandwidth is

$$\Delta f \equiv \frac{1}{|H_{PK}|^2} \int_0^\infty |H(f)|^2 df.$$

H_{PK} is peak value of magnitude of filter voltage transfer function H(f)

For a single pole RC low pass filter the -3-dB bandwidth (hertz) is simply $1/2\pi RC$, but the equivalent noise bandwidth is as

$$\Delta f \equiv \frac{1}{|H|^2} \int_0^\infty \left[\frac{1}{(2\pi R f C)^2 + 1} \right] df$$

$$= \frac{1}{2\pi RC} \arctan 2\pi f RC \Big|_0^\infty$$

$$= \frac{\pi}{2} f_{3\,dB} = \frac{1}{4RC}$$

The single pole LPF has noise bandwidth is about 1.57 times the -3-dB bandwidth.

Similarly calculation shows that a critically damped second order LPF has noise bandwidth is about 1.22 times the -3-dB bandwidth.

A more general expression for the Thermal noise voltage is as

$$\overline{e_n^2} = \frac{hwR\Delta f}{\pi} \coth\left(\frac{hw}{4\pi kT}\right)$$

h is plank's constant which is 6.62×10^{-34} J-s

THERMAL NOISE IN MOSFET

Both BJT and MOSFET are voltage controlled resistors, they exhibit thermal noise. In Triode region, practically there will be noise with resistance value

The expression for drain current noise in FETs

$$\overline{i_{nd}^2} = 4kT\gamma g_{do}\Delta f$$

where g_{do} is drain source conductance at zero V_{ds}. The parameter γ has value of unity at zero V_{ds}, in long devices, decreases toward a value of 2/3 in saturation

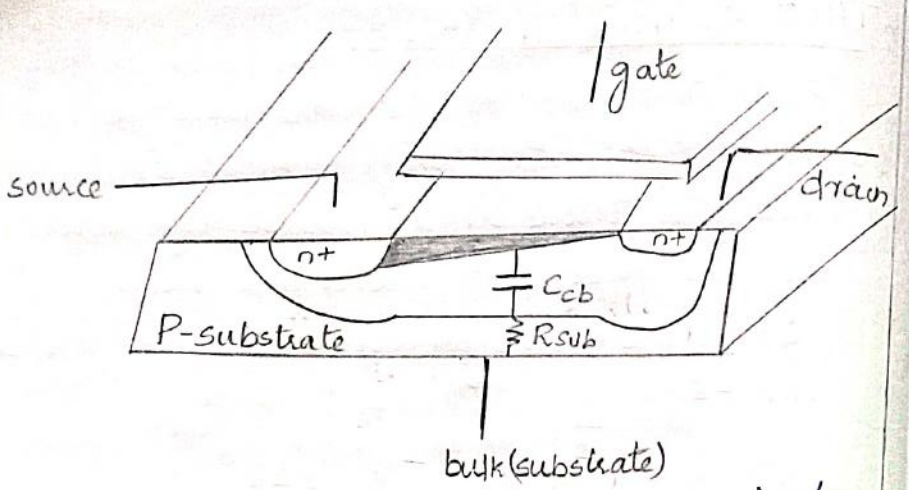
In some cases shows that short channel NMOS devices exhibit noise in excess of values predicted by long channel theory.

SUBSTRATE THERMAL NOISE

The thermal noise associated with the substrate resistance can produce measurable effect at main terminal of devices

The Thermal noise R_{sub} modulate the potential of back gate contributing noise drain current

$$\overline{i_{nd,sub}^2} = 4kTR_{sub}g_{mb}^2\Delta f$$



Depending on bias condition and also on magnitude of substrate resistance and size of back gate transconductance the noise generated is often called epi noise.

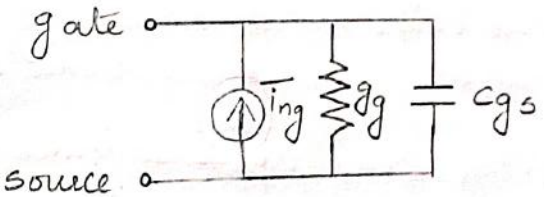
The physical structure and corresponding frequency-dependent expression is for substrate noise is

$$\overline{i^2_{ndsub}} = \frac{4KTR_{sub}g^2_{mb}}{1+(\omega R_{sub}C_{cb})^2}\Delta f$$

GATE NOISE

In addition to thermal noise agitation of channel charge has other outcome: gate noise. The floating channel potential couples capacitively into gate terminal leading to noisy gate current Vander ziel's expression gate noise is as $\overline{i^2_{ng}} = 4KTS_{gg}\Delta f$

$$g_g = \frac{\omega^2 C^2_{gs}}{5g_{do}}$$



The gate noise current has a spectral density that is not constant and increases with frequency and ought to be called 'like' noise' to continue the optical energy.

The alternative gate noise is given by.

$$r_g = \frac{1}{g_g}\cdot\frac{1}{Q^2+1} \simeq \frac{1}{g}\cdot\frac{0}{Q^2} = \frac{1}{5g_{do}}$$

SHOT NOISE.

Shot noise was explained by Schottky in 1918 and occasionally known as schottky noise, which is granular nature of electronic charge

Two conditions for shot noise to occur.

(i) There must be direct current flow and also a potential barrier over which the charge carriers hop.

(ii) Ordinary, linear resistors do not generate shot noise despite of quantized nature of electronic charge.

The shot noise is given by.

$$\overline{i_n^2} = 2qI_{DC}\Delta f.$$

$\overline{i_n^2}$ - rms of noise current

q - quantum electronic charge (1.6×10^{-19} C)

I_{DC} - DC current in A.

Δf - noise bandwidth in Hertz.

The shot is not corruption of 'schottky' on connection of audio system with a source of shot noise biased at very low current, the resulting sound is much like that of buck shot (pellets) dropping onto a hard surface.

FLICKER NOISE

The mysterious type of noise is flicker noise, also known as 1/f noise or pink[20] noise).

The term 1/f suggests, the noise is characterized by a spectral density that increases without time limit as frequency decreases. Due to lack of unifying theory, the mathmatical expression for 1/f noise contain various Empherical parameters as below

$$\overline{N^2} = \frac{k}{f^n}\Delta f.$$

$\overline{N}$ is rms noise (either Voltage or current).

K is empirical parameter.

The parameter n is occuring at value of unity, on integration the density to find noise in frequency band bounded by lower frequency f_1 and upper frequency f_2 is given by

$$\overline{N^2} = \int_{f_L}^{f_h} \frac{k}{f} df = k \ln\left(\frac{f_h}{f_L}\right)$$

which says the total mean-square noise depends on the log of the frequency ratio.

FLICKER NOISE IN RESISTOR

The noise in resistor is often called excess noise as this noise is in addition to what is expected from thermal noise

Carbon film resistors exhibits less noise than carbon composition types. It is true that excess noise increases with Dc, so one must minimize Dc drop across a resistor.

$$\overline{e_n^2} = \frac{K}{f} \cdot \frac{R_\square^2}{A} \cdot V^2 \Delta f$$

A is Area of resistor
$R_\square$ is sheet resistivity
V is the Voltage across resistor, K is material specific parameter.

FLICKER NOISE IN MOSFET

In electronic devices, 1/f noise raises from a number of different mechanism and it is more significant in MOSFET than in bipolar devices as MOSFET devices are surface devices, they exhibit this type of noise to a much greater degree than bipolar. Larger MOSFETs exhibits less 1/f noise because of their large gate capacitance smooths the fluations at channel charge

The mean-square 1/f drain noise current is given by

$$\overline{i_D^2} = \frac{K}{f} \cdot \frac{g_m^2}{WLC_{ox}^2} \cdot \Delta f$$

$$\approx \frac{K}{f} \cdot W^2 T \cdot A \cdot \Delta f$$

where A - area of gate and K is device-specific constant. Thus for a fixed transconductance, a larger gate area and thinner dielectric reduce this noise term.

FLICKER NOISE IN JUNCTIONS

Foswaed-biased junctions also exhibit 1/f noise. The noise is proportional to the bias current and inversly Proportional to junction Area

$$\overline{i_J^2} = \frac{K}{f} \cdot \frac{I}{A_j} \cdot \Delta f$$

K is constant and value of around 10^{-25} A-m^2

POPCORN NOISE

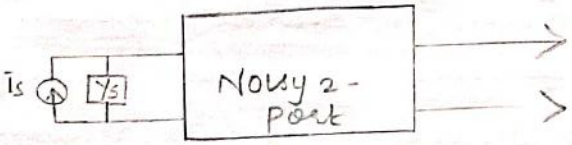
Another type noise in semiconductor is known as popcorn noise, Also known as burst noise, bistable noise, random telegraph signals RTS)

Gold plated BJT exhibit highest level of burst noise and may be sensitively to contamination by metal done

This noise was observed in point-contact diode, ordinary junction diode and tunnel diode, resistor of some type and both discrete and integrated circuit junction transistor.

The equation is

$$\overline{N^2} = \frac{K}{1+(f/fc)^2}\Delta f.$$



K is emphirical value.

fc is corner frequency

For frequency below fc, the first noise density flattens out.

for frequency well above fc, the total mean square noise between f1 and fh is

$$K f_c^2 \left[\frac{1}{f_1} - \frac{1}{f_h}\right].$$

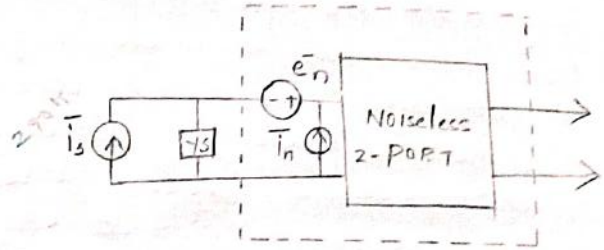
TRANSCEIVER SPECIFICATIONS:

to optimize noise perform in cls

TWO PORT NOISE THEORY

NOISE FACTOR.

A useful measure of the noise Performance of a system is the noise factor denoted by F



A noisy two port driven by source with admittance Ys and equivalent shunt noise current $\bar{i}_s$. We are concerned only with overall input-output behaviour and unnecessary to track of all internal noise sources and the net effect of all sources can be represented by one pair of external sources:- a noise voltage and noise current.

The noise factor is defined by

$$F \equiv \frac{\text{total output noise power}}{\text{output noise due to input source}}$$

By convention, the source is at a temperature of 290 K. The noise factor is a measure of degradation in signal-to-noise ratio that system introduces. The larger the degradation, the larger the noise factor. If a system adds no noise of its own, the total output noise is due to source only and noise factor is unity

An equivalent method is to compute the total short-circuit mean square noise current and then divide the total by short circuit mean square current due to input source. In this the power contributions are proportional to short circuit mean square current with proportionality constant.

While using this we may encounter the problem of combining noise sources that are varying in degree of correlation with each other

In this special case of zero correlation the expression for noise figure

$$F = \frac{\overline{i_s^2} + |i_n + Y_s e_n|^2}{i_s^2} \quad -①$$

For correlation between e_n and i_n. make i_n as sum of two components. one i_c is correlated and with e_n and other i_u is not correlated.

$$i_n = i_c + i_u \quad -②$$

since i_c is correlated with e_n

$$i_c = Y_c e_n \quad -③$$

Y_c is correlation admittance

combining ①, ② and ③

The factor becomes

$$F = \frac{\overline{i_s^2} + |i_u + (Y_c + Y_s) e_n|^2}{i_s^2}$$

$$\overline{i_s^2} + |(i_c + i_u) + Y_s|^2 = n$$

$$i_s^2 = |(Y_c e_n) + i_u| Y_s^2$$

$$F = \frac{(Y_c + Y_n) e_n + i_u}{i_s^2} \quad (2)$$

$$= 1 + \frac{\overline{i_u^2} + |Y_c + Y_s|^2 \overline{e_n^2}}{\overline{i_s^2}} \quad -④$$

(2) (1) (3)

eqn ④ contains three independent noise sources, each is treated as thermal noise produced by equivalent resistance or conductance.

$$R_n \equiv \frac{\overline{e_n^2}}{4KT\Delta f} \quad -⑤$$

$$G_u \equiv \frac{\overline{i_u^2}}{4KT\Delta f} \quad -⑥$$

$$G_s \equiv \frac{\overline{i_s^2}}{4KT\Delta f} \quad -⑦$$

using these equivalences, the expression for noise factor is written in terms of as impedence and admittance

$$F = \frac{1 + G_u + |Y_c + Y_s|^2 R_n}{G_s}$$

(impedence → , conductance →)

$$= \frac{1 + G_u + [(G_c + G_s)^2 + (B_c + B_s)^2] R_n}{G_s} \quad -⑧$$

(sum →)

Here each admittance into sum of conductance G and susceptance B.

OPTIMUM SOURCE ADMITTANCE

once two port noise is given by four noise parameters G_c, B_c, R_n and G_u eqn ⑧ given condition for minimizing noise factor with first derivative into respect of source addmittance with zero set.

$B_s = -B_c = B_{opt}$ (susceptance admittance)

$$G_s = \sqrt{\frac{G_u}{R_n} + G_c^2} = G_{opt}$$

To minimize the noise factor, the source susceptance should be made equal to the inverse of correlation susceptance, while source conductance should be set to value in G_{opt}.

$$F_{min} = 1 + 2R_n[G_{opt} + G_c]$$

$$= 1 + 2R_n\left[\sqrt{\frac{G_u}{R_n} + G_c^2} + G_c\right]$$

We may express noise factor in terms of F_{min} and source admittance

$$F = F_{min} + \frac{R_n}{G_s}\left[(G_s - G_{opt})^2 + (B_s - B_{opt})^2\right]$$

Thus contours of constant noise factor are non-overlapping circles in admittance plane.

LIMITATIONS OF CLASSICAL NOISE OPTIMIZATION.

In RF design, the freedom to choose I_C relation there is no specific guidance is given that what device size will reduce noise.

Power consumption is not considered in classical noise optimization.

NOISE FIGURE

other than noise factor, the other figure of merit is noise figure and noise temperature

The Noise Figure (NF) is the noise factor expressed in decibles

Noise Temperature T_N is an alternative way of expressing the effect of an amplifier's noise contribution and defined as the increase in temperature required of the source resistance for it to account for all of the output noise at reference temperature T_{ref} (290K).

$$F = 1 + \frac{T_N}{T_{ref}} \Rightarrow T_N = T_{ref}(F-1)$$

An amplifier that adds no noise of its own has a noise temperature of 0K.

Noise Temperature is useful for describing the performance of cascaded amplifiers whose noise factor is close to unity

THD - Total Harmonic Distortion

HARMONIC DISTORTION

The harmonic distortion RF circuits are due to non linearities

If sinusoid is applied to non-linear system, the output exhibit frequency components that are integer of input frequency ω = fundamental frequency.

$$y(t) = \alpha_1 A\cos\omega t + \alpha_2 A^2\cos^2\omega t + \alpha_3 A^3\cos^3\omega t.$$

$x(t)$ → [NS] → $y(t)$

$x(t)$ → [LTI system response] → $y(t)$

$$= \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t)$$

$$= \alpha_1 A\cos\omega t + \frac{\alpha_2 A(1+\cos 2\omega t)}{2} +$$

$x(t) = A\cos\omega t$

$$\alpha_1 A\cos\omega t + \alpha_2 A^2\cos^2\omega t + \frac{\alpha_3 A^3}{3}(3+\cos\omega t+\cos 3\omega t)$$

* signal Quality Degradation
* spectral purity
* cross talk and interference

$$+\frac{\alpha_2 A^2}{2}\cos(2\omega t) + \frac{\alpha_3 A^3}{4}\cos(3\omega t) + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)\cos\omega t$$

→ harmonic operated with bandwidth

SECOND INTERCEPT POINT IP2

IP2 is also known as SOI, IIP2 is a measure of linearity that quantifies the second order distortions generated by non-linear system and devices.

It is an interpolated point, where the fundamental component power curve meets the second order intermod (IMD2

Consider non linear amplifier whose input to output characteristic is given by

3rd order polynomial.

$$V_o(t) = \alpha_0 + \alpha_1 V_i(t) + \alpha_2 V_i(t) + \alpha_3 V_i(t) \quad -①$$

$V_o(t)$ is output of amplifier

$V_i(t)$ is input voltage to the amplifier.

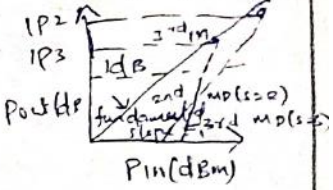
Generally a two tone test is used to compute IP3 for

$$V_i = A_{i,1}\cos(\varphi_1) + A_{i,2}\cos(\varphi_2)$$

omega

$$\varphi_1 = \omega_1 t + \phi_1$$

$$\varphi_2 = \omega_2 t + \phi_2 \quad -②$$



Substituting eqn ② in ①

$$V_o = \alpha_1 + \alpha_3\left(\frac{3}{4}A_{i,1}^2 + \frac{3}{2}A_{i,2}^2\right)A_{i,1}\cos\varphi_1 + \alpha_1 + \alpha_3\left(\frac{3}{4}A_{i,2}^2 + \frac{3}{2}A_{i,1}^2\right)$$

fundament.

$$+\frac{1}{2}\alpha_2(A_{i,1}^2\cos 2\varphi_1 + A_{i,2}^2\cos 2\varphi_2)$$

2nd harmonic.

At second order IP2 ≃ second order IM_2

$$\left(\alpha_1 + \alpha_3\left(\frac{3}{4}A_{i,1}^2\right)\right)A_{i,1} = \frac{1}{2}\alpha_2 A_{i,1}A_{i,1}$$

$$\alpha_1 A_{i,1} \simeq \frac{1}{2}\alpha_2 A_{i,1}A_{i,2}.$$

2nd order intermod component in output voltage

$$\frac{V_{o,1}}{V_{o,IMD2}} = \frac{\alpha_1 A_{i,1}^2}{\frac{1}{2}\alpha_2 A_{i,1}A_{i,2}} = \frac{A_{IP2}}{A_{i,2}}$$

THIRD INTERCEPT POINT

The concept of IP3 originates from observation if amplitude of each tone rises that of output IM products increase more sharply at αA^3. if we raise Amplitude of IM products become equal to fundamental tones at output.

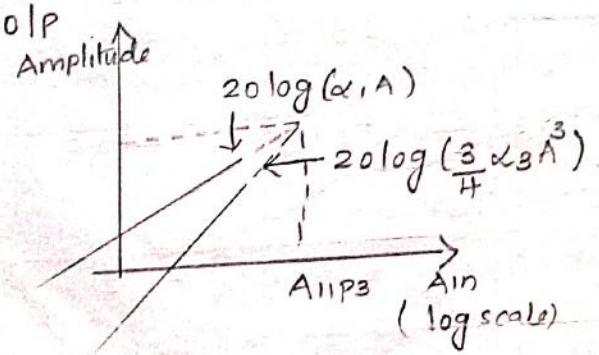
To find IIP3

$$|\alpha_1 A_{IIP3}| = \left|\frac{3}{4}\alpha_3 A^3_{IIP3}\right|$$

$$A_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|}$$

$$\frac{A_{IIP3}}{A_{1dB}} = \sqrt{\frac{4}{0.435}}$$

$$\approx 9.6\ dB.$$



SENSITIVITY.

which is defined as the minimum signal level that a receiver can detect with the acceptable quality.

In presence of more noise, the detected signal becomes unintelligle and carries little information.

SNR in range of 6 to 25 dB.

Sensitivity can be written as

$$NF = \frac{SNR_{in}}{SNR_{out}}$$

$$= \frac{P_{sig}/P_{RS}}{SNR_{out}}$$

P_{sig} - input signal power and

P_{RS} - source resistance noise power.

$$P_{sig} = P_{RS} \cdot NF \cdot SNR_{out}.$$

To obtain total mean squared power.

$$P_{sig.tot} = P_{RS} \cdot NF \cdot SNR_{out} \cdot B.$$

$$P_{sen}|_{dBm} = P_{RS}|_{dBm/Hz} + NF|_{dB} + SNR_{min}|_{dB} + 10\log B.$$

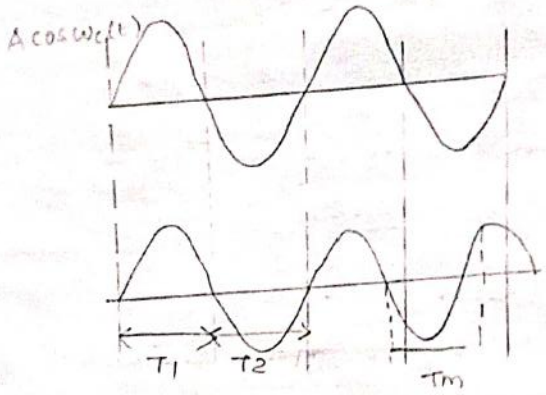
P_{sen} is sensitivity and B in z is directly depend on gain of the system,

If receiver is matched to antenna $P_{RS} = KT = -174$ dBm/Hz.

$$P_{sen} = -174\ dBm/Hz + NF + 10\log B + SNR_{min}.$$

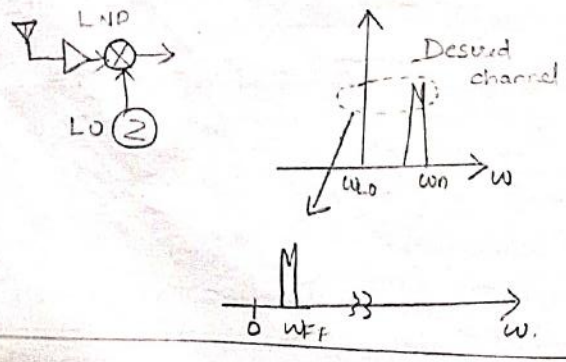
PHASE NOISE

An ideal oscillator produces perfectly-periodic output of the form $x(t) = A\cos \omega_c t$. The zero crossing occur at exact inter multiples of $T_C = 2\pi/\omega_c$.



$$x(t) = A\cos[\omega_c t + \phi_n(t)]$$
$$\simeq A\cos\omega_c t - A\sin\omega_c t \sin[\phi_n(t)]$$
$$\alpha A\cos\omega_c t - A\phi_n(t) \sin\omega_c t.$$

EFFECT OF PHASE NOISE



TRANSCEIVER ARCHITECTURE:

RECEIVER

There are 2 main architecture and RF receiver of any s/m.

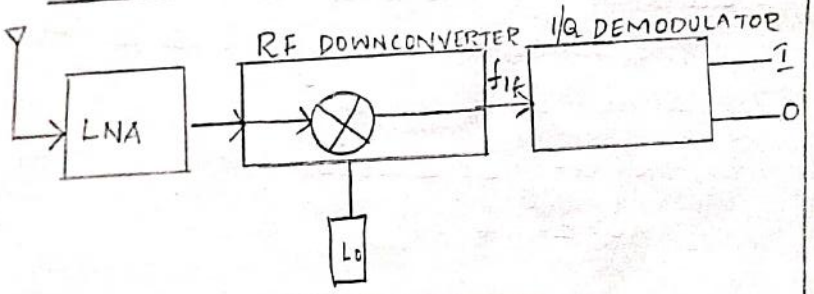
They are.

(i) Heterodyne

(ii) Homodyne

where both converts modulated RF signal to baseband I/Q signal zero IF frequency.

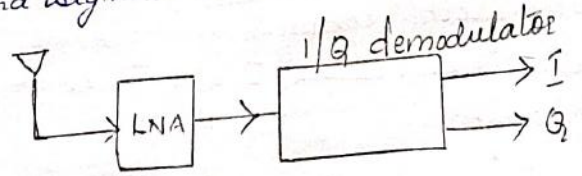
HETERODYNE RECEIVER.



It requires one mixer to bring the modulated RF signal to modulated IF signal, which is applied to I/Q de-modulator which brings the modulated low IF to baseband at zero IF

HOMODYNE RECEIVER

In homodyne receiver, it does not require any mixers at RF stage. The modulated RF signal is directly applied to I/Q demodulator which gives base band signals out (I and Q) at zero F.

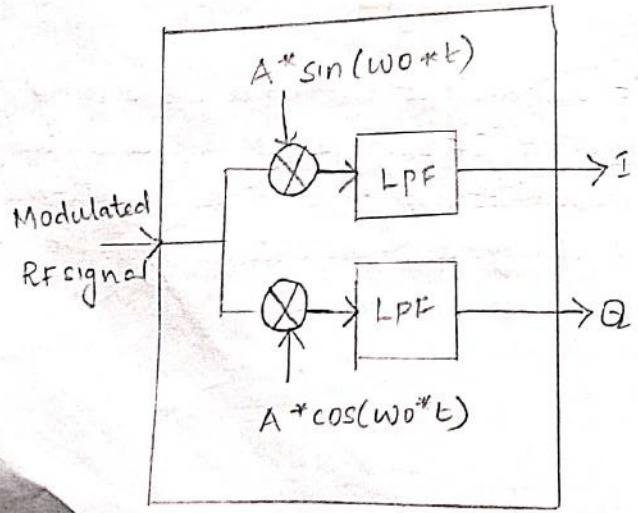


295
306

This I/Q demodulator circuit which is used in all modems that converts the modulated IF/RF signal to baseband signal at zero frequency.

fo frequency is choosen.

Wo = 2*pi*fo.



The signal is first amplified at low noise stage known as LNA. After the low noise amplification signal is connected to base band. If RF frequency signal and LO frequency signal are equal the circuit operates as phase detector.

IMAGE REJECTION RECEIVER

Image reject architecture are another class of receivers that supress the image without filtering thereby avoiding the trade off between the image rejection and channel selection.

Define 90° phase shift.

$$A\cos(\omega_c t - 90^\circ) = \frac{A\, e^{+j(\omega_c t - 90^\circ)} + e^{-j(\omega_c t}}{2}$$

$$= -\frac{A}{2} j e^{+j\omega_c t} + \frac{A}{2} j e^{-j\omega_c t}$$

$$= A\sin\omega_c t.$$

Similarly in narrow band modulated signal $x(t) = A(t)\cos[\omega_c t + \phi(t)]$ we do 90° phase shift.

$$A(t)\cos[\omega_c t + \phi(t) - 90^\circ] = A(t) \frac{e^{+j(\omega_c t + \phi(t) - 90^\circ]} + e^{j(\omega_c t + \phi(t)}}{2}$$

$$= A(t) \frac{-j e^{+j[\omega_c t + \phi(t)]} + j e^{-j(\omega_c t + \phi(t)]}}{2}$$

$$= A(t)\sin[\omega_c t + \phi(t)].$$

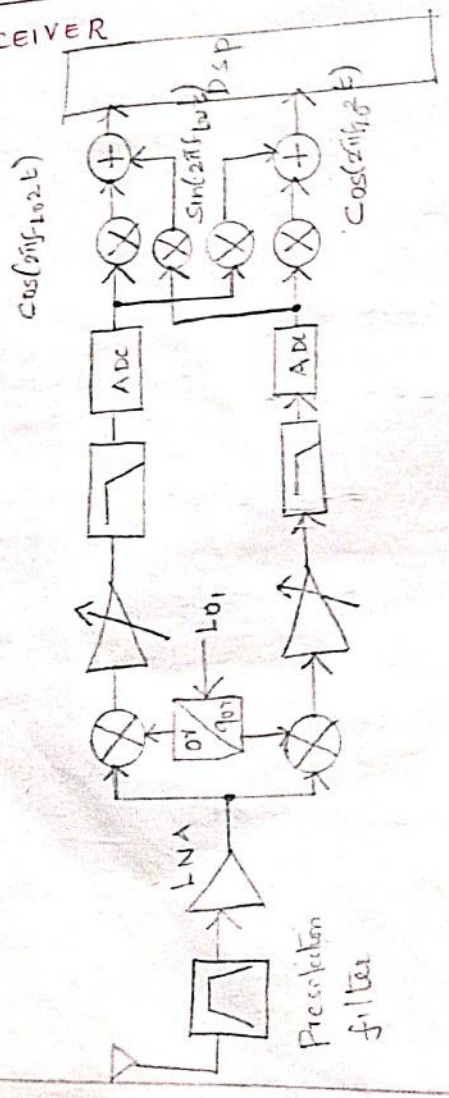
$$X_{90^\circ}(\omega) = X(\omega)[-j\,sgn(\omega)]$$

where sgn(ω) is sign function

This shift by 90° is called Hilbert transform which negates the original signal.

LOW IF RECEIVER ~~ARCHITECTURE~~

RECEIVER



At the hybrid out:

$$V_{OL,I} = V_{OL}\cos(\omega_0 t)$$

$$V_{OL,Q} = -V_{OL}\sin(\omega_0 t)$$

At the mixer out:

$$V_U = -K\,V_{OL}V_M\cos(\omega_0 t + \phi)\sin(\omega_0 t)$$

$$= \frac{1}{2}K V_{OL}V_M(\cos(2\omega_0 t + \phi) + \sin(\phi))$$

$$V_L = K V_{OL}V_M\cos(\omega_0 t + \phi)\cos(\omega_0 t)$$

$$= \frac{1}{2}K\,V_{OL}V_M(\cos(2\omega_0 t + \phi) + \cos(\phi))$$

The low pass (LP) filter removes the component at $2\omega_0$ (and all the others produced by the actual non-linearities). The output of two signals are then proportional to I and Q components of the modulated R.F signal.

Pros & cons.

* Reduced complexity
* Easier to integrate
* More susceptible to noise and distortion.
* ** DC offset voltage at the mixer output due to spurious signal from antennas

* Offset voltage at mixer output not easy to eliminate

TRANSMITER ARCHITECTURE.

The choice of Transmitter is determined by 2 Factor.

(i) wanted and unwanted emission requirements

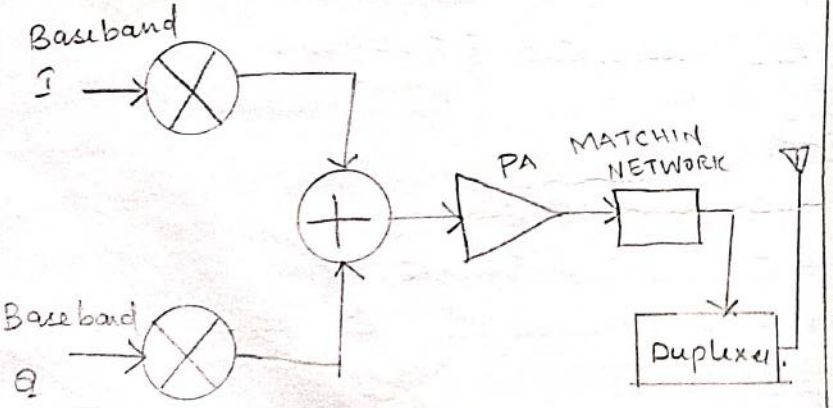
(ii) no of oscillators and external filters;

DIRECT UP CONVERSION ARCHITECTURE.

In direct conversion architecture:

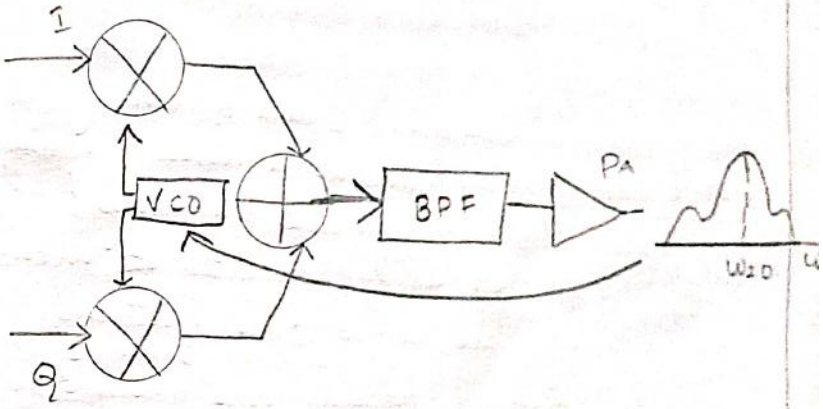
In direct conversion architecture transmitter the output carrier frequency is equal to the LO frequency and modulation, up. conversion occur in the same circuit.

The topology simplicity makes for high level of integration.



The direct - conversion drawbacks

* Disturbance of the local oscillator by the power amplifier output. This issue arises because the PA output is a modulated waveform having a high power and a spectrum centered around the LO frequency.

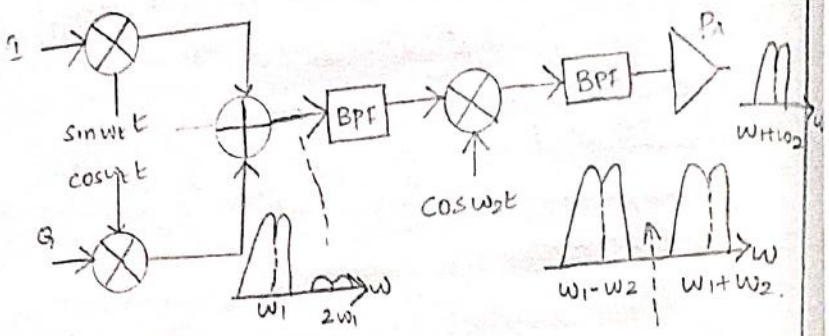


DIRECT UP CONVERSION TRANSMITTER

TWO-STEP UP ARCHITECTURE

Another approach to circumventing the problem of LO pulling in Transmitters is to up convert the baseband signal in two or more steps so that the PA output spectrum is far from the frequency of the Vco's.

TWO STEP TRANSMITTER.



The channels baseband I and Q undergo quadrature modulation at a lower frequency w_1 [called the intermediate frequency (IF)] and the result is upconverted to w_1+w_2 by mixing the band pass filtering. The first BPF suppresses the harmonics of the IF signal while the second removes the unwanted side band centered around w_1-w_2.

Advantages

Over the direct approach is that same quadrature modulation is performed at lower frequencies I and Q matching is superior leading to less cross-talk between two bit streams.

A channel filter may be used at the first IF to limit the transmitted noise and spurs in adjacent channels.

The difficulty in two-step transmitter is that the bandpass filter following the second upconversion must reject the unwanted side band by large factor typically 50 to 60 dB. This is because the simple upconversion operation produces both the wanted and the unwanted side bands with equal magnitude. Owing to higher center frequency, this filter is typically a passive, relatively expensive off-chip device.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

Another popular specification in communication system is spurious free dynamic range.

The two Variations

(i) single-tone SFDR

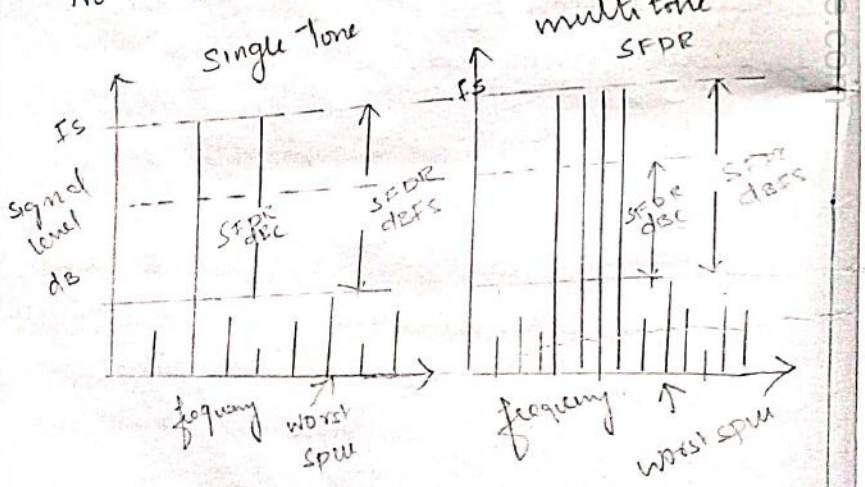
is the ratio of signal to the most spur in the band width of interest which is not harmonic and can be referenced to the signal or carrier level (dBc) or to full scale (dBFS)

The reference is minimum detectable signal level at the input of a receiver which can be calculated with noise figure and input signal bandwidth of the receiver. The difference between this value and the input level which will produce distortion products is equal to minimum detectable signal referred as to the input of the system is SFDR. This prouduces for ADC.

$$DR_f(dB) = \frac{2}{3}(P_3 - N_0)$$

P_3 - third order intercept point

N_0 - is noise component (dB/dBm).



Two Marks.

1. Can MOSFET conduct in both direction

Yes, MOSFET are bi-directional

2. What are the types of MOSFET and regions of operations?

Types.

* Enchancemode mode
* Depletion mode.

Region of Operations

(i) cut-off region
(ii) Linear region
(iii) saturation region.

3. List the effects of non-linearity in amplifiers.

The effects of non-linearity in amplifiers are

(i) Harmonic Distortion
(ii) intermodulation Distortion
(ii) Phase noise
(iv) other noise: Thermal, Pop corn noise flicker noise, and etc.

4. what are the chose of substrate material in amplifiers

* Most widely used substrate material is silicon, due to its excellent semiconductor properties, low cost and high integration density.

5. Derive expression for phase noise

$$x(t) = A\cos[\omega_c t + \phi_n(t)]$$
$$\simeq A\cos\omega_c t - A\sin\omega_c t \sin(\phi_n(t))]$$
$$\simeq A\cos\omega_c t - A\phi_n(t)\sin\omega_c t.$$

6. what is Noise figure

Noise figure is the Noise factor Expressed in decibles. usually the difference between the decibles of noise output of the actual (receiver) to the ideal (receiver) with same over all gain and band width matched to sources at stand noise temperature (290k).

7 what is image rejection

Image rejection is the measure of the receivers ability to reject the signals at image frequency. normally in dB.

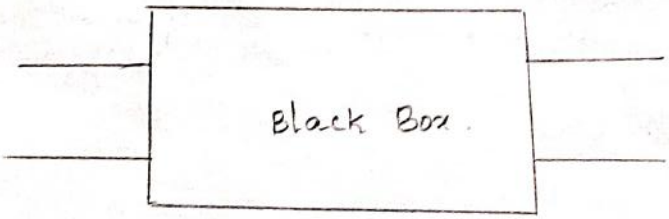
8. Dwhat are the Draw backs of Direct conversion Receiver.

* Dc offset - is coming from local oscillator leakage cause large Dc offset in the base band
* There is a small voltage in the local Oscillator and find a way as input of LNA, through mixer due to poor isolation. Even, there is isolation we will have small leakage as it is not possible to eliminate completely.

UNIT II : IMPEDENCE MATCHING NETWORK AND AMPLIFIERS.

Review of S-parameters and Smith chart - Passive IC components - impedence matching networks - Amplifiers : common Gate, common source Amplifiers - OC time constants in bandwidth estimation and enhancement - high frequency amplifier design - Low noise Amplifiers : Power match and noise Match, single - ended and differential LNAS.

REVIEW OF S-PARAMETERS.

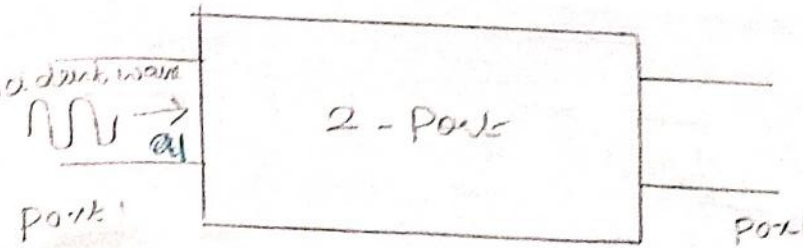


S-parameters are useful method for representing a circuit as 'Black box'

The external behaviour of this black box can be predicted without any regard for the contents.

This black box can be

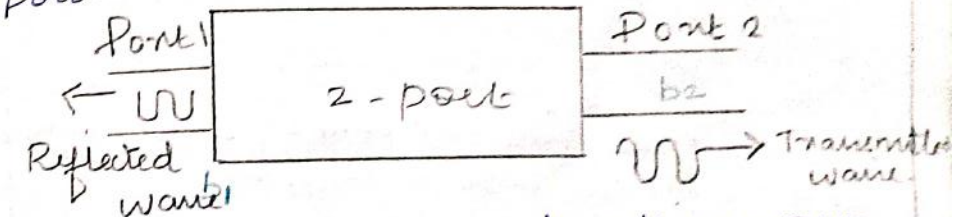
* A resistor
* a transmission line or
* a integrated circuit



This is a simple network with 2 ports

A port is terminal pair of wire.

S-Parameters are measured by sending a single frequency signal into the network and to detect what waves exit from each port.



Power, Voltage, current are travelling waves in both direction

The wave incident on port 1, some of the signal reflects back and some exit other port

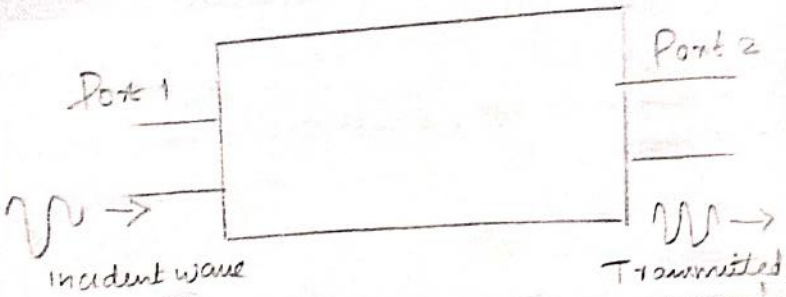
S_{11} refers to reflected at port 1 for signal incident at port 1.

* S-parameter S_{11} is ratio of two waves b_1/a_1

S_{21} refers to existing at port 2 for incident at Port 1.

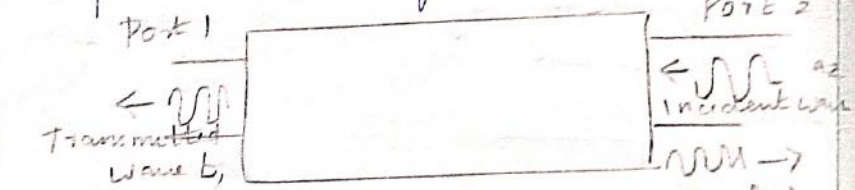
* S-Parameter S_{21} is ratio of two waves b_2/a_1

(S_{21} is considered of S_{12} → because responding Port is always first considered).



S_{21} refers to signal exiting at port 2 (b_2) for signal incident at port 1.

S-Parameter - ratio of 2 waves b_2/a_1



S_{22} is signal exiting at port 2 for port 2 incident signal. S_{22} is ratio of b_2/a_2

A linear network characterised by a set of simultaneous eqn describing exiting from each port in terms of incident wave.

$S_{11} = b_1/a_1$

$S_{12} = b_1/a_2$

$S_{21} = b_2/a_1$

$S_{22} = b_2/a_2$

The transmitted and reflected wave will have change in amplitude and phase from incident wave.

Generally reflected wave will be at same frequency as incident wave.

S-parameters are complex (ie they have magnitude and angle because both Magnitude and phase of input signal are changed by network and thus referred as complex scattering parameters.

These 4 S-parameters actually contain eight seperate number, ie the real and imaginary parts.

S-PARAMETERS DEPENDON

S-Parameter depend on the network and the characteristic impedence of the source and load use to measure it, and frequency measured at.

(ie)

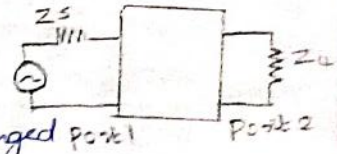
The S-parameter change

(i) when network change

(ii) when frequency is changed

(iii) when load impedence is changed

iv) whe source impedence is changed



MATRIX ALGEBRIC REPRESENTATION OF 2-PORT S-PARAMETERS:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \times \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$

S_{11}, S_{22} Reflection co-effcient [they refer to the reflection occurs at one port only]

S_{12}, S_{21} Transmission coffcient [transmission from one to another port]

some matrices are symmetrical about diagonal

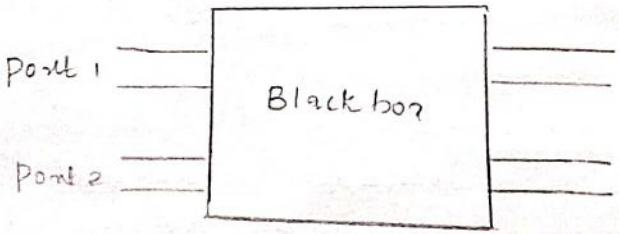
In 2 port network of symmetrical means $S_{21} = S_{12}$ and interchanging input and output Port does not change transmission properties

EXAMPLE OF 2-PORT SYMMETRICAL NETWORK IS A TRANSMISSION LINE

LARGER NETWORKS.

A network may have any number of ports.

* The S-matrix of an n-port contains n^2 coffients (S-parameters), each one representing a possible input-output path.
* The number of rows and columns in an S-parameters matrix is equal to the number of ports.
* S-parameter subscripts "ij" - j is port that is excited (input port) and "i" is the output port.



$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} \times \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix}$$

SMITCH CHART:

The reflection co-efficient Γ is given interms of normalized load impedence.

$$\Gamma = \frac{\frac{Z_L}{Z_0} - 1}{\frac{Z_L}{Z_0} + 1} = \frac{Z_{nL} - 1}{Z_{nL} + 1} \quad -(1).$$

REASONS FOR GOING TO SMITH CHARTS.

Smitch chart is more straight foward to plot the real and emaginary parts of impedence directly in standard cartesian co-ordinates.

* Because, plotting infinite impedence directly creates practical problems, and plotting in Γ handles impedence neatly as it cannot exceed unity for passive loads.
* Γ repeats every half-wavelength, when a lossless transmission line is terminated in a fixed impedence.

Eqn (1) is mapping of one complex numbers to another, so bilinear transformation is used, which is the ratio of two linear functions, because circles remain as circles when mapped and lines are considered as circles of infinite radius.

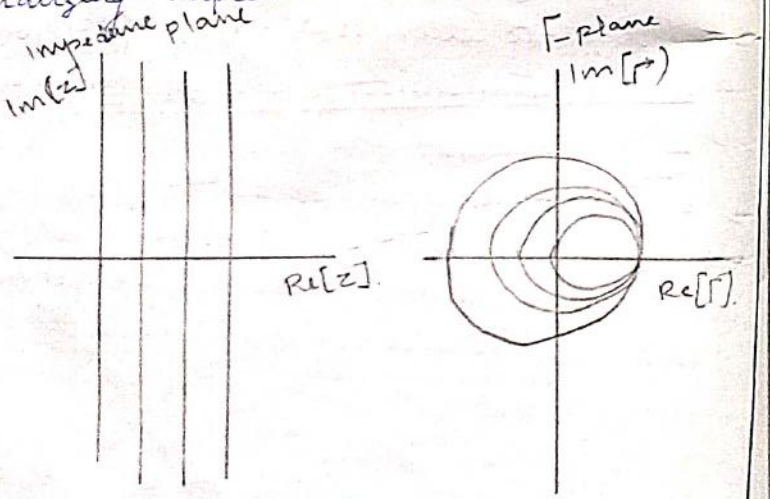
Hence circle and lines map into either circles or lines.

From Eqn (1), it is straight foward to

to show imaginary axis of z-plane maps into the unit circle of Γ-plane, while the other constant-resistance in z-plane maps to circle of varying diameter, that all are tangent at point Γ=1.

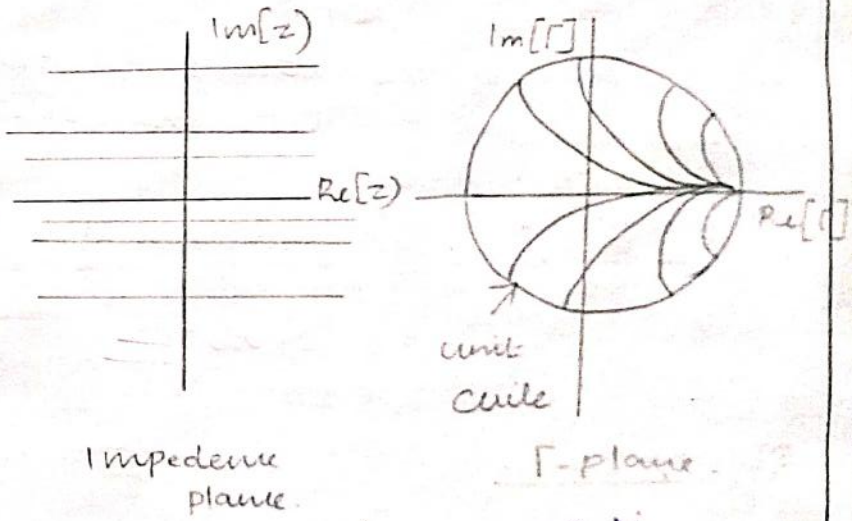
Lines of constant reactance are orthogonal to lines of constant resistance in z-plane since, lines maps to lines or circles, one expect constant reactance line to transform to the circular arcs.

The smith chart is just plotting of both constant-resistance and constant-reactance contour in Γ-plane without out explicit presence of Γ-plane axes. The center of smith chart corresponds to zero reflection coefficient and therefore, a resistance equal to the normalizing impedance.



* The bottom half of z-plane maps into the bottom half of unit circle in Γ-plane and thus capacitive impedence are found there.
* IIIrdly the top half of z-plane corresponds to the top half of unit circle and inductive impedence.
* The smaller circles of constant resistance correspond to progressively larger resistance values.

The point Γ = -1 corresponds to zero and the point Γ = 1 corresponds to infinite resistance (or) reactance.



VSWR - Voltage Standing Wave Ratio

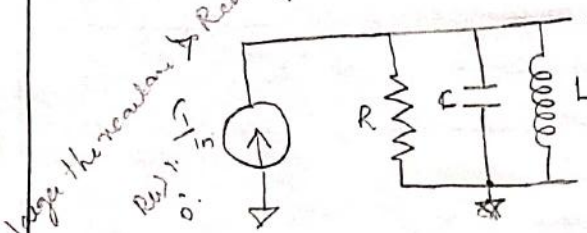
* is ratio between transmitted and reflected Voltage standing wave in RF transmission s/m.
* measures how RF power is transmitted from power source through transmission line to the load

PASSIVE IC COMPONENTS

PARALLEL RLC TANK:-

This circuit exhibits Resonant behaviour This circuit is often called as Tank circuit or simply tank.

We begin by studying its complex impedence or more directly its admittance (for parallel network)



At low frequency, the network admittance is essentially that of inductor and capacitor at very high frequency.

The Resonant frequency is given by.

$$\sqrt{\frac{V^2}{R^2}+\left(\frac{V}{X_L}-\frac{V}{X_C}\right)^2}\left(\omega_0 C-\frac{1}{\omega_0 L}\right)=0 \Rightarrow \omega_0=\frac{1}{\sqrt{LC}}$$

$f_0 = 1/2\pi\sqrt{LC}$ - Resonant

QUALITY FACTOR:

$$Q = \omega \frac{\text{Energy stored}}{\text{Average power dissipated}}$$

At Resonant frequency the energy in network moves back and forth between the inductor and capacitor with a constant sum at resonance.

Network Energy and power is given by

$$E_{avg} = \frac{1}{2} C (I_{PK} R)^2$$

$$P_{avg} = \frac{1}{2} I_{PK}^2 R$$

Q is given by

$$Q = \omega_0 \frac{E_{wc}}{P_{avg}} = \frac{1}{\sqrt{LC}} \cdot \frac{\frac{1}{2} C (I_{PK} R)^2}{\frac{1}{2} I_{PK}^2 R}$$

$$= \frac{R}{\sqrt{L/C}}$$, where $\sqrt{L/C}$ is charastic impedence

SERIES RLC NETWORK.

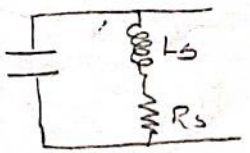
The equation for Q involves the same terms as for parallel case. The reciprocal form

$$Q = \frac{\sqrt{L/C}}{R}$$

At, resonance, the voltage across either the inductor or capacitor is Q times as great as that resistor.

ORTHER RESONANT RLC NETWORKS:

Pure parallel or series RLC network rarely exist so well will consider a realistic examples.



$$j\omega_0 L_s + R_s = [(j\omega_0 L_p) \| R_p] = \frac{(\omega_0 L_p)^2 R_p + j\omega_0 L_p R_p^2}{R_p^2 + (\omega_0 L_p)^2}$$

if are equal and $Q = R_p / \omega_0 L_p = \omega_0 L_s / R_s$

$$R_p = R_s (Q^2 + 1)$$

equating imaginary

$$L_p = L_s \left(\frac{Q^2+1}{Q^2} \right)$$

III rd eqn for computing series and Parallel Rc equivalents:

$$R_p = R_s (Q^2 + 1)$$

$$C_p = C_s \left(\frac{Q^2}{Q^2+1} \right)$$

$$R_p = R_s (Q^2 + 1)$$

$$X_p = X_s \left(\frac{Q^2+1}{Q^2} \right)$$

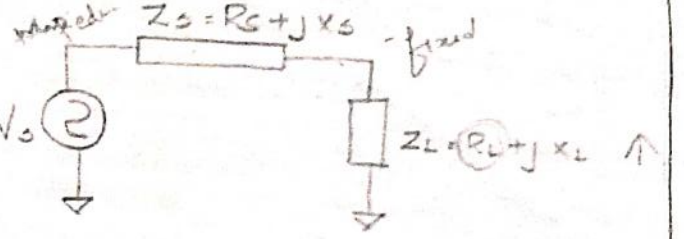
This way, one need to remember a single pair of "summed formulas in order to convert impure RLC network to pure parallel / series.

RLC NETWORK AS IMPEDENCE TRANSFORMER

Circuit design at low frequency usually proceed in ignorance of the Max power transfer theorem derived.

THE MAXIMUM POWER TRANSFER THEOREM

We will consider the below Example



Z_s - fixed source impedance, Z_L - maximize the power delivered to the load?

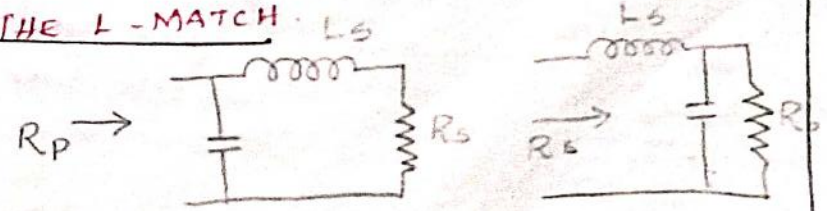
The power delivered to the load impedance is entirely due to R_L, as reactive elements do not dissipate power and power is simply delivered.

$$\frac{|V_R|^2}{R_L} = \frac{R_L [V_s]^2}{(R_L + R_s)^2 + (X_L + X_s)^2}$$

To maximize the power delivered to R_L ie X_L and X_s should be smaller and their to zero. and hence the maximum Power transfer from a fixed source impedance to load occurs when the load and source impedance are complex conjugate

For practical methods to achieve maximum power transfer by:

THE L-MATCH



R_s is load resistance, when this resistor is viewed across capacitor. It is transformed to equivalent.

This is called L-match, because of its shape and simplicity as there are only two degree of freedom. (i) impedence transformation ratio and resonant frequency, and Q is found.

$$R_p \simeq R_s Q^2 = R_s \left(\frac{1}{\omega_0 R_s C}\right)^2 = \frac{1}{R_s}\frac{L_s}{C}$$

$$R_p R_s \simeq \frac{L_s}{C} = Z_0^2.$$

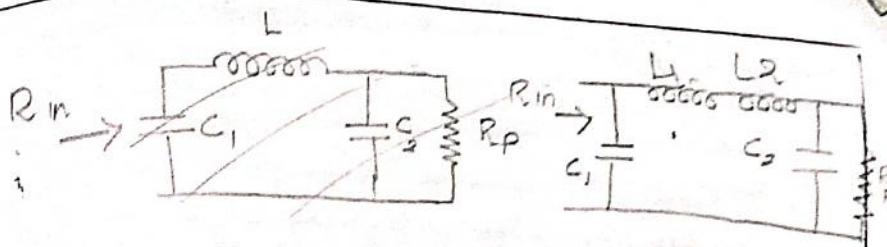
Q is approximately the square root of the transformation ratio is given by

$$Q = \sqrt{\frac{R_P}{R_s}}$$

As long as $Q > 3$ or 4, the error will be under 10%. and $Q > 10$, the max error will be 1% or 5%.

THE PI-MATCH.

Limitation of L match is one can specify two of center frequency, impedence transformation ratio and Q. To acquire third degree of freedom, the pi-match and called because of its shape. Here the load resistance R_p is transformed to a lower resistance known as image or intermediate resistance.



Q in right network $= \frac{\omega_0 L_2}{R_1}$

$$= \sqrt{\frac{R_P}{R_1} - 1}$$

$$= Q_{right}$$

Q in left network $= \frac{\omega_0 (L_1 + L_2)}{R_1}$

$$= \sqrt{\frac{R_{in}}{R_1} - 1} + \sqrt{\frac{R_P}{R_1} - 1}$$

The above eqn allows us to find image resistance, one R is computed the total inductance is found

$$L_1 + L_2 = \frac{Q R_1}{\omega_0}$$

The capacitance

$$C_1 = \frac{Q_{left}}{\omega_0 R_{in}}.$$

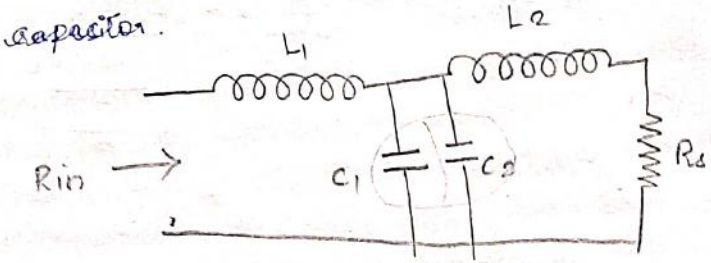
$$C_2 = \frac{Q_{right}}{\omega_0 R_P}$$

$$R_1 = \frac{\left(\sqrt{R_{in}} + \sqrt{R_P}\right)^2}{Q^2}$$

THE T-MATCH

Practical implementation

In this single capacitor is decomposed into two equal one. The Parallel image resistance is seen across the capacitor.



The net Q is

$$Q = \omega_0 R_{in}(C_1+C_2)$$

image resistance

$$= \sqrt{\frac{R_{in}}{R_{in}} - 1} + \sqrt{\frac{R_{in}}{R_s} - 1}.$$

From which image resistance

$$C_1 + C_2 = \frac{Q}{\omega_0 R_{in}}$$

$$L_1 = \frac{Q_{left} R_{in}}{\omega_0}$$

$$L_2 = \frac{Q_{right} R_{in}}{\omega_0}$$

T match is particularly useful when source and termination parasitic are inductive nature.

IMPEDENCE MATCHING NETWORKS

Impedence Z is a measure of opposition to electrical flow. It is measured in ohms.

For DC System, the impedence and resistance are same

In AC system, the reactance enters the equation due to frequency dependent capacitor and inductor.

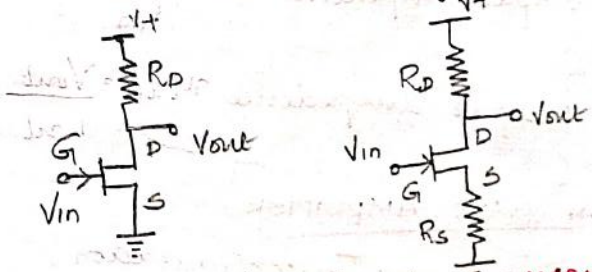
$$Z = \sqrt{R^2 + (X_L - X_C)^2}$$

↓ Resistance + inductive reactance. ↓ capacitive reactance.

Impedence matching is designing source and load impedence to minimize signal reflection or maximize power transfer.

In DC, the source and load should be equal

In AC, the source should either be equal to the load or complex conjugate of the load.



AMPLIFIERS: COMMON SOURCE, COMMON GATE

In common source configuration.

* The FET exhibits high input impedance, high gain, potential instability and low noise figure.
* high source and load impedence are required by the device for high gain.

This amplifier can work as either
* Transconductance amplifier
* Voltage amplifier.

If amplifier works as transconductance then, the input signals are amplified and modulated the current flowing to the load.

* If amplifier working as voltage amplifier the input signal is amplified and modulates the current passing through the FET and changes the voltage across the load resistor according to ohm's law

Current gain $A_i = \frac{i_{out}}{i_{in}}$

Voltage gain $AV = \frac{V_{out}}{V_{in}}$.

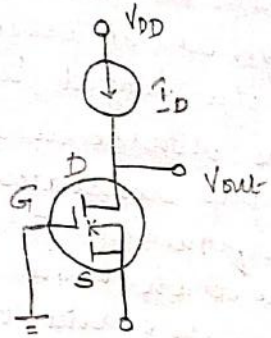
Input impedence $r_{in} = \frac{v_{in}}{i_{in}}$.

Output impedence $r_{out} = \frac{V_{out}}{i_{out}}$.

COMMON GATE AMPLIFIER

In common gate configuration.

The FET generally exhibits high gain, high output impedence, low input impedence unconditional stability and noise performance comparable to that of the common source mode.



This configuration is used less often than the common source or common follower. However, it can be combined with common source amplifier to create cascode configuration it is used in CMOS RF receiver when operating near the frequency limitations of FETs due to desirable impedence matching and potentially has lower noise.

short circuit current gain $A_i = \left.\frac{i_{out}}{i_s}\right|_{R_L=0}$

open circuit voltage gain $AV = \left.\frac{V_{out}}{V_s}\right|_{R_L=\infty}$

Input resistance $R_{in} = \frac{V_s}{i_s}$

output resistance $R_{out} = \frac{V_x}{i_x}$

A common-gate amplifier is one of three basic single stage field-effect transistor (FET) amplifier as current buffer or voltage amplifier.

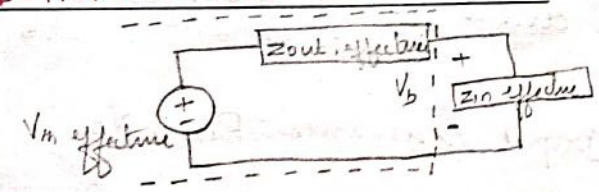
The common source and common drain configurations have high input resistance because the gate is the input terminal. In common gate, the source is input terminal has low input resistance. Common Gate FET configuration provides low input impedence with high voltage gain, current gain is low and net all power gain is low.

common gate amplifier, often used in high frequency application and has much larger bandwidth.

common gate amplifier provides a power gain for the signal amplifier.

The common gate Amplifier is used less often than the common source or source follower.

OC TIME CONSTANT IN BANDWIDTH ESTIMATION AND ENHANCEMENT:

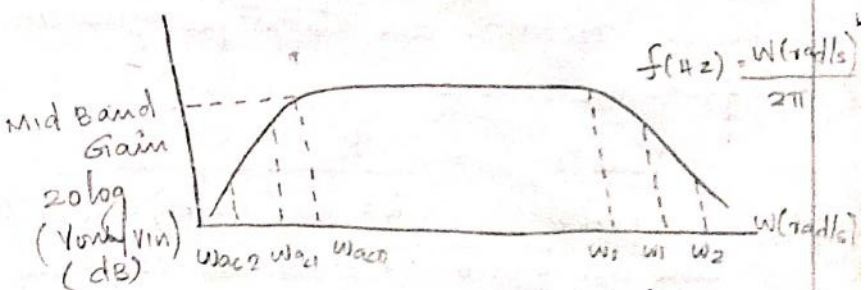


Two port analysis allows us to quickly calculate small signal gain from cascaded network stages

when complex impedences are considered (ie: resistor, inductor and resistor).

* complex impedence calculations are time consuming.

* Capacitance between drain and gate transistor complicates calculation effort further



* Mid Band gain can be calculated by assuming purely resistive impedence
* large valued capacitor used for AC coupling will be shorts in this analysis.
* For Dc coupled circuits, typically DC gain = Mid gain.
* Small valued capacitor will be open in this analysis.
* we are interested in knowing the bandwidth

Bandwidth is primarily set by the lowest frequency pole wo

* Additional attenuation occurs at frequencies beyond the amplifier bandwidth by higher frequency poles w1, w2 etc
* Open circuit time constant (OCT) technique allow to estimate bandwidth of amplifier circuit.

This means that W_1, W_2 and higher poles are not close in frequency to W_0.

let us assume the transfer function from V_{in} to V_{out}

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{K}{(T_0 s+1)(T_1 s+1)\cdots(T_{n-1}s+1)}$$

we are ignoring any ac coupling poles and zeros.

which means DC gain = Midband gain. which is required to simplify the analysis.

DC gain equals k in as $s=0$

The OCT approximates the Transfer function as

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{K}{\left(\sum_{i=0}^{n-1} T_i\right)s+1}.$$

The estimated bandwidth is found by substituting $s=j\omega_0$ and solving for ω_0 such that magnitude is $K/\sqrt{2}$.

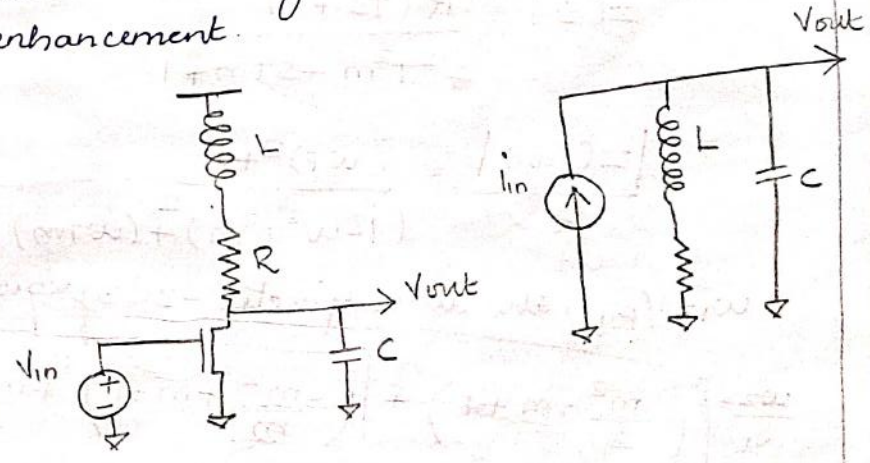
$$\omega_0 = \frac{1}{\sum_{i=0}^{n-1} T_i} \Rightarrow \left|\frac{V_{out}(\omega_0)}{V_{in}(\omega_0)}\right| = \left|\frac{K}{j1+1}\right| = K/\sqrt{2}.$$

HIGH FREQUENCY AMPLIFIER DESIGN.

* The design of amplifiers at high frequency demands more effort in reaching the performance when approaching the inherit limitations of the device
* The effect of parasitic capacitances and inductances can impose serious constraints on performance
* A collection of useful bandwidth extension techniques shall be introduced.

The shunt peaked Amplifier.

A standard common source Amplifier with addition of induction provides bandwidth enhancement.



Qualitative analysis.

- frequency domain. introducing a 'zero'
- Time domain ; step response.

The impedance of RLC network

$$z(s) = (sL+R) \| \frac{1}{sC} = \frac{R\left[s\left(L/R\right)+1\right]}{s^2LC+sRC+1}$$

$$|z(j\omega)| = R\,\frac{(\omega L/R)^2+1}{(1-\omega^2LC)^2+(\omega RC)^2}$$

* $\omega L/R^2$ increases as ω increases
$(1-\omega^2LC)^2$ decreases as ω increases.

Design and procedure

Given R and C, determine L

Introducing $m = RC/L/R = RC/\tau$ where

$\tau = L/R$

$$z(s) = \frac{R(\tau s+1)}{s^2\tau^2 m + s\tau m + 1}$$

$$\frac{|z(j\omega)|}{R} = \frac{(\omega\tau)^2+1}{(1-\omega^2\tau^2 m)^2+(\omega\tau m)^2}$$

$\omega_1 = 1/R_1$, the uncompensated -3dB frequency

$$\frac{\omega_2}{\omega_1} = \sqrt{\left(-\frac{m^2}{2}+m+1\right)+\sqrt{\left(-\frac{m^2}{2}+m+1\right)^2+m^2}}$$

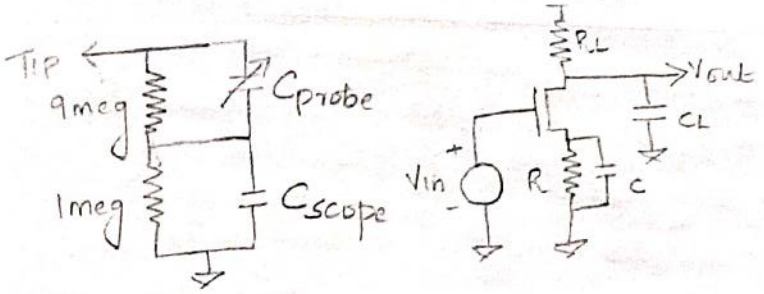
To max bandwidth set $d\omega_2/dm = 0$.

$$m = \sqrt{2} \simeq 1.41$$

$$\omega_{2,max} = 1.85\omega_1$$

m leads to 20% peak in frequency

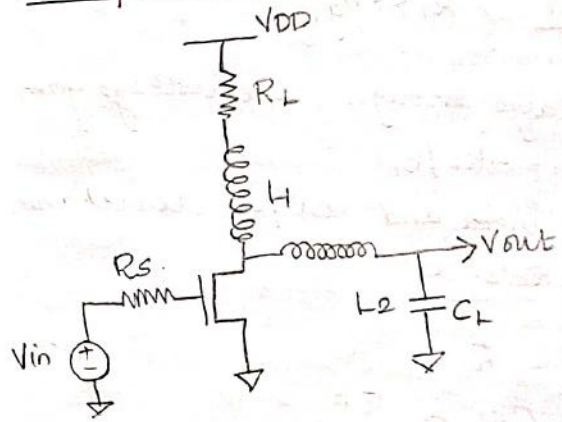
Zeros as Bandwidth Enhancers



Pole zero doublet:

$$H(s) = \frac{\alpha\tau s+1}{\tau s+1}$$

Two port Bandwidth Enhancement.



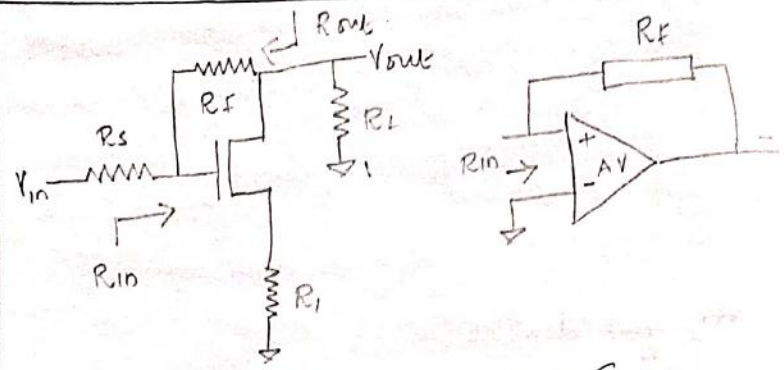
series peacking only without H.

- maximum $\omega_2 = \sqrt{2}\omega_1$, smaller than shunt peaking provided by complex poles

$m = R^2C/L_2 = 2$.

$m = 3$: maximally flat group delay, $\omega_2 = 1.36\omega_1$

The Shunt Series Amplifier



Effective gain $g_{m,eff}$ or G_m

$$G_m = \frac{i_d}{V_{in}} = \frac{g_m}{1+g_m R_1}$$

$$\simeq \frac{1}{R_1} \quad \text{if } R_1 >> 1/g_m$$

Assume R_F large enough, the voltage gain

$$A_0 = -R_L/R_1.$$

R_F reduces both input and output resistance through shunt feedback.

Input resistance R_{in}

$$R_{in} = \frac{R_F}{1-A_V} \simeq \frac{R_F}{1+R_L/R_1}$$

output resistance R_{out}

$$R_{out} = \frac{R_F+R_s}{1+R_s/R_1} \simeq \frac{R_F}{1+R_s/R_1}$$

if $R_L = R_s = R$

$$R_{in} \simeq R_{out} \simeq \frac{R_F}{1+R/R_1} \simeq \frac{R_F}{1-A_V}.$$

Gain and input - output Impedance of Shunt series Amplifier.

Gate to drain gain.

$$V_{out} = -g_{m\,eff} V_{test} \frac{R_F R_L}{R_F+R_L} + V_{test} \frac{R_L}{R_F+R_L}$$

$$A_V = \frac{V_{out}}{V_{test}} = -\frac{R_L}{R_1} \cdot \left[\frac{1}{1+1/g_m R_1}\right] \cdot \left[\frac{1}{1+R_L/R_F}\right] \cdot \left[1 - \frac{1}{g_{m,eff} R_F}\right]$$

$$A_V = -\frac{R_L}{R_E}\left[\frac{R_F - R_E}{R_F+R_E}\right]$$

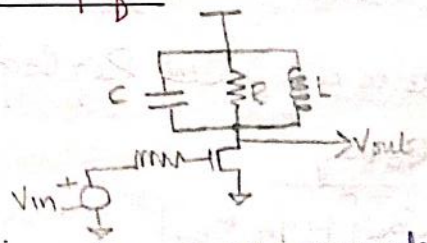
Input Resistance.

$$R_{in} = \frac{R_F}{1-A_V} = \frac{R_E(R_F+R_L)}{R_E+R_L}.$$

output Resistance.

$$R_{out} = \frac{R_E(R_F+R_s)}{R_E+R_s}$$

Tuned Amplifier



- Driving from a zero impedence source with neglect the series gate resistance. Then, C_{gd} can be absorbed into C.

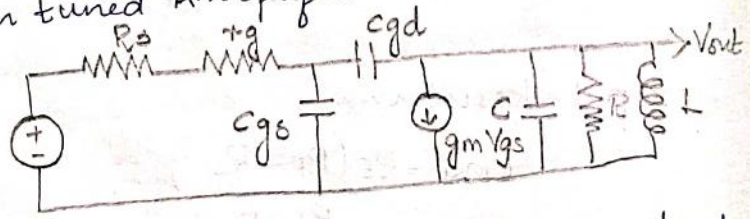
The circuit is thus an ideal transconductor driving an RLC tank

* At the resonant frequency, the gain is $g_m R$.
* The total -3 dB bandwidth is $1/RC$
* The product of gain and bandwidth is

$$G.BW = g_m R \cdot \frac{1}{RC} = \frac{g_m}{C}.$$

which is independent of center frequency.

* The key is the cancellation of the load capacitance by the inductor in tuned Amplifier



Admittance seen to the left of RLC tank (y_{out})

The result is a parallel R_{eq} C_{eq}

$$R_{eq} = R_s + r_g$$

$$C_{eq} = C_{gd}[1 + g_m R_{eq}]$$

$$= C_{gd}[1 + g_m(R_s + r_g)]$$

This is the alternative manifest of miller Viewed from output port.

The components in the responsive current

* Resistive
* Capacitive

Admittance seen to the right of C_{gs}

$$y_{in} = \frac{y_L + y_F}{y_L + y_F} + \frac{g_m y_F}{y_L + y_F}$$

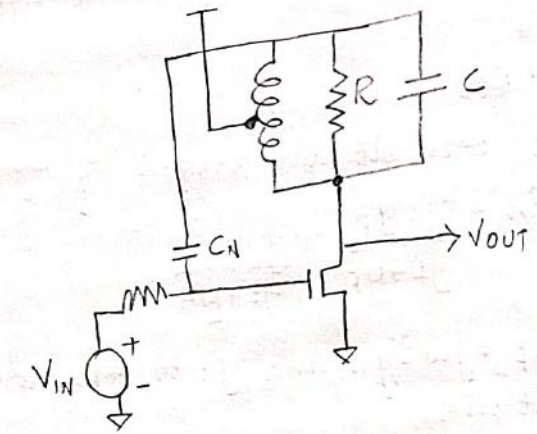
where $y_F = j\omega C_{gd}$ and y_L is the admittance of RLC tank

$$y_{in} \simeq y_F + \frac{g_m(j\omega C_{gd})}{y_L}.$$

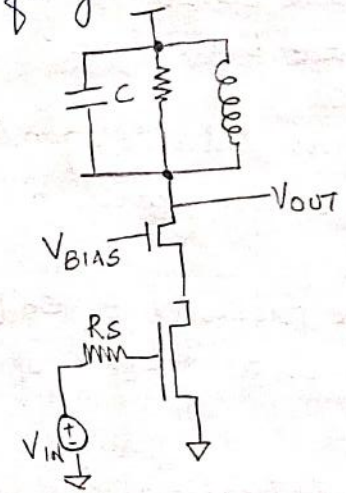
* y_L has a net negative imaginary part at frequency where the tank look inductive
* 2nd term on RHS of the above equation can have a negative resistance when connected to it.
* All are caused by the presence of C_{gd} which may be as much as 30-50% of main gate capacitance

Neutralization and unilateralization

Neutralization: Cannot be done precisely for C_{gd} is voltage-dependent.



unilateralization and source-coupled version of cascode amplifier trade off for given total current and headroom



CASCADED AMPLIFIER.

* How many amplifier stages to use to achieve a certain gain?
* Given a BW for each stage, what is BW of overall amplifier.
* Any optimum number of stages to maximize the overall BW?

* Bandwidth Shrinkage

Assumption : Each stage has a unit DC gain and a single pole.

$$H(s) = \frac{1}{\tau s + 1}$$

A cascade of n such amplifier

$$A(s) = \left(\frac{1}{(\tau s+1)}\right)^n$$

$$|A(j\omega)| = \left|\frac{1}{j\omega\tau + 1}\right|^n = \frac{1}{\sqrt{2}}$$

so that

$$\left(\frac{1}{\sqrt{(\omega\tau)^2+1}}\right)^n = \frac{1}{\sqrt{2}}$$

The band width is

$$\omega = \frac{1}{\tau}\sqrt{2^{1/n}-1}.$$

As n approaches infinity, the overall bandwidth tends towards zero to make physics make clear

$$2^{1/n} = \exp\left[\ln\left(2^{1/n}\right)\right] = \exp\left(\frac{1}{n}\ln 2\right)$$

for large n,

$$\exp\left(\frac{1}{n}\ln 2\right) \simeq 1 + \frac{1}{n}\ln 2$$

Thus $$\omega = \frac{1}{\tau}\sqrt{2^{1/n}-1} \simeq \frac{1}{\tau}\sqrt{\frac{1}{n}\ln 2} \simeq \frac{0.833}{\tau\sqrt{n}}.$$

The error for n=1 is 17% and 28%, 36% drops pretty fast as n increases. The open circuit time constant method would predict the bandwidth goes directly as 1/n, while in fact it goes as the reciprocal square root.

* optimum gain per stage.

Assuming each stage is identical and width constant gain-bandwidth Product. The goal is to find the number of stages that, for given overall gain requirement, maximizing the bandwidth.

over all gain G, meaning $G_{ss} = G^{1/n}$

Gain-bandwidth product for each stage : ω_T

$$BW_{ss} = \frac{\omega_T}{G^{1/n}}$$

The bandwidth for the total Amplifier

$$BW_{tot} \simeq \frac{\omega_T \sqrt{\ln 2}}{G^{1/n}\sqrt{n}}$$

or $$\frac{1}{BW_{tot}} \simeq \frac{1}{\omega_T \sqrt{\ln 2}} (\sqrt{n}\, G^{1/n}).$$

The maximum total bandwidth is achieved when

$$\frac{d}{dn}(\sqrt{n}\, G^{1/n}) = 0$$

which yields.

$$\ln(G^{1/n}) = \frac{1}{2} \Rightarrow G^{1/n} = e^{1/2} = 1.619$$

The number of stages corresponding to this optimum is

$$n = 2 \ln G$$

The overall bandwidth in this case is

$$BW_{tot} = \omega_1 \sqrt{\frac{\ln 2}{2e \ln G}} \simeq \frac{0.357}{\sqrt{\ln G}} \omega_T$$

It can be seen when n is chosen optimally (knowing G), the product of the bandwidth and the square root of the log of the gain is a constant. The overall bandwidth is relatively insensitive to the value of overall gain.

---

* A Voltage step applied to input.
* The input propagates down the input line causing a step to appear at each transistor in succession.
* Each transistor generates a current (g_m V step)
* ultimately all the transistor output current are summed in time coherence

over all gain $A_V = \frac{n g_m z_0}{9}$

This amplifier has overall gain that depends linearly on the number of stages. Thus each stage can operate at frequencies where the gain is smaller than unity.

- can operate at substantially higher frequencies than conventional amplifier
- since delay is proportional to the number of stages, it trades gain for delay, not bandwidth.
- Transistor input/output capacitances are absorbed by delay line.
- Each stage can have gain smaller than unity, hence higher BW.
- power hungry.

Low Noise Amplifier

The first stage of receiver is typically a LNA, whose main function is to provide enough gain to overcome the noise of subsequent stages (Friis).

In principle, one can obtain minimum noise figure from a given device using optimum source impedance defined by 4 noise parameter G_c, B_c, R_n and G_u. This classical method faces power consumption.

To develop design strategy that balances gain, input impedance, noise figure, power consumption, we will derive analytical expression for 4 noise parameters directly from the device noise model.

Derivation of intrinsic mosfet Two port noise parameters

MOSFET noise model consist of two sources.

(i) mean square drain current noise

$$\overline{i^2_{nd}} = 4kT\gamma g_{do}\Delta f$$

(ii) gate current noise

$$\overline{i^2_{ng}} = 4kT\delta g_g \Delta f$$

$$g_g = \frac{\omega^2 C^2_{gs}}{5 g_{do}}$$

further gate noise is correlated with drain noise by correlation coefficient

$$C = \frac{\overline{i_{ng} \cdot i^*_{nd}}}{\sqrt{\overline{i^2_{ng}} \cdot \overline{i^2_{nd}}}}$$

where reference direction for gate noise is from source to gate.

drain source is from drain to source

In long channel the value of c (theoretically - j0.395).

Assumptions

* c is constant at its long channel
* Value and thermal noise due to resistive gate material will be neglected
* C_{gd} also be neglected

To derive the 4 equivalent 2-port noise parameters

$$R_n \equiv \frac{\overline{e_n^2}}{4KT\Delta f}$$

$$G_U \equiv \frac{\overline{i_u^2}}{4KT\Delta f}.$$

$$Y_c = \frac{i_c}{e_n} = G_c + jB_c$$

To find input noise voltage

$$\overline{e_n^2} = \frac{\overline{i_{nd}^2}}{g_m^2} = \frac{4KT\gamma g_{do}\Delta f}{g_m^2}.$$

This input noise voltage is correlated and in phase with drain current noise.

$$R_n \equiv \frac{\overline{e_n^2}}{4KT\Delta f} = \frac{\gamma g_{do}}{g_m^2}.$$

under open circuit condition dividing drain current noise by transconductance yields an equivalent i/p voltage, which when multiplied by input admittance yield equivalent input current noise and modeling of ind:

$$\overline{i_{n1}^2} = \frac{\overline{i_{nd}^2}(j\omega C_{gs})^2}{g_m^2} = \frac{4KT\gamma g_{do}\Delta f(j\omega C_{gs})^2}{g_m^2}$$

$$= \overline{e_n^2}(j\omega C_{gs})^2$$

we have assumed that input admittance of MOSFET is purely capacitive which is good for frequency below ω_T.

The total equivalent input current noise is the sum of reflected drain noise and the induced gate current noise.

The induced gate noise current of 2 terms

(i) i_{ngc} → fully correlated with drain current noise

(ii) i_{ngu} → uncorrelated with drain current noise.

The correlation admittance is

$$Y_c = \frac{i_{n1} + i_{ngc}}{e_n} = j\omega C_{gs} + \frac{i_{ngc}}{e_n}$$

$$= j\omega C_{gs} + \frac{g_m}{i_{nd}} \cdot i_{ngc} = j\omega C_{gs} + g_m \cdot \frac{i_{ngc}}{i_{nd}}$$

To express Y_c in more useful form. i.e. we express in terms of cross-correlation by multiplying both numerator and denominator by conjugate of drain noise current.

$$g_m \cdot \frac{\overline{i_{ng} c}}{i_{nd}} = g_m \cdot \frac{\overline{i_{ng} c \cdot i_{nd}^*}}{\overline{i_{nd} \cdot i_{nd}^*}}$$

$$= g_m \cdot \frac{\overline{i_{ng} c \cdot i_{nd}^*}}{\overline{i_{nd}^2}}$$

$$= g_m \cdot \frac{\overline{i_{ng} \cdot i_{nd}^*}}{\overline{i_{nd}^2}}$$

The last equality i_{ng} is replaced by i_{ngc}

$$Y_c = j\omega C_{gs} + g_m \cdot \frac{\overline{i_{ng} \cdot i_{nd}^*}}{\overline{i_{nd}^2}}$$

$$= j\omega C_{gs} + g_m \cdot \frac{\overline{i_{ng} \cdot i_{nd}^*}}{\sqrt{\overline{i_{nd}^2}}\sqrt{\overline{i_{nd}^2}}} \sqrt{\frac{\overline{i_{ng}^2}}{\overline{i_{ng}^2}}}$$

$$Y_c = j\omega C_{gs} + g_m \cdot \frac{\overline{i_{ng} \cdot i_{nd}^*}}{\sqrt{\overline{i_{ng}^2} \cdot \overline{i_{nd}^2}}} \sqrt{\frac{\overline{i_{ng}^2}}{\overline{i_{nd}^2}}}$$

$$= j\omega C_{gs} + g_m \cdot c \sqrt{\frac{\overline{i_{ng}^2}}{\overline{i_{nd}^2}}}$$

Substitute for radical terms.

$$Y_c = j\omega C_{gs} + g_m \cdot c \sqrt{\frac{\delta \omega^2 C_{gs}^2}{5 \gamma g_{do}^2}}$$

$$= j\omega C_{gs} + \frac{g_m}{g_{do}} \cdot c \sqrt{\frac{\delta}{5\gamma}} \cdot \omega C_{gs}$$

c is purely imaginary.

$$Y_c = j\omega C_{gs} - j\omega C_{gs} \frac{g_m}{g_{do}} \cdot |c| \sqrt{\frac{\delta}{5\gamma}}$$

$$= j\omega C_{gs} \left(1 - \alpha |c| \sqrt{\frac{\delta}{5\gamma}}\right)$$

where $\alpha = \frac{g_m}{g_{do}}$ and unity for long channel devices.

Further noise

$$\overline{i_{ng}^2} = \overline{(i_{ngc} + i_{ngu})^2} = 4KT\Delta f \delta g_g |c|^2 + 4KT\Delta f \delta g_g (1 - |c|^2).$$

uncorrelated of gate noise current

$$G_u \equiv \frac{\overline{i_u^2}}{4KT\Delta f} = \frac{4KT\Delta f \delta g_g (1 - |c|^2)}{4KT\Delta f} = \frac{\delta \omega^2 C_{gs}^2 (1 - |c|^2)}{5 g_{do}}$$

$$B_{opt} = -B_c = -\omega C_{gs} \left(1 - \alpha |c| \sqrt{\frac{\delta}{5\gamma}}\right).$$

(optimum source susceptance).

$$G_{opt} = \sqrt{\frac{G_u}{R_n} + G_c^2} = \omega C_{gs} \sqrt{\frac{\delta}{5\alpha}(1-|c|^2)}$$

(optimum source admittance)

The minimum noise figure is given by.

$$F_{min} = 1 + 2R_n [G_{opt} + G_c) \simeq$$

$$1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\alpha \delta (1-|c|^2)}.$$

* if there is no gate current noise, the minimum noise figure would be 0 dB.

* The improvement in ω_T that accompany technology scaling improve noise figure at any given frequency.

The noise parameter for a device of width W are

$$G_c = \frac{W_0}{W} G_{co}$$

$$B_c = \frac{W}{W_0} B_{co}$$

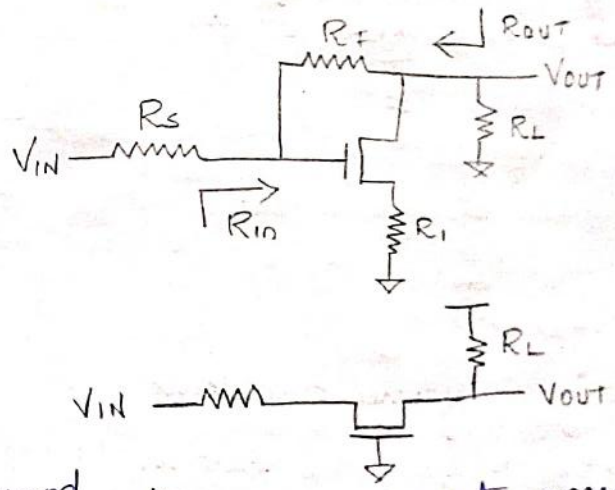
$$G_u = \frac{W}{W_0} G_{uo}$$

$$R_n = \frac{W_0}{W} R_{no}$$

The subscript 0 identifies to unit device of width W_0. The noise factor F is a dimension less quantity and therefore independent of width.

POWER MATCH VERSUS NOISE MATCH

* The input impedence of MOSFET is inherently capacitive, so providing a good match to a 50 Ω source without degrading noise performance would be difficult.



broadband 50 Ω input 50 Ω resistor across the input terminal of common-source amplifier

Resistor R_1 adds thermal noise of own The combination of these two effects produces high noise figure.

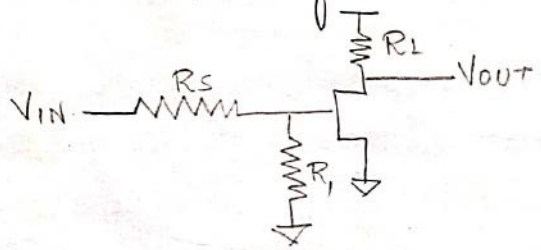
$$F \geq 2 + \frac{4}{\alpha}\gamma \cdot \frac{1}{g_m R}$$

where $R_S = R_1 = R$

This bound applies in low frequency limit and ignores gate current noise.

The shunt series amplifier.

Provides a broad band real input impedance. since it not reduce the signal with a noisy attenuator before amplifier as NF better that of circuit as.



Disadvantages.

Suffers from former problems yet resistive feedback generate thermal noise on its own and fails to present transistor an impedance that equals z_{opt} at all frequencies as a result, overall amplifier noise figure, usually better of above circuit exceeds the device F_{min} by considerable amount.

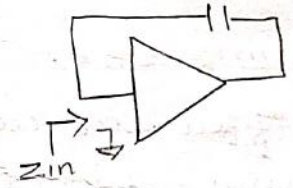
This circuit is used in many application even though its noise figure is not minimum possible.

Another method is for realizing a resistive input impedance is to use a common gate configuration. The resistance looking into source is $1/g_m$, a proper selection of device size and bias current can provide desired 50-Ω resistance.

with circuit it is straight to establish lower bound on noise figure of CG Amplifier

$$F \geq 1 + \gamma/\alpha.$$

All three topologies suffer noise figure degradation from presence of noisy resistance in signal path. which is rectified by



impedance transformation model.

This amplifier is ideal except for frequency dependent of gain $A(s)$. The input terminal is analogous to the gate terminal and amplifier is connected

to bottom plate of gate capacitance. The input impedance is

$$Z_{in} = \frac{1}{sC[1+A(s)]}$$

A(s) have gain and phase shift.

$$A(s) = A_0 e^{-j\phi}$$

then

$$Z_{in} = \frac{1}{j\omega C[1+A_0 e^{-j\phi}]} = \frac{1}{j\omega C[1+A_0(\cos\phi - j\sin\phi)]}$$

$$Y_{in} = j\omega C[1+A_0\cos\phi] + A_0\omega C\sin\phi.$$

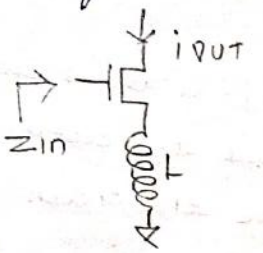
* Phase lag grows with frequency and ↑ with square of frequency to a good approximation.

* Transit time effects also cause a resistive component of input impedance.

* To enhance this effect we will create a resistive input impedance without noise of real resistor.

* A better method to employ inductive source degeneration [current lags behind gate voltage and advantage it control over real part of impedance

of inductance from computing input resistance of circuit



For simple analysis a device model with transconductance and gate source capacitance is considered.

$$Z_{in} = sL + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}}L \simeq sL + \frac{1}{sC_{gs}} + \omega_T L$$

The input impedance of RLC N/w with resistive term is ∝ to inductive value.

The source degeneration impedance z is modified by factor equal to $[B(j\omega)+1]$.

where $B(j\omega) = \frac{\omega_T}{j\omega}$.

current gain magnitude goes to unity at ω_T and capacitive phase angle due to C_{gs}.

$$Z_{in}(j\omega) = \frac{1}{j\omega C_{gs}} + [B(j\omega)+1]z$$

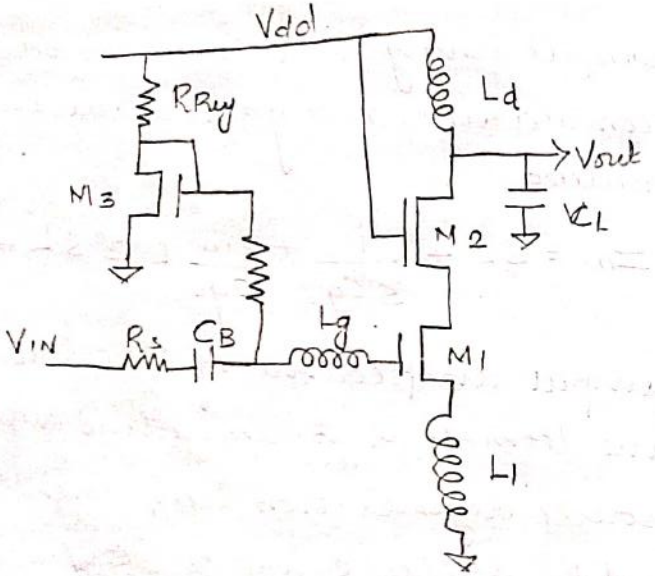
$$= \frac{1}{j\omega C_{gs}} + z + \left[\frac{\omega_T}{j\omega}\right]z.$$

The capacitive degeneration causes negative resistance to the input impedance.

SINGLE ENDED AND DIFFERNTIAL LNA

SINGLE ENDED

For narrowband applications it is advantageous to tune out the output capacitance to increase the gain.



* Cascoding transistor M_2 is used to reduce the interaction of tuned output with the tuned input and reduce the effect of M_1's C_{gd}.
* The total node capacitance at drain of M_2 resonate with inductance L_d both to increase gain at center frequency and provide desired Band pass filtering.
* The input and output resonance are set equal to each other. if vary from each other flatter and broader response is obtained.
* Transistor M_3 is form a current mirror with M_1 and its width is some small fractions of M_1's width to minimize the power overhead of bias circuit
* current through M_3 is set by the supply voltage and Ref in conjunction with V_{gs} of M_3
* The resistor R_{BIAS} is chosen large so that more current is small and ignored.
* TO complete DC blocking, capacitor C_B to prevent upsetting the gate to source bias of M_1. The value of C_B is chosen to have a negligible reactance at signal frequency

To determine component value and device size.

Assuming
(i) operation at 10 Gbps, resistance - 50Ω
(iii) 5-mA bias current for M_1, for 0.5 μm technology. Leff - 0.35 μm and C_{ox} - 3.8 mF/m^2

from this we calculate
(i) Optimum width of main input M_1 transistor ≃ 500 μm at bias current of 5 mA, W_T is 35 Gbps, α - 0.85

To find degeneration inductance

To generate real part of 50 Ω, L_S must be 11nH

C_{gs} must be known ≈ 0.5 pF.

For degenerating this capacitance at 10 GHz

The finished LNA, the bias transistor width and current are arbitrarily chosen as 1/10th of main transistor.

The resistive component at i/p is given by

$$Re[Z_{in}] = \frac{\omega T L_S}{1 + 2C_{gd}/C_{gs}}$$

The degenerating inductance must increase be increased to compensate.

The drain noise component whose value is given by

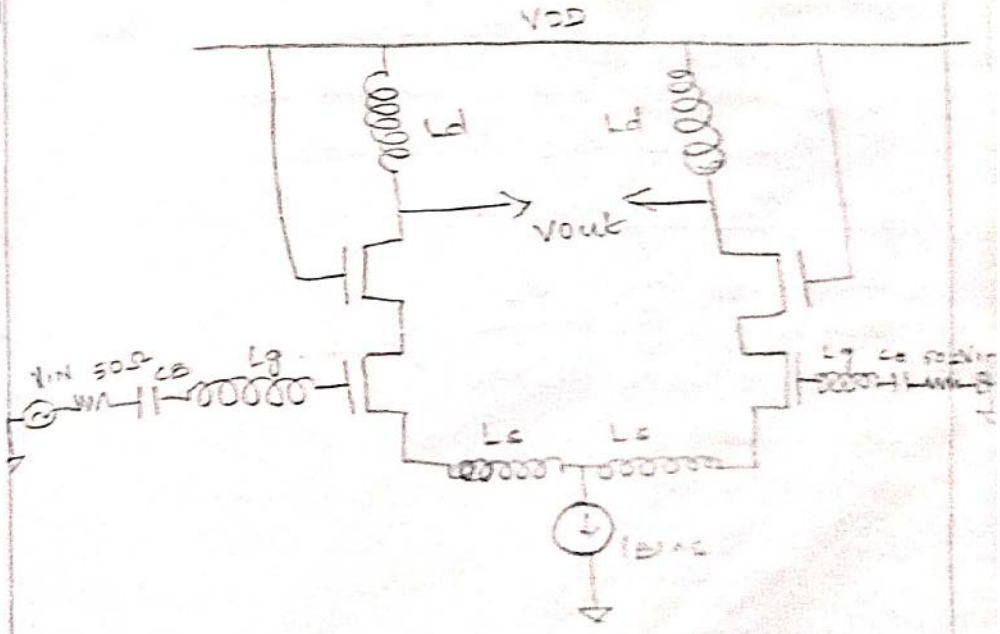
$$\overline{I_{nd,sub}} = \frac{4KTR_{sub}g_{mb}^2}{1 + (\omega R_{sub} C_{sb})^2} \Delta f.$$

* For frequencies below pole frequency of $1/R_{sub} C_{sb}$, this extrinsic noise contribution remain negligible

$$R_{sub} \leq 2R_s.$$

DIFFERENTIAL LNA

* The disadvantage of single ended LNA is its sensitivity to parasitic ground inductance
* The ground return of signal source is supposed to be at same potential as the bottom source of degenerating inductor, there is difference in these potential because there is non-zero impedance between the two points.
* Alternative method is to increment ground located at symmetrical part of a differential structure by parasitic resistance in series with an impedance a still source current



* Another attribute, its ability to reject common mode disturbances

* The noise figure in this amplifier is higher than its single ended counter part

* The power consumed is twice as single ended amplifier to achieve the same noise figure and the disadvantage is the improved linearity that attends during the input voltage between two devices.

* The operational amplifier compares this voltage with the common-mode drain voltage of input pair and drives the gate of cascoding transistor to make the two voltages

$$V_{d1,2} = \frac{R_4}{R_3+R_4} V_{gs1,2}.$$

UNIT - III

FEEDBACK SYSTEMS AND POWER AMPLIFIERS

Feedback systems: stability of feedback Systems - Gain and phase margin, Root-locus Techniques, Time and frequency domain Considerations, compensations, - Power Amplifiers: General model - Class A, AB, B, C, D E and F Amplifiers - Linearization Techniques - Efficiency boosting Techniques - ACPR metric.

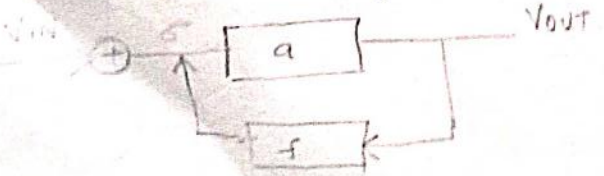
FEEDBACK SYSTEMS:

History of modern Feedback.

* Application of feedback concepts is very ancient.
* The first concious applications of feedback Principles in electronic was by Rocket pioneer Robert Goddar in 1912, a vaccum tube oscillator that employes positive feedback

ARMSTRONG AND ATID THE REGENERATIVE AMPLIFIERS:

This Paper on Vaccum tube by Armstrong in 1915 explains how positive feedback (regeneration could be used to greatly increase the voltage gain.



where a is forward gain, f is feedback gain, a, represents the gain of ordinary (open loop) f - represents the fraction of o/p voltage is fed back to the amplifier input

Overall gain of this amplifier

$$\sigma = V_{in} + f \cdot V_{out}$$

$$V_{out} = a * \sigma = a (V_{in} + f \cdot V_{out})$$

Solving for input and output transfer function $A = \frac{a}{1 - af}$

Any positive value of af, small than unity gives us an overall gain A, that exceeds a, the ordinary gain of Vaccum tube amplifier.

If af = 0.9, the overall gain is increased ten times of a,

If af is product of 0.99 where a is 100 fold time gain increases.

In this way, he was able to obtain gain from single stage, which other could obtain by cascading. which allowed the construction of relatively in expensive, high gain receivers and enabled reduction in transmitter power because of enhanced sensitivity provided by the increased gain.

HAROLD BLACK AND THE FEEDFORWARD AMPLIFIER.

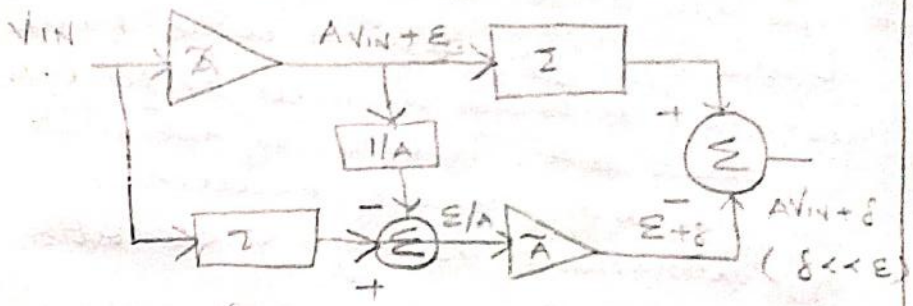
* Although Armstrong's regenerative amplifier solve the problem of obtaining large gain from vaccum tube amplifier,
* A different problem in telephone industry occupied, (ie) when trying to extend long distance communication, the amplifiers needed to compensate for transmission lines attenuation. Amplifiers available those days could achieve around 1000-2000 miles but the quality was poor.

After long work, a crude transcontinental telephone service was found in 1915 by Alexander Graham Bell at 68 yrs.

The problem was just not insufficient amplification, but was distortion. Each amplifier contributed 1% of distortion and in cascading that (o/p) did not match the input.

* Let 'small signal' operation was opted but it was quite inefficient as it required the construction of say 100-W amplifiers for processing of milliwatt signals.
* And in 192, Harold Black joined Bell laboratories, he became aware of this distortion and found solving involving known as 'feed forward correction'.

The basic idea is to build 2 identical amplifiers and use one amplifier to subtract out the distortion of the first.



* There is no feedback and signals move forward only from input to output
* 2 - time delay elements, which compensate for group delay 2 of each amplifier, ensuring substraction operation on signals that have experienced equal delays in travelling the over all system.
* linear gain A, non linear gain Ã
* The input is given to amplifier and Produces nominal gain A and produces some distortion as the process and its output is

AVIN + E → error voltage (where assumed to be small)

* The output of 1st amplifier is given to linear attenuator whose gain is 1/A

The attenuator output is subtracted from the input to get voltage which is perfectly scaled version of distortion.

* This pure distortion signals feeds to another amplifier. Because we have assumed distortion is small in first place we expect 2nd amplifier to act quite linearly and produces excellent approximation to the original distortion

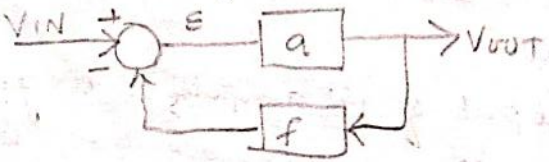
* The distortion from second amplifier is subtracted from the distorted signal of first amplifier to yield final output that has greatly reduced distortion.

Disadvantage

- Proved impractical with old technology.
- It is virtually impossible to maintain tight levels of matching to make feed forward amplifier work well.

THE NEGATIVE FEEDBACK AMPLIFIER.

On August 1927, the idea of negative feedback amplifier came to mine.



The overall gain is

$$A = \frac{a}{1+af}$$

make af product much larger than unity

$$A \simeq 1/f$$

Observations

* The feedback factor f can be implemented with linear elements like resistive voltage divider, so that over all closed loop behaviour is linear even though the amplifier in block a is not.

* closed loop gain A is much smaller than forward gain but. if gain is cheap but not distortion and best solution for is negative feedback.

DESENSITIVITY OF NEGATIVE FEEDBACK SYSTEMS.

There are some valid claims about negative feedback

(i) It increases bandwidth
(ii) It decreases distortion
(iii) It reduces noise.
(iv) removes unsightly facial blemishes.

One absolute fundamental benefit is the desensitivity (ie) The overall passes an attenuated sensitivity to changes in the forward gain a

if $af >> 1$

To quantify this notation of desensitivity let's calculate differential change in A that result from differential change in a.

$$\frac{dA}{da} = \frac{d}{da}\left(\frac{a}{1+af}\right) = \frac{1}{(1+af)^2} = \frac{A}{a}\left(\frac{1}{1+af}\right)$$

By Re-arranging

$$\frac{dA}{A} = \frac{da}{a}\left(\frac{1}{1+af}\right)$$

The above equation tell us that given fractional change in A equals the fractional change in a, attenuated ("desensitized") by a factor of $1+af$. For this reason, the quantity $1+af$ is often called the desensitivity of a feedback system.

* If forward gain varies with time, temperature, or i/p amplitude, the closed-loop gain exhibits smaller variations since they are attenuated by desensitivity factor. If factor af is large, the desensitivity will be large and variation in A due to change in A.

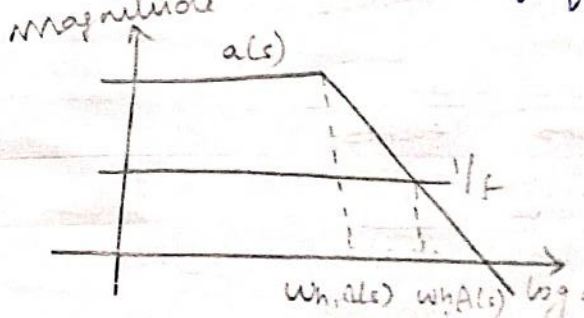
$$\frac{dA}{df} = \frac{d}{df}\left(\frac{a}{1+af}\right) = -\frac{a^2}{(1+af)^2}$$

$$\frac{A}{f}\left(\frac{-af}{1+af}\right).$$

(i) Negative feedback extends bandwidth.

The negative feedback extends bandwidth by selectively throwing away gain at lower frequencies.

Let us suppose that forward gain is now at purely scalar quantity but is instead some a(s) that rolls off with single pole behaviour, as long as af had magnitude large compared with unity, the closed loop gain equal to reciprocal of feeback gain.



Plotting $|a(s)|$ and $|1/f|$ on same graph.

* If $|1/f|$ is much lower than $|a(s)|$ → a(s)f has large magnitude and therefore closed loop behaviour is approximately $1/f$

* If $|1/f|$ is much higher than $|a(s)|$, a(s)f has small magnitude and closed loop behaviour converges to a(s).

(ii) Negative feedback reduces noise.

* Actually negative feedback cannot reduce input-referred noise of a system
* In most practical cases feedback typically increases the input-referred noise

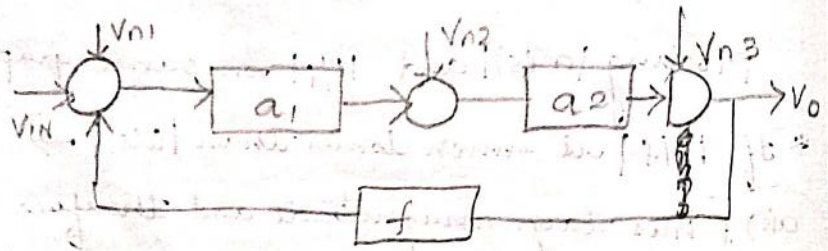
The idea that negative feedback reduces noise stems, for such system the transfer functions are

$$\frac{V_{out}}{V_{in}} = \frac{a_1 a_2}{1+a_1 a_2 f}$$

$$\frac{V_{out}}{V_{n1}} = \frac{a_1 a_2}{1+a_1 a_2 f}$$

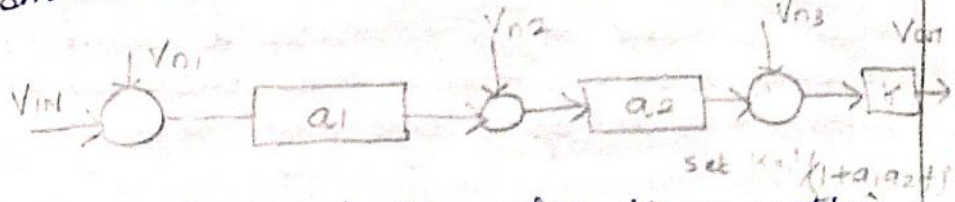
$$\frac{V_{out}}{V_{n2}} = \frac{a_2}{1+a_1 a_2 f}$$

$$\frac{V_{out}}{V_{n3}} = \frac{1}{1+a_1 a_2 f}$$



From these eqn, the gain from noise sources V_{ni} to the output is same as that the input to the output as amplifier cannot differentiate input and V_{ni} and enters the same point.

But gain to other noise sources are small which is a benefit



set $K = \frac{1}{1+a_1 a_2 f}$

To understand the idea that nothing happens with negative feedback limit to have gain between two nodes, where noise signal could enter.

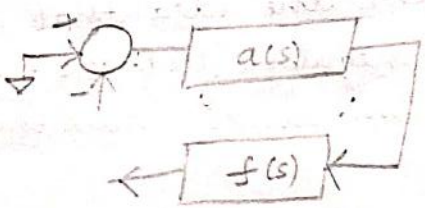
We choose K, for which the input and output transfer functions of the feedback and open loop amplifiers are same for every input. Thus feedback offers no noise reduction beyond what open-loop system could give.

Finally, the desensitivity to the forward gain is the only benefit confirmed by negative feedback which is fundamental one.

STABILITY OF FEEDBACK SYSTEMS

The use of negative feedback allows the closed-loop transfer function $A(s)$ to approach the reciprocal of feedback gain f as (minus) the loop transmission $a(s)f(s)$ increases,

We use BIBO definition of stability which states that a system is stable if every bounded input produces a bounded output. A system H(s) is BIBO stable if all poles of H(s) are in open left half plane.



To apply this test to our feedback system we must find poles of A(s), the roots of $P(s) = 1 + a(s)f(s)$.

Determination of loop transmission is usually straight forward, whereas the closed loop transfer function requires identification of forward path and an additional mathematical step. Hence any method can determine stability from examination of loop transmission.

GAIN AND PHASE MARGIN AS STABILITY MEASURE

For stability consideration, TO determine whether Sine wave actually sine wave exist require the use of nyquist stability test. which is complicated and many fail to use it.

stability measure is used instead of nyquist test to find quantities like Phase margin and gain Margin.

(i) Gain Margin : Find fqeuny at which Phase shift of $a(j\omega)f(j\omega)$ is -180° called $\omega\pi$. Then gain Margin is $\frac{1}{|a(j\omega\pi)f(j\omega\pi)|}$

(ii) Phase Margin - The frequency at which magnitude of $a(j\omega)f(j\omega)$ is unity call this frequency ωc, the cross over frequency.

Phase margin $= 180^\circ + \angle[a(j\omega c) f(j\omega c)]$.

ROOT LOCUS TECHNIQUE.

Gain and Phase use behaviour of loop transmission to determine the stability of closed loop system

* TO find roots of the polynomial $1 + a(s) f(s)$

$$P(s) = 1 + a(s)f(s) = 0$$

$$\Rightarrow a(s)f(s) = -1.$$

may decompose as magnitude and phase angle for loop transmission.

$|a(s)f(s)| = 1$

$\angle[a(s)f(s)] = (2n+1).180^\circ$

Rule 1: The locus starts at the poles of the loop transmission and it terminates on the zeros of loop transmission.

Suppose $a(s)f(s)$ as $kg(s)$. $K \rightarrow$ gain factor and varying $g(s)$

$$|g(s)| = \frac{1}{K}$$

where $g(s)$ must be large for small value of K. hence s satisfy magnitude, conditions near pole of $g(s)$, and when small indicates values of s near zeros of $g(s)$.

Rule 2: If a root locus branch lies on the real axis, it resides to the left of an odd number of left hay plane poles + zeros and to the right of an odd number of right hay plane poles + zeros.

$$g(s) = \frac{\Pi_{i=1}^{z}(T_{zi}s+1)}{\Pi_{K=1}^{p}(T_{pK}s+1)}$$

Rule 3: If number of poles exceeds the number of zero by two or more, then average distance of poles to the imaginary axis is

is independent of K

$$C.\prod_{j=1}^{n}(s+s_j) = C.\left[s^n + s^{n-1}\sum_{j=1}^{n}s_j + \frac{n}{\Pi}_{j=1} s_j\right] = L(s).$$

$$g(s) = p(s)/q(s)$$

$$P(s) = q(s) + Kp(s).$$

Rule 4: As $K \rightarrow 0$, $P \rightarrow z$ branches to ∞

$$\theta_n = \frac{(2n+1).180^\circ}{P-z}$$

Rule 5:

$$\sigma = \frac{\Sigma Re(poles) - \Sigma Re(zeros)}{P-z}$$

$$P(s) = 1 + \frac{C_1.\left[s^z + s^{z-1}\sum_{i=1}^{z} Re(zeros)_i\right]}{s^p + s^{p-1}\sum_{i=1}^{p} Re(poles)_i}$$

$$0 \simeq 1 + \frac{C_1}{s^{p-z} + s^{p-z-1}\left[\Sigma Re(poles) - \Sigma Re(zeros)\right]}$$

Rule 6: If real axis branch of locus lies b/w a pair of poles then locus breaks away from the real axis between the poles.

Rule 7: The locus forms an initial stage angle θ_p with respect to complex pole or angle θ_z

$$\theta_p = 180^\circ - \sum\angle[\text{poles}] + \sum\angle[\text{zeros}]$$

$$\theta_z = 180^\circ + \sum\angle[\text{poles}] - \sum\angle[\text{zeros}]$$

$$-\theta_p + \sum\angle[\text{zeros}] - \sum\angle[\text{poles}]$$

$$\theta_z + \sum\angle[\text{zeros}] - \sum\angle[\text{poles}]$$

Rule 8:

If a particular value of s is known to lie on locus.

$$K = \frac{1}{|g(s)|}$$

ROOT-LOCUS RULES FOR POSITIVE FEEDBACK SYSTEM.

$$\angle g(s) = n \cdot 360^\circ$$

rules developed for negative feedback in which $K > 0$

Therefore all occurrence of $(2n+1)\cdot 180^\circ$ should be replaced with $n \cdot 360^\circ$.

ZEROS OF A(s).

how poles of A(s) behave is given by root locus, given poles and zeros of g(s).

$$A(s) = \frac{a(s)}{1 + a(s) f(s)}$$

FREQUENCY AND TIME DOMAIN CHARACTERISTICS OF FIRST ORDER AND SECOND ORDER SYSTEM.

Formulas for first-order low pass system.

Assume transfer function is

$$H(s) = \frac{1}{\tau s + 1}$$

$$t_r = \tau \ln 9 \simeq 2.2\tau = 2.2/\omega_h$$

$$P_o = M_P = 1$$

$$t_p = \infty$$

$$t_{s/2\%} \simeq 4\tau$$

$$\varepsilon_1 = \tau$$

$$\omega_p = 0;$$

Formulas for second order system

$$H(s) = \left[\frac{s^2}{\omega_n^2} + 2\frac{\xi_1 s}{\omega_n} + 1\right]^{-1}$$

$$t_r \simeq 2.2\tau = \frac{2.2}{\omega_h}$$

$$P_o = 1 + \exp\left(\frac{-\pi \xi}{\sqrt{1-\xi^2}}\right)$$

$$t_p = \frac{T_{osc}}{2} = \frac{\pi}{\omega_n \sqrt{1-\xi^2}}$$

$$t_{s|2\%} \simeq 4\tau_{env} = \frac{4}{\xi \omega_n}$$

$$\varepsilon_1 = \frac{2\varepsilon}{\omega_n}$$

$$M_p = \frac{1}{2\xi\sqrt{1-\xi^2}}, \quad \varepsilon < \frac{1}{\sqrt{2}}$$

$$\omega_p = \omega_n \sqrt{1-2\xi^2}, \quad \xi < \frac{1}{\sqrt{2}}$$

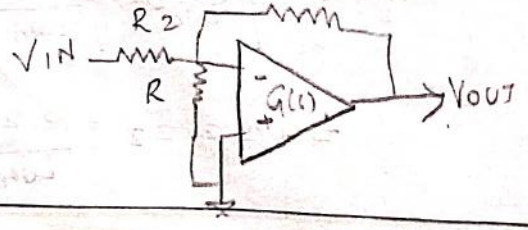
$$\omega_h = \omega_n \left[1 - 2\xi^2 + \sqrt{2 - 4\xi^2 + 4\xi^4}\right]^{1/2}$$

$$= \omega_n \Big|_{\xi = 1/\sqrt{2}}$$

COMPENSATIONS:

Compensations through Gain Reduction

Example $G(s) = \dfrac{10^7}{(s+1)(10^{-3}s+1)}$



$$-L(s) = \frac{R_2}{R_1+R_2} \cdot G(s) = 10^{-2} \cdot G(s)$$

$$= \frac{10^5}{(s+1)(10^{-3}s+1)}$$

$$\omega_c \simeq 10^4 \text{ rps}$$

A new desired cross over frequency.

$$|L(j10^3)| = \frac{10^5}{|\sqrt{10^6+1}|\sqrt{2}|} = 70.7$$

Old loop transmission

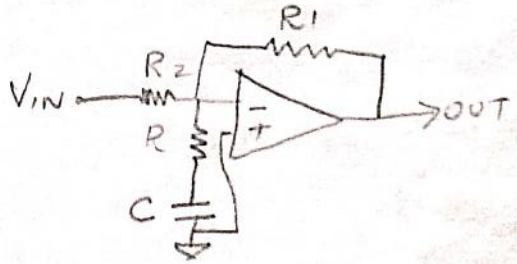
$$-L(s) = \frac{R_2}{R_1+R_2} \cdot G(s) = \left(\frac{R_1}{R_2}+1\right)^{-1}$$

$$= G(s)$$

New loop transmission

$$-L(s) = \left(\frac{R_1}{R_2 \| R} + 1\right)^{-1} \cdot G(s)$$

$$R \simeq \frac{R_2}{70.4}$$



LAG COMPENSATION

To discover the real effect of compensator

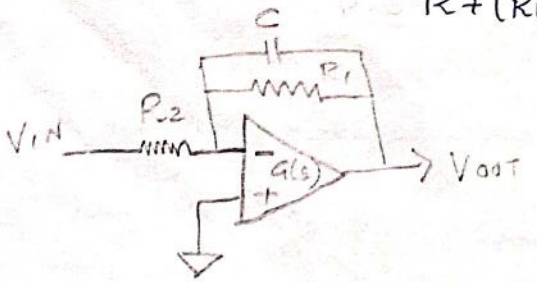
$$-L(s) = \left[\frac{R1}{R2 \| R + 1/sC} + 1\right] \cdot G(s)$$

$$-L(s) = \left\{\frac{sRC+1}{sC[R(1+R_1/R_2)+R_1]} + (1+R_1/R_2)\right\} \cdot G(s)$$

$$-L(s) = \left\{\frac{sRC+1}{sC[R+R_1\|R_2)]+1}\right\} \cdot \frac{R_2}{R_1+R_2} G(s)$$

At DC, the compensator transfer function is unity

$$C(s) \to \frac{R_1}{R+(R_1\|R_2)}$$



LEAD COMPENSATION

We have seen phase margin can be improved by reducing the magnitude of loop transmission in order to lower the cross frequency.

An Alternative method to alter Phase of loop transmission than its magnitude.

We wish to add positive or leading phase shift near cross over to improve phase margin.

Addition of capacitor causes the loop transmission to zero. As frequency increases, transmission through capacitor increase.

A zero provides an increase phase margin, magnitude addition to its positive phase shift.

$$-L(s) = \frac{R_2}{R_2+[R_1 \| 1/sC]} \cdot G(s)$$

which may expressed as.

$$-L(s) = \left(\frac{R_2+R_1}{R_1}\right)\left(\frac{sR_1C+1}{sR_1C+1+R_1/R_2}\right) \cdot \frac{R_2}{R_2+R_1} \cdot G(s)$$

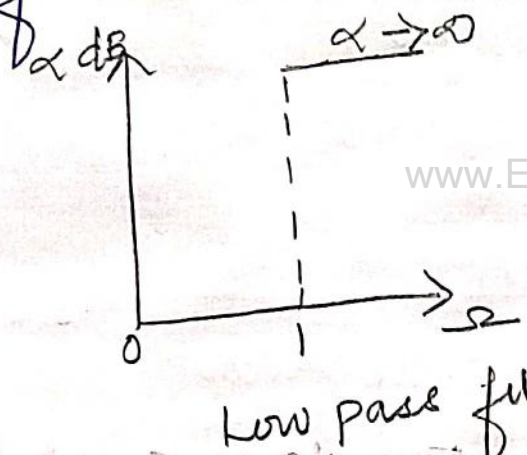
UNIT - 4

FILTER, OSCILLATOR AND MIXER

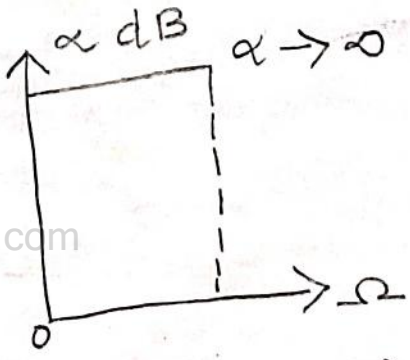
Overview - basic resonator and filter configuration Special filter realization. filter implementation Basic oscillator model, high frequency oscillator configuration, colpitt's configuration - basic characteristics of mixers, single and double balanced mixers.

BASIC RESONATOR AND FILTER CONFIGURATION

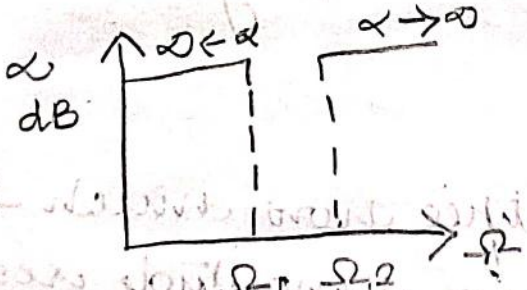
The ideal behaviour of four types of filters

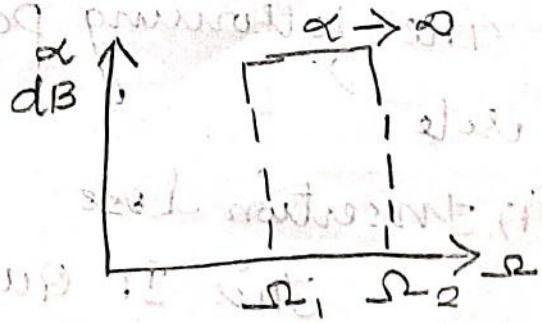


Low pass filter



High pass filter





$\Omega = w/w_c$ as normalized frequency.

w_c → cut off frequency for Low pass and high frequency.

→ centre frequency for band pass and Band stop filter.

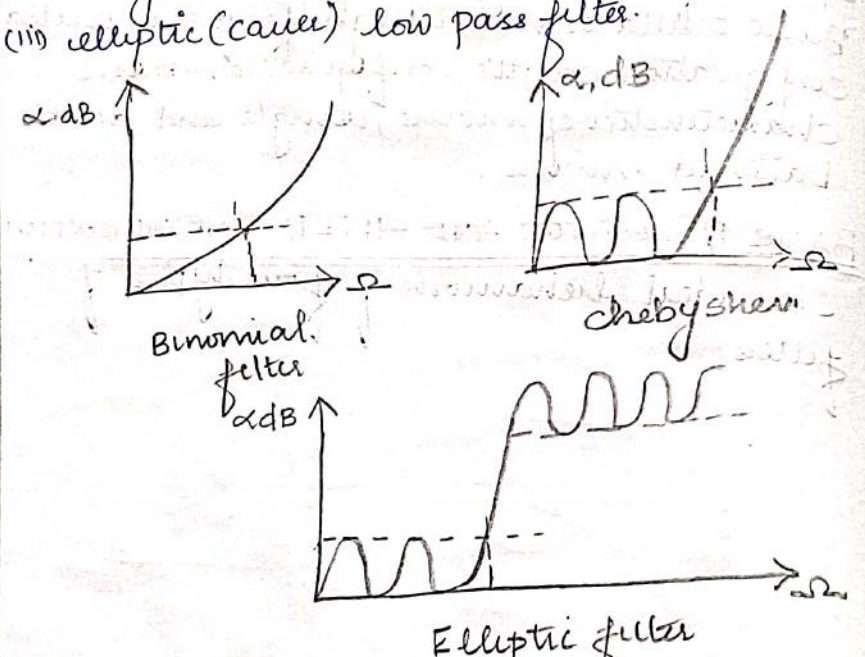
There are 3 standard filter approaches

They are

(i) binomial (Butterworth)

(ii) chebyshere

(iii) elliptic (cauer) low pass filter.



The following parameters plays a vital role:

(i) Insertion loss:

This IL Quantifies how much below the 0dB line the power amplitude response drops.

$$IL = 10 \log \frac{P_{in}}{P_L} = -10 \log (1 - |\Gamma_{in}|^2).$$

P_{in} → Power input from source

P_L → Power delivered to load.

$|\Gamma_{in}|$ → reflection coefficient

RIPPLE: The flatness of signal in passband can be quantified specifying the ripple or difference between maximum and minimum amplitude response in either dB or neper.

BANDWIDTH:

Bandwidth defines the difference between upper and lower frequencies typically recorded at 3dB attenuation point above passband

$$BW^{3db} = f_u^{3dB} - f_L^{3dB}.$$

SHAPE FACTOR:

This factor describes the sharpness of the filter by taking ratio between the 60dB and 3 dB bandwidth

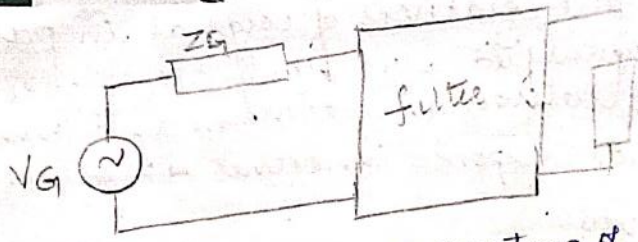
$$SF = \frac{BW^{60dB}}{BW^{3d}} = \frac{f_u^{60dB} - f_L^{dodB}}{f_u^{3dB} - f_L^{3dB}}.$$

REJECTION:

For ideal filter, the infinite attenuation level for undesirable signal frequencies. One additional parameter describes the sensitivity of filter is Q factor.

$$Q = w \frac{\text{average store energy}}{\text{energy loss per cycle}} \Big|_{w = w_c}$$

$$= w \frac{\text{average stored energy}}{\text{Power Lose}} \Big|_{w = w_c} = w \frac{W_{stored}}{P_{loss}} \Big|_{w = w_c}$$



The power loss as consisting of power loss associated with external load and filter. The resulting Q factor is called loaded Q or Q_{LD}.

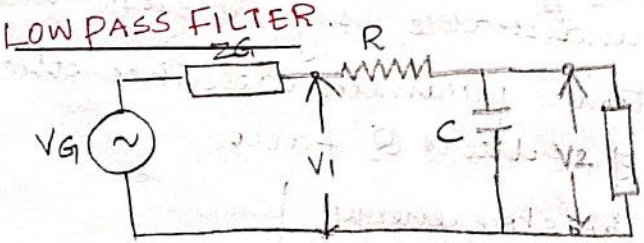
$$\frac{1}{Q_{LD}} = \frac{1}{\omega}\left[\frac{\text{Power loss in filter}}{\text{average stored energy}}\right]\Bigg|_{\omega=\omega_x} + \frac{1}{\omega}\left[\frac{\text{Power loss in load}}{\text{average stored energy}}\right]_{\omega=\omega_x}$$

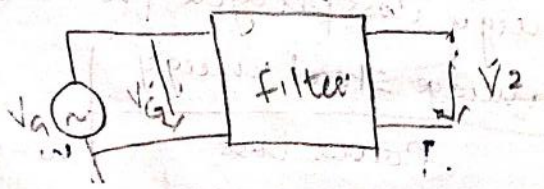
$$\frac{1}{Q_{LD}} = \frac{1}{Q_F} + \frac{1}{Q_E}$$

(filter Q) (external Q)

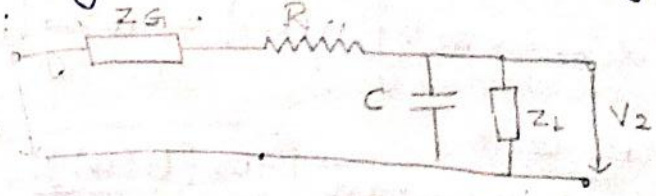
$$Q_{LD} = \frac{f_c}{f_U^{3dB} - f_L^{3dB}} = \frac{f_c}{BW^{3dB}}.$$

LOW PASS FILTER





For any filter design, it is to find V_2 due to input voltage V_1 or the generator voltage V_G.



The overall ABCD network is

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & R_G \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 1 & R \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 1 & 0 \\ 1/R_L & 1 \end{bmatrix}$$

$$= \begin{bmatrix} 1+(R+R_G)\left(j\omega C + \frac{1}{R_L}\right)R_G + R_L & \\ j\omega C + \frac{1}{R_L} & 1 \end{bmatrix}$$

Both source impedance and load impedance are resistive (i.e) $Z_G = R_G$ and $Z_L = R_L$.

$$\frac{V_2}{V_G} = \frac{1}{A} = \frac{1}{1+(R+R_G)\left(j\omega C + \frac{1}{R_L}\right)}$$

$$\frac{V_2}{V_G} = \frac{1}{1+(R+R_G)/R_L} = \frac{R_L}{R_G+R+R_L}$$

for $\omega \to \infty$

$$\frac{V_2}{V_G} = 0$$

In first order

$$\frac{V_2}{V_G} = H(\omega) = \frac{1}{1+j\omega(R_G+R)C}.$$

$$\alpha(\omega) = -\ln|H(\omega)| = -\frac{1}{2}\ln|H(\omega)|^2$$

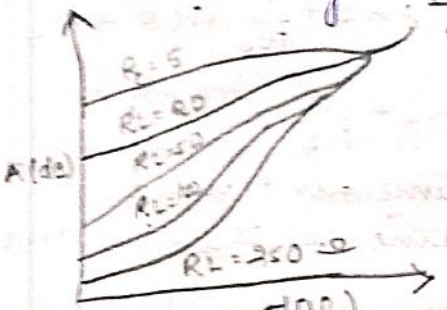
$$\alpha(\omega) = -20\log|H(\omega)| = -10\log|H(\omega)|^2$$

Phase is

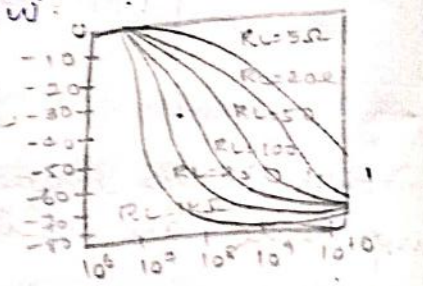
$$\phi(\omega) = \tan^{-1}\left[\frac{\mathrm{Im}\{H(\omega)\}}{\mathrm{Re}\{H(\omega)\}}\right]$$

Phase is called group delay t_g.

$$t_g = \frac{d\phi(\omega)}{d\omega}$$



(Attenuation profile)



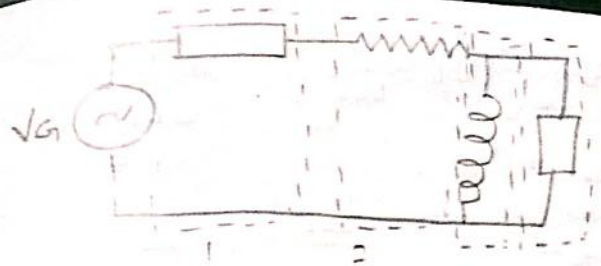
(phase response)

HIGH PASS FILTER

Replacing capacitor with inductor allows the construction of first order high pass filter.

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & R_G \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 1 & R \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 1 & 0 \\ \frac{1}{j\omega L} & 1 \end{bmatrix}\begin{bmatrix} 1 & 0 \\ \frac{1}{R_L} & 1 \end{bmatrix}$$

$$= \begin{bmatrix} 1+(R+R_G)\left[\frac{1}{j\omega L}+\frac{1}{R_L}\right] & R_G+R \\ j\omega C+\frac{1}{R_L} & 1 \end{bmatrix}$$



$$\frac{V_2}{V_G} = \frac{1}{A} = \frac{1}{1+(R+R_G)\left[\frac{1}{j\omega L}+\frac{1}{R_L}\right]}$$

as $\omega \to 0$

$$\frac{V_2}{V_G} = 0$$

as $\omega \to \infty$

$$\frac{V_2}{V_2} = \frac{1}{1+(R+R_G)/R_L} = \frac{R_L}{R_G+R+R_L}$$

BANDPASS AND BANDSTOP FILTER

A Bandpass filter can be constructed through RLC series or through parallel connection of RLC shunt circuit.

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & Z_G \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 1 & Z \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 1 & 0 \\ 1/Z_L & 1 \end{bmatrix}$$

$$= \begin{bmatrix} 1+\frac{Z+Z_G}{Z_L} & Z_G+Z \\ \frac{1}{Z_L} & 1 \end{bmatrix}$$

$$Z = R + j\left(\omega L - \frac{1}{\omega C}\right).$$

$$H(\omega) = 1/A$$

$$\frac{V_2}{V_G} = H(\omega) = \frac{Z_L}{(Z_L + Z_G) + R + j[\omega L - 1/(\omega C)]}$$

SPECIAL FILTER REALIZATIONS

There are 2 types of filters.

(I) The maximally flat Butterworth.

(II) The equi-ripple Chebyshev filter.

BUTTERWORTH-TYPE FILTER.

This filter type is known as maximally flat filter as no ripple is permitted in its attenuation profile.

$$IL = -10\log(1 - |T_{in}|^2 = 10\log\{LF\}$$

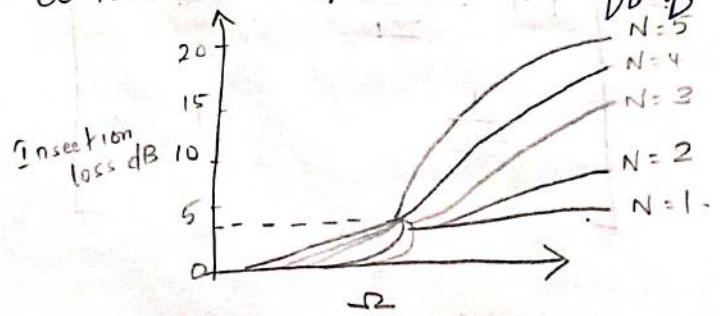
$$= 10\log\{1 + a^2\Omega^{2N}\}.$$

Ω - normalized frequency.

$N \rightarrow$ order of filter.

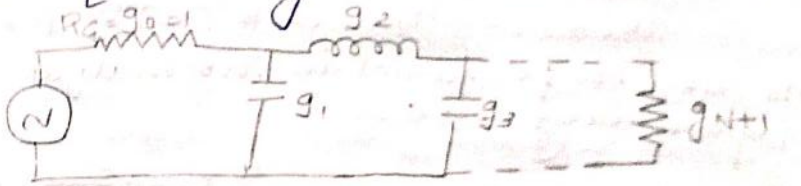
when $a = 1$ $\Omega = \omega/\omega_C = 1$, then $IL = 1.0\log\{2\}$.

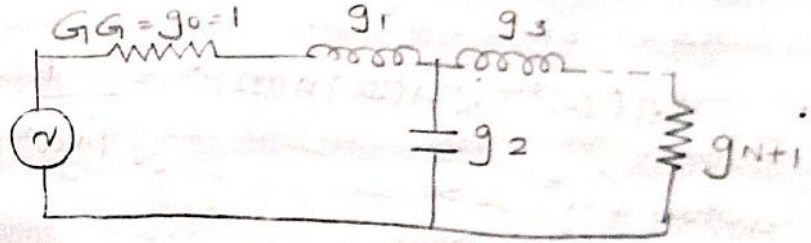
which is 3 dB point at cut off frequency.



The elements are numbered g_0 at generator side and g_{N+1} at load as elements alternate between series inductance and shunt capacitance.

$g_0 =$ { internal generator resistance / internal generator conductance





$g_m =$ { inductance for series inductor / capacitance for shunt capacitor ($m = 1 \ldots N$)

$g_{N+1} =$ { load resistance if last element is shunt capacitor / load conductance if last element is series inductor.

Linear phase behaviour is more critical issue in wireless communication

$$\phi(\Omega) = A_1\Omega(1 + A_2\Omega^{2N}).$$

The associated group delay t_g is

$$t_g = \frac{d\phi(\Omega)}{d\Omega} = A_1\left[1 + A_2(2N+1)\Omega^{2N}\right]$$

CHEBYSHEV FILTER TYPE

The design of equi ripple filter type is described by chebyshev polynomial $T_N(\Omega)$.

$$LF = 10\log\{LF\} = 10\log\{1+a^2 T_N^2(\Omega)\}$$

$$T_N(\Omega) = \cos\{N[\cos^{-1}(\Omega)]\}, \text{ for } |\Omega| \le 1$$

$$T_N(\Omega) = \cosh\{N[\cosh^{-1}(\Omega)]\}, \text{ for } |\Omega| \ge 1$$

The chebyshev polynomial in normalized frequency range $-1 < \Omega < 1$.

$T_0 = 1, T_1 = \Omega, T_2 = -1 + 2\Omega^2, T_3 = -3\Omega + 4\Omega^3$.

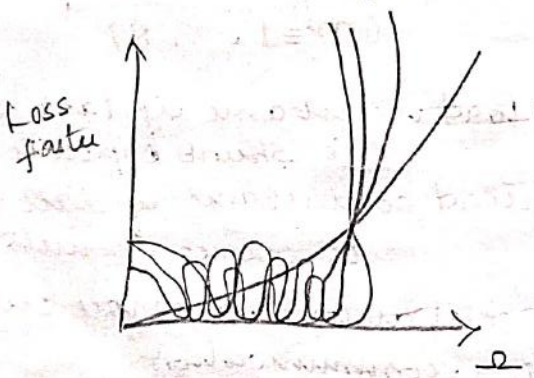
$T_4 = 1 - 8\Omega^2 + 8\Omega^4$.

$$|H(\Omega)| = \sqrt{H(\Omega)H(\Omega)^*} = \frac{1}{\sqrt{1+a^2 T_N^2(\Omega)}}$$

when $a = 1$, $\Omega = 1$

we have

$$|H(0)| = \frac{1}{\sqrt{2}} = 0.707.$$



FILTER IMPLEMENTATION:

Filter design beyond 500 MHz are difficult to realize with discrete components because wavelength becomes comparable with physical filter elements resulting in loss that degrade the circuit performance. Thus to arrive at practical filters, the lumped component filters must be converted to distributed element realizations.

The neccassary tools are

(i) Richards Transformation
(ii) the concept of unit element and
(iii) Kuroda's identities.

There should a conversion be established between lumped and distributed design. Richard proposed a transformation that allows open- and short circuit transmission line segment to emulate inductive and capacitive behaviour of discrete components.

Impedence Z_{in} of short circuit line of characteristic line impedence Z_0 is reactive

$$Z_{in} = jZ_0 \tan(\beta l) = jZ_0 \tan\theta.$$

reference frequency $f_0 = v_p/\lambda_0$.

$$\theta = \beta\frac{\lambda_0}{8} = \frac{2\pi f}{v_p}\frac{v_p}{8f_0} = \frac{\pi f}{4f_0} = \frac{\pi}{4}\Omega.$$

$$jX_L = jwL = jZ_0 \tan\left[\frac{\pi}{4}\frac{f}{f_0}\right]$$

$$= jZ_0 \tan\left[\frac{\pi}{4}\Omega\right] = SZ_0$$

where $S = j\tan(\pi\Omega/4)$ is actual Richards transform.

$$\therefore jB_C = j\omega C_1 = jY_0 \tan\left[\frac{\pi}{4}\Omega\right] = SY_0$$

$Z_0 = L$, and $Z_0 = 1/C$.

$\lambda_0/8$ is length, a property that is known as commensurate line length.

UNIT ELEMENT:

When converting lumped elements into transmission lines (elements spatially to achieve practically realizable configuration by inserting so-called unit elements (UE's). The unit length has electric length of $\theta = \frac{\pi}{4}\left(\frac{f}{f_0}\right)$

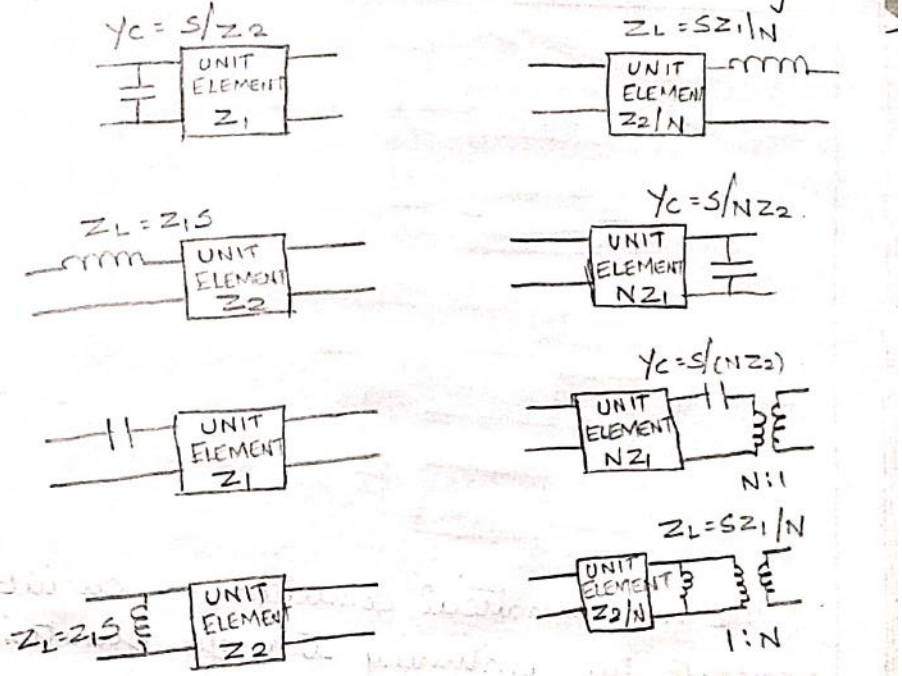
$$[UE] = \begin{bmatrix} A_{UE} & B_{UE} \\ C_{UE} & D_{UE} \end{bmatrix} = \begin{bmatrix} \cos\theta & jZ_{UE}\sin\theta \\ \frac{j\sin\theta}{Z_{UE}} & \cos\theta \end{bmatrix}$$

$$= \frac{1}{\sqrt{1-S^2}} \begin{bmatrix} 1 & Z_{UE}S \\ \frac{S}{Z_{UE}} & 1 \end{bmatrix}$$

KURODA'S IDENTITIES

It is important to convert a practially difficult-to-implement design to more suitable filter realization.

Initial Circuit — Kuroda's Identity

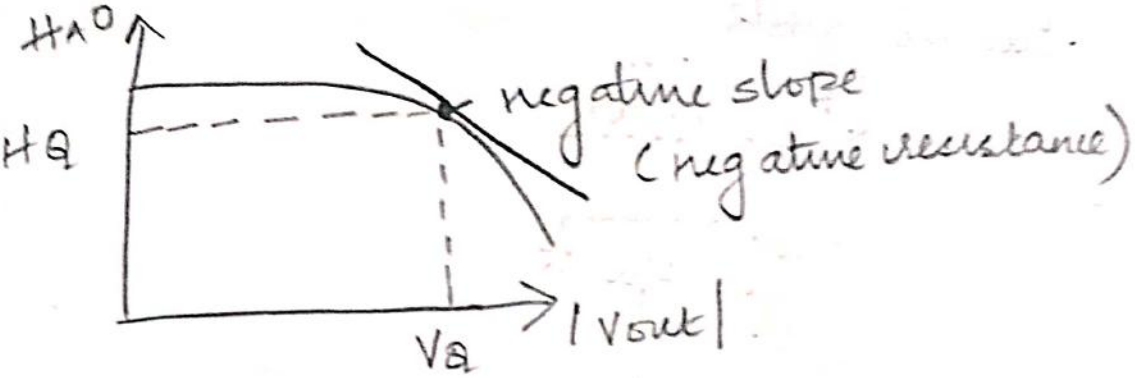


$$N = 1 + Z_2/Z_1$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_L = \begin{bmatrix} 1 & 0 \\ \frac{1}{SZ_1} & 1 \end{bmatrix} \frac{1}{\sqrt{1-S^2}} \begin{bmatrix} 1 & Z_2 S \\ \frac{S}{Z_2} & 1 \end{bmatrix} = \frac{1}{\sqrt{1-S^2}} \begin{bmatrix} 1 & Z_2 S \\ 1 + \frac{S}{SZ_1 Z_2} & 1 + \frac{Z_2}{Z_1} \end{bmatrix}$$

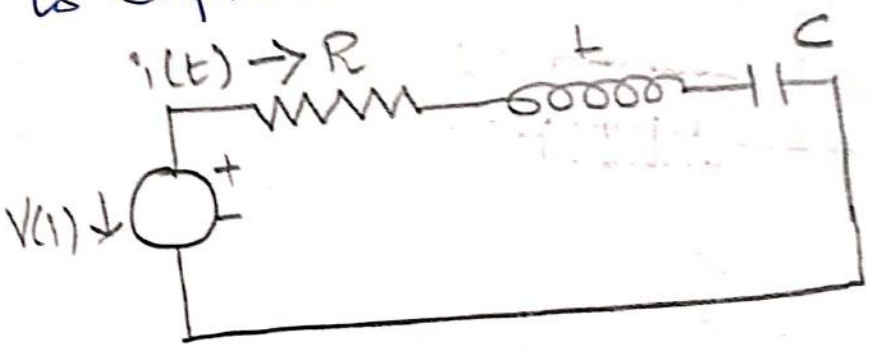
$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_R = \frac{1}{\sqrt{1-S^2}} \begin{bmatrix} 1 & \frac{Z_2 S}{N} \\ \frac{SN}{Z_2} & 1 \end{bmatrix}_{UE} \begin{bmatrix} 1 & 0 \\ \frac{N}{SZ_1} & 1 \end{bmatrix}_{ind} \begin{bmatrix} 1/N & 0 \\ 0 & N \end{bmatrix}_{trans}$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_R = \frac{1}{\sqrt{1-S^2}} \begin{bmatrix} \frac{1}{N}\left(1 + \frac{Z_2}{Z_1}\right) & Z_2 S \\ \frac{S}{Z_2} + \frac{1}{SZ_1} & N \end{bmatrix}.$$



Negative Resistance Oscillator.

is explained with R L C circuit.



$$L\frac{d^2i(t)}{dt^2} + R\frac{di(t)}{dt} + \frac{1}{C}i(t) = -\frac{dV(i)}{dt}$$

$$i(t) = e^{\alpha t}(\hat{I}_1 e^{j\omega_Q t} + \hat{I}_2 e^{-j\omega_Q t}).$$

where $\alpha = -R/2L$, $\omega_Q = \sqrt{1/(LC) - (R/(2L))^2}$.

α is negative Quantity

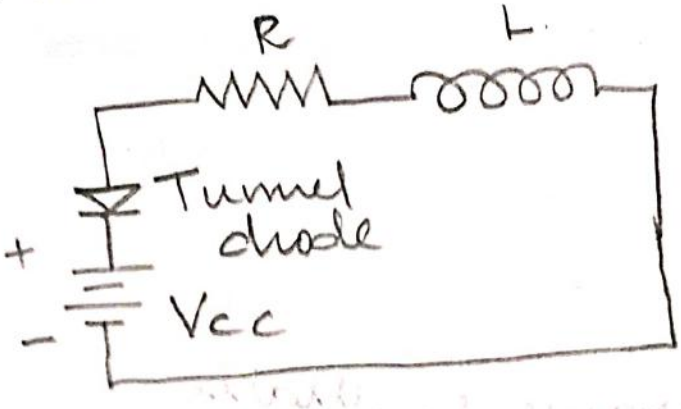
$$V(i) = V_0 + R_1 i + R_2 i^2 + \dots$$

$$L\frac{d^2i(t)}{dt^2} + R\frac{di(t)}{dt} + \frac{1}{C}i(t) = \frac{dV(t)}{dt}$$

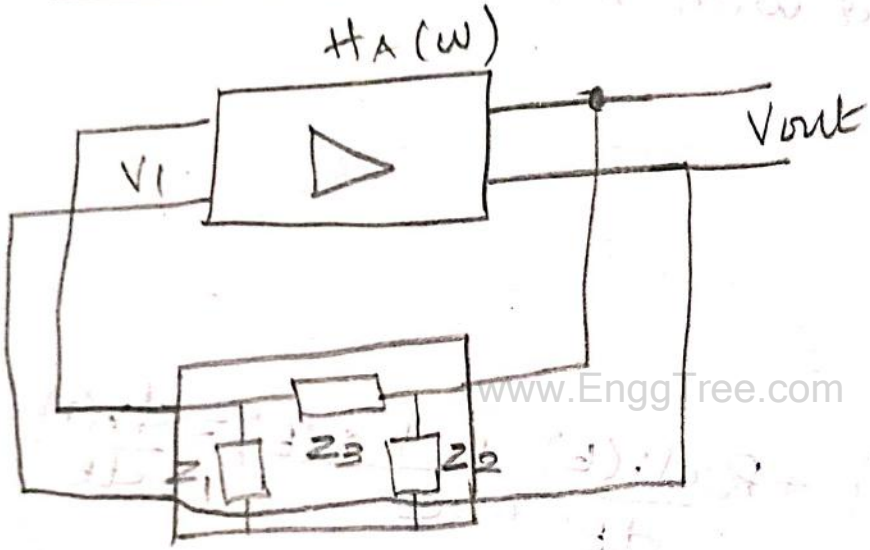
$$= -R_1\frac{di(t)}{dt}.$$

$$R + R_1 = 0$$

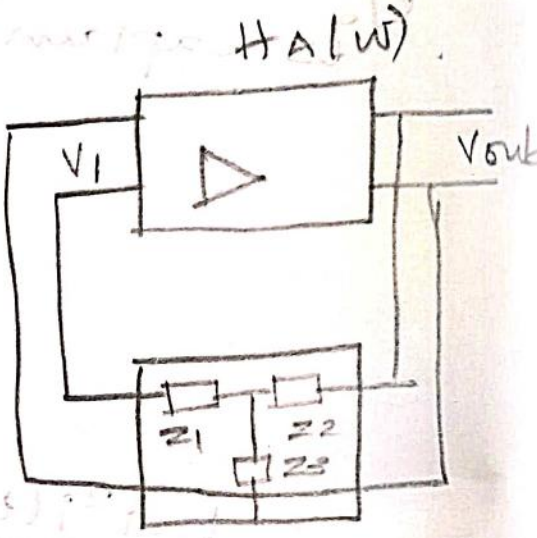
Negative resistance can be achieved by tunnel diode.



FEEDBACK OSCILLATOR DESIGN.



Pi-type



T-type

$$H_F(w) = \frac{V_1}{V_{out}} = \frac{Z_1}{Z_1 + Z_3}$$

$$\mu_V V_1 + I_B R_B + I_B Z_C = 0$$

where $1/Z_C = Y_C = 1/Z_2 + 1/(Z_1 + Z_3)$

$$H_A(\omega) = \frac{V_{out}}{V_1} = \frac{-\mu_V}{Y_C R_B + 1}$$

closed transfer function is

$$H_f(\omega) H_A(\omega) = \frac{-\mu_V Z_1 Z_2}{Z_2 Z_1 + Z_2 Z_3 + R_B(Z_1 + Z_2 + Z_3)}$$

$$\equiv 1.$$

$$X_3 = -(X_1 + X_2).$$

$$\frac{\mu_V X_1 X_2}{-X_2 X_1 + X_2(X_1 + X_2)} = \frac{\mu_V}{X_2} X_1 = 1.$$

HIGH FREQUENCY OSCILLATOR CONFIGURATION

As operating frequency approaches GHz range the wave nature of voltage and current cannot be neglected.

The input reflection coefficient for matched source impedence

$$\Gamma_{in} = \frac{b_1}{a_1} = S_{11} + \frac{S_{12}S_{21}}{1 - S_{22}\Gamma_L} = \frac{S_{11} - \Delta\Gamma_L}{1 - S_{22}\Gamma_L}.$$

where $\Delta = S_{11}S_{22} - S_{12}S_{21}$.

$b_3 = V_G\sqrt{Z_0}/(Z_G + Z_0)$.

$$\frac{b_1}{b_3} = \frac{\Gamma_{in}}{1 - \Gamma_S \Gamma_{in}}$$

$$\Gamma_{in}\Gamma_S = 1.$$

The identical circuits.

$$\Gamma_{out}\Gamma_L = 1.$$

when stability factor $K = (1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2)/(2|S_{12}||S_{21}|)$.

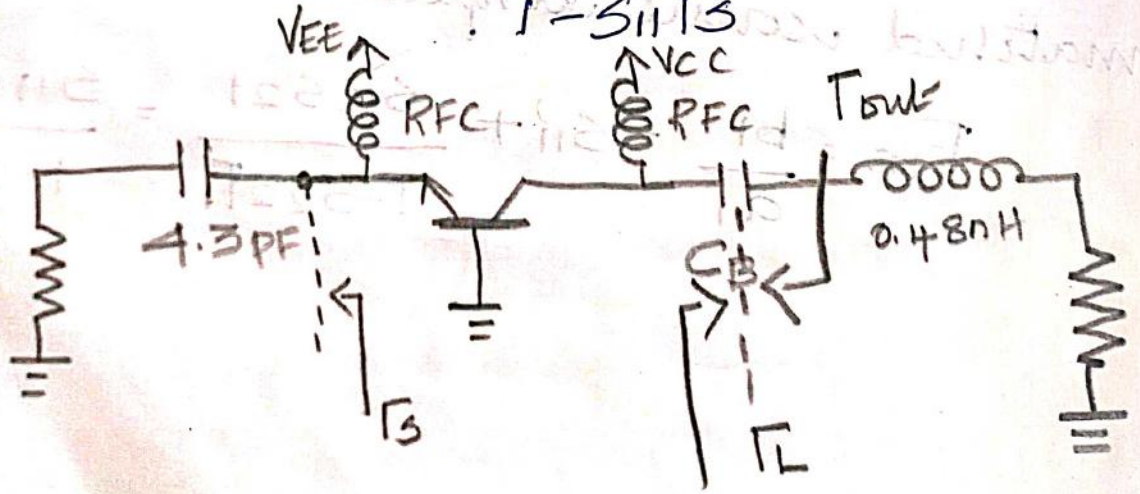
$K < 1$

$$\Gamma_{in}\Gamma_S = 1$$

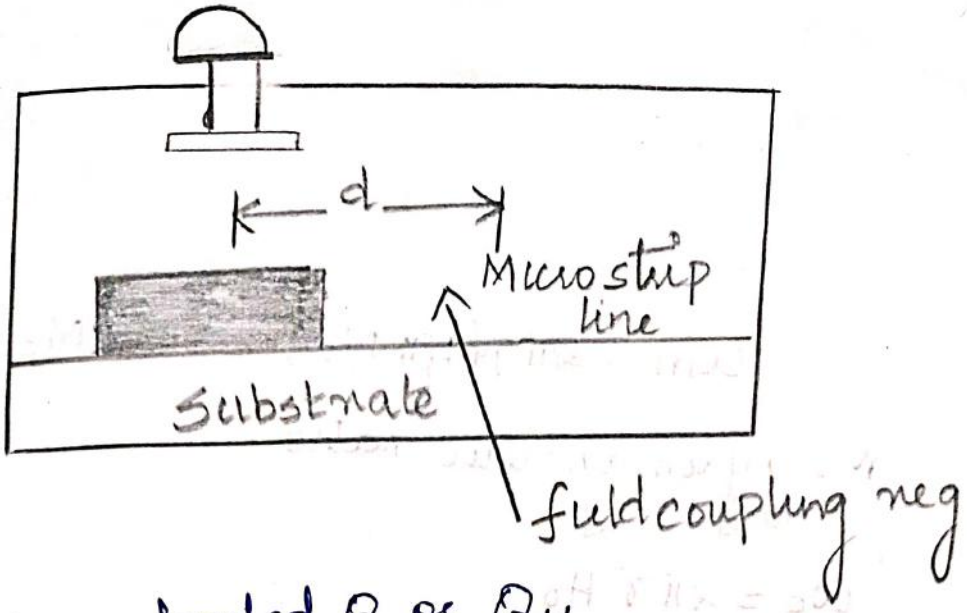
$$\Gamma_{out}\Gamma_L = 1.$$

FIXED - FREQUENCY OSCILLATORS.

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}}{1 - S_{11}\Gamma_S}\Gamma_S.$$



DIELECTRIC RESONATOR OSCILLATORS



The unloaded Q or Q_u

$$Q_u = \frac{R}{\omega_0 L} \doteq \omega_0 RC$$

the coupling coefficient β

$$\beta = \frac{R}{R_{ext}} = \frac{R}{2Z_0} = \frac{\omega_0 Q_u L}{2Z_0}$$

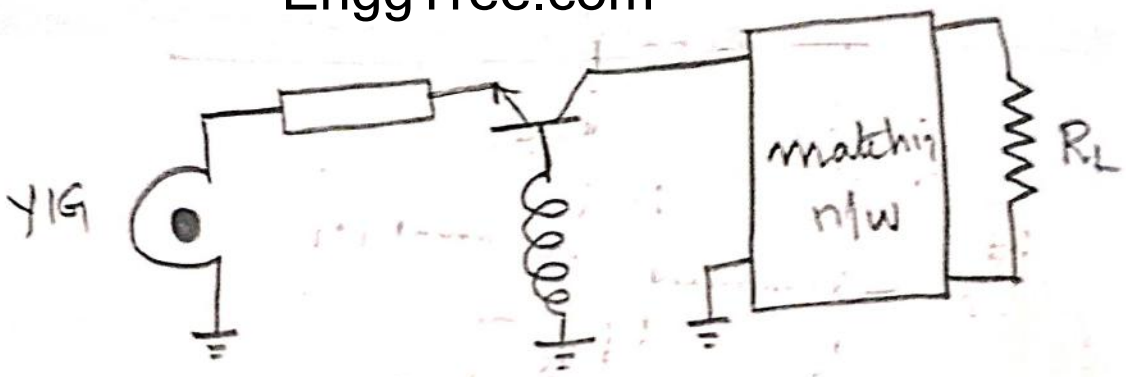
$$\omega_0 = 1/\sqrt{LC}$$

$$Q_u = \beta Q_E = (1+\beta) Q_L$$

YIG-TUNED OSCILLATOR.

The dielectric resonator allows tuning over a very narrow band, typically between 0.01 and 1%. such a tunable element, often of spherical shape called yttrium iron garnet (YIG)

$$Q_u = \frac{-H\pi(M_s/3) + H_0}{H_L}$$



$$\omega_m = 2\pi\gamma(H\pi M_s) = 8\pi^2\gamma M_s.$$

γ - gyromagnetic ratio

$$\omega_0 = 2\pi\gamma H_0$$

$$L_0 = \frac{\mu_0 \omega_m}{\omega_0 d^2}\left[\frac{4}{3}\pi a^3\right]$$

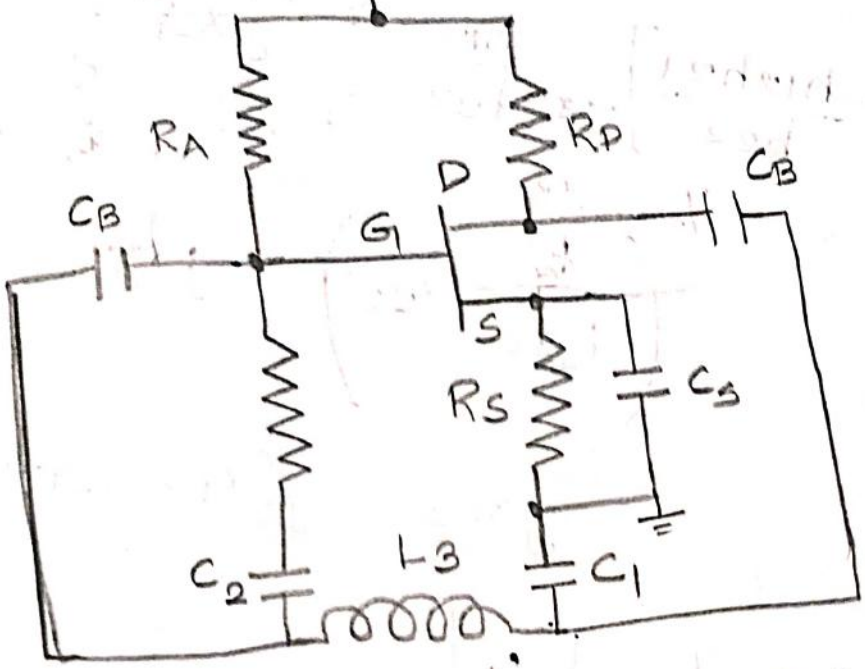
$$C_0 = L_0 \omega_0^2$$

Conductance

$$G_{10} = \frac{d^2}{\mu_0 \omega_m Q_u \left[\frac{4}{3}\pi a^3\right]}$$

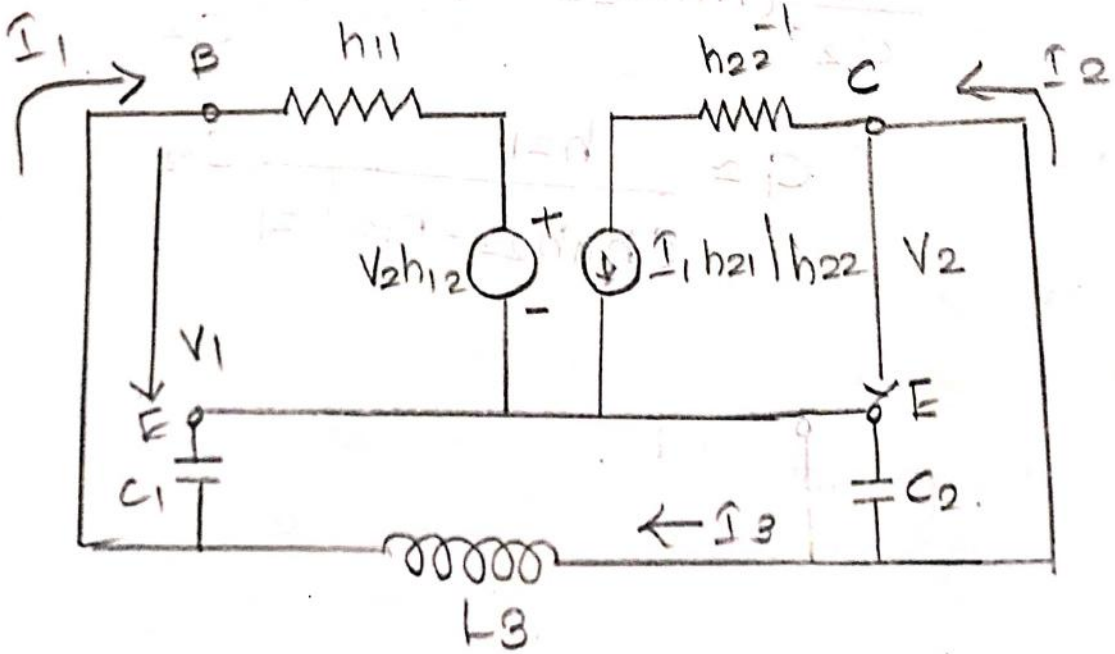
COLPITTS OSCILLATOR.

In colpitts oscillator realizations $X_1 = 1/\omega C_1$, $X_2 = 1/\omega C_2$ and $X_3 = \omega L_3$. where FET is active device. Here R_A R_B and R_D and R_S set the DC bias point. C_S is RF by pass capacitor and C_B is blocking capacitor.



DESIGN STEPS:

The h-parameter configuration with the appropriate feedback loop is as shown. The Kirchoff voltage mesh equations involving input, output and feedback loops are given as $V_2 = V_{out} = I_2/h_{22}$



$$\begin{bmatrix} h_{11} - jX_{C_1} - \frac{h_{12}h_{21}}{h_{22}} & \frac{h_{12}}{h_{22}} & jX_{C_1} \\ -\frac{h_{21}}{h_{22}} & \left(\frac{1}{h_{22}} - jX_{C_2}\right) & -jX_{C_2} \\ jX_{C_1} & -jX_{C_2} & j(X_{L_3} - X_{C_1} - X_{C_2}) \end{bmatrix}$$

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix}$$

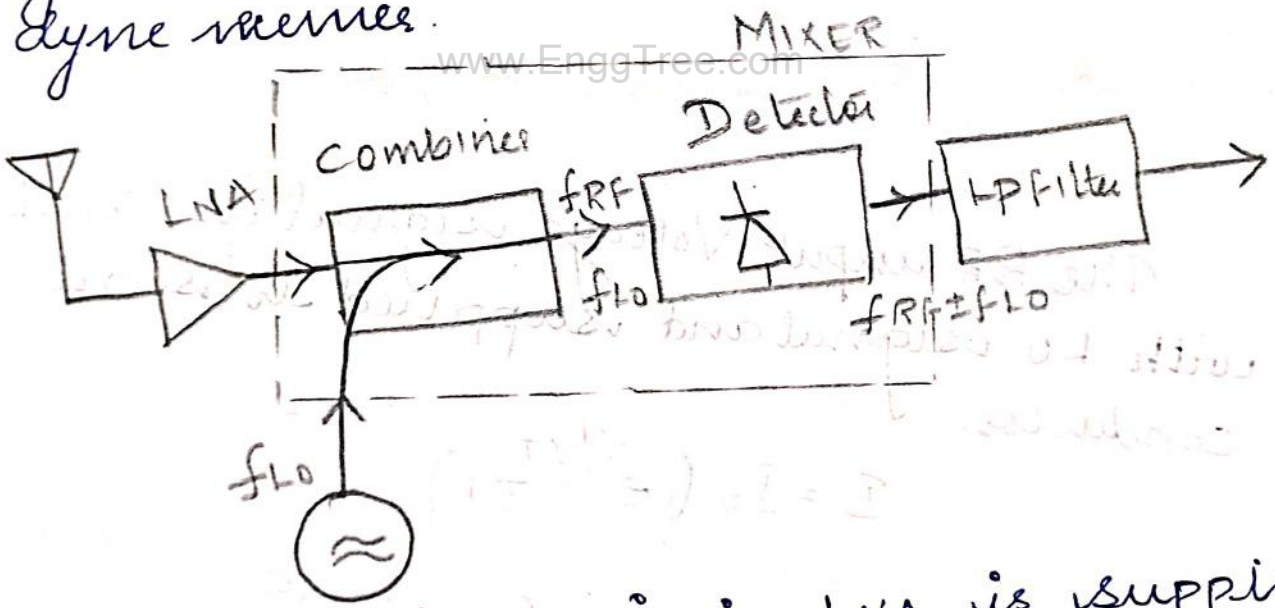
$$f = \frac{1}{2\pi} \frac{1}{\sqrt{C_1 C_2}} \sqrt{h_{22}/h_{11} + (C_1 + C_2)/L_3}$$

$$\frac{\omega^2}{C_2^2}(h_{11}h_{22} - h_{12}h_{21}) - \frac{C_1}{C_2}h_{21} + 1 = 0$$

$$C_1 \simeq \frac{h_{21}}{(h_{11}h_{22} - h_{12}h_{21})} C_2$$

BASIC CHARACTERISTICS OF MIXER

* Mixers are commonly used to multiply signals of different frequencies.
* A particular RF signal channel centered among many densely populated, narrowly spaced neighboring channels would require extremely high Q filters
* The task becomes much manageable if RF signal carrier frequency can be reduced or downconverted in this communication system. perhaps one of the best known system is downconversion in a hetero dyne receiver.

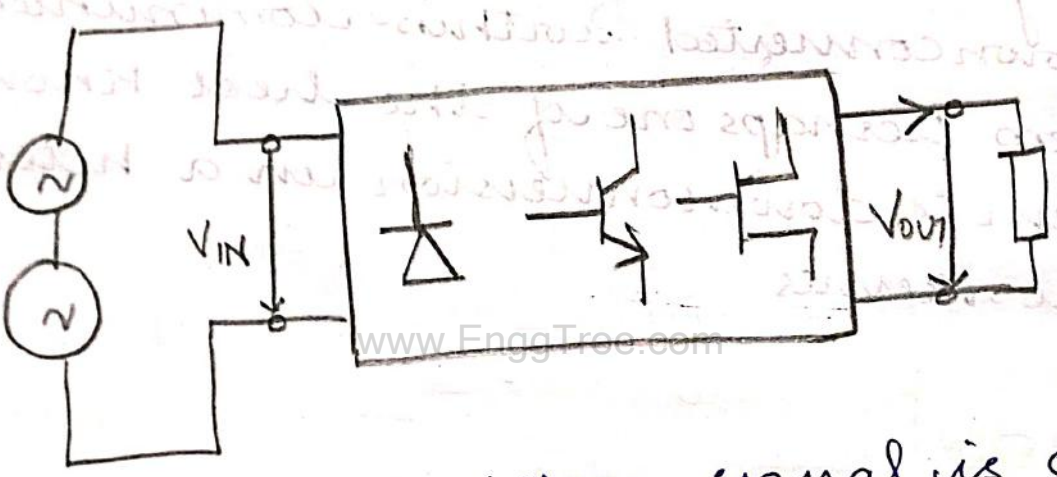


After preamplification in LNA, is supplied to a mixer whose task is to multiply the input signal of center frequency f_{RF} with with local oscillator (LO) frequency f_{LO}. The signal obtained after the mixer contains the frequencies $f_{RF} \pm f_{LO}$, of which after low pass filtering, the lower

frequency component $f_{RF} - f_{LO}$ known as intermediate frequency IF.

The combiner and detector are constituting the mixer. The combiner is implemented through 90° or (180°) directional coupler.

The mixer connected to an RF signal $V_{RF}(t)$ and local oscillator signal, $V_{LO}(t)$ known as pump signal.



The RF input voltage signal is combined with LO signal and supplied to semi-conductor.

$$I = I_0 \left(e^{V/V_T} - 1\right).$$

$$I(V) = I_{DSS}\left(1 - \frac{V}{V_{TO}}\right)^2.$$

The input voltage is sum of RF signal $V_{RF} = V_{RF}\cos(\omega_{RF}t)$ and LO signal $V_{LO} = V_{LO}\cos(\omega_{LO}t)$ and bias V_Q.

$$V = V_Q + V_{RF}\cos(\omega_{RF}t) + V_{LO}\cos(\omega_{LO}t$$

$$I(V) = I_Q + V\left[\frac{dI}{dV}\right]_{V_Q} + \frac{1}{2}V^2\left[\frac{d^2I}{dV^2}\right]_{V_Q} + \ldots = I_Q + V_A + V^2 B + \ldots$$

$$I(V) = A\{V_{RF}\cos(\omega_{RF}t) + V_{LO}\cos(\omega_{LO}t) + B\{V_{RF}^2\cos^2(\omega_{RF}t) + V_{LO}^2\cos^2(\omega_{LO}t)\}$$

$$I(V) = \ldots + BV_{RF}V_{LO}\{\cos[(\omega_{RF}+\omega_{LO})t] + \cos[(\omega_{RF}-\omega_{LO})t]\}.$$

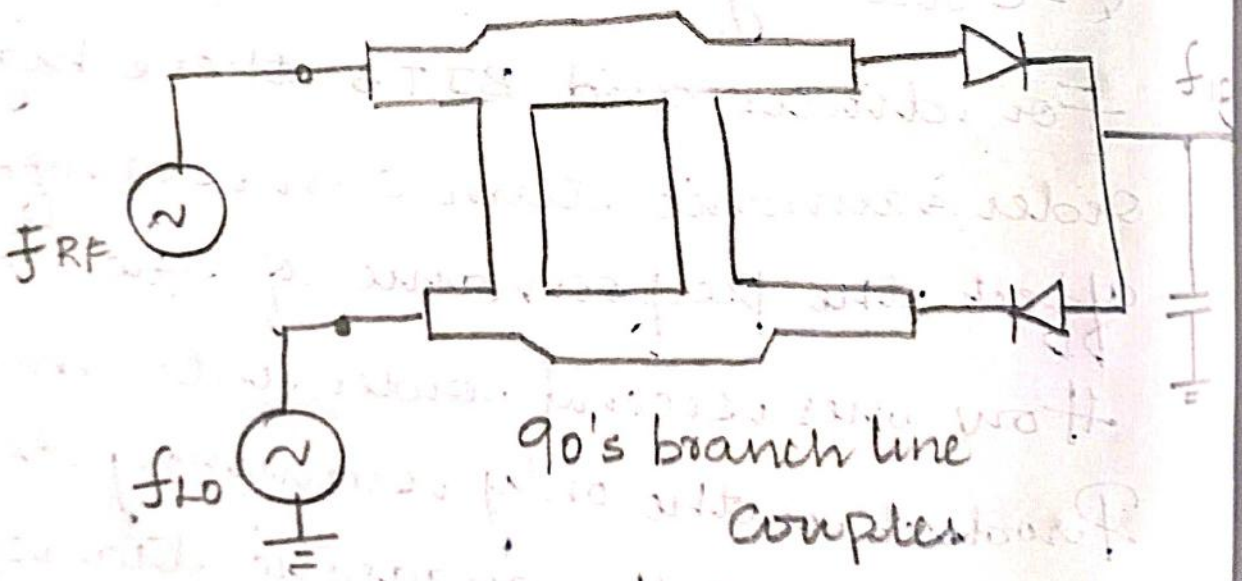
which is Taylor series upto third term and thus upto second order inter modular product (V^2B).

Any higher order products such as third order intermodular product V^3C are neglected.

For diodes and BJTs these higher order harmonic term can significantly affect the performance of the mixer However second order inter modular Product is the only occurring term if a FET with quadratic transfer Characteristic is utilised.

SINGLE - BALANCED MIXER

The main disadvantage of these designs is the difficulty associated with providing LO energy while maintaining isolation between LO, RF and RF signals for broadband applications. The balanced dual-diode or dual-transistor mixer in conjunction with hybrid coupler offers the ability to conduct such broad band operations and provides related noise suppression and spurious mode rejection. Spur arise in oscillators and amplifiers due to parasitic resonance.



90's branch line coupler.

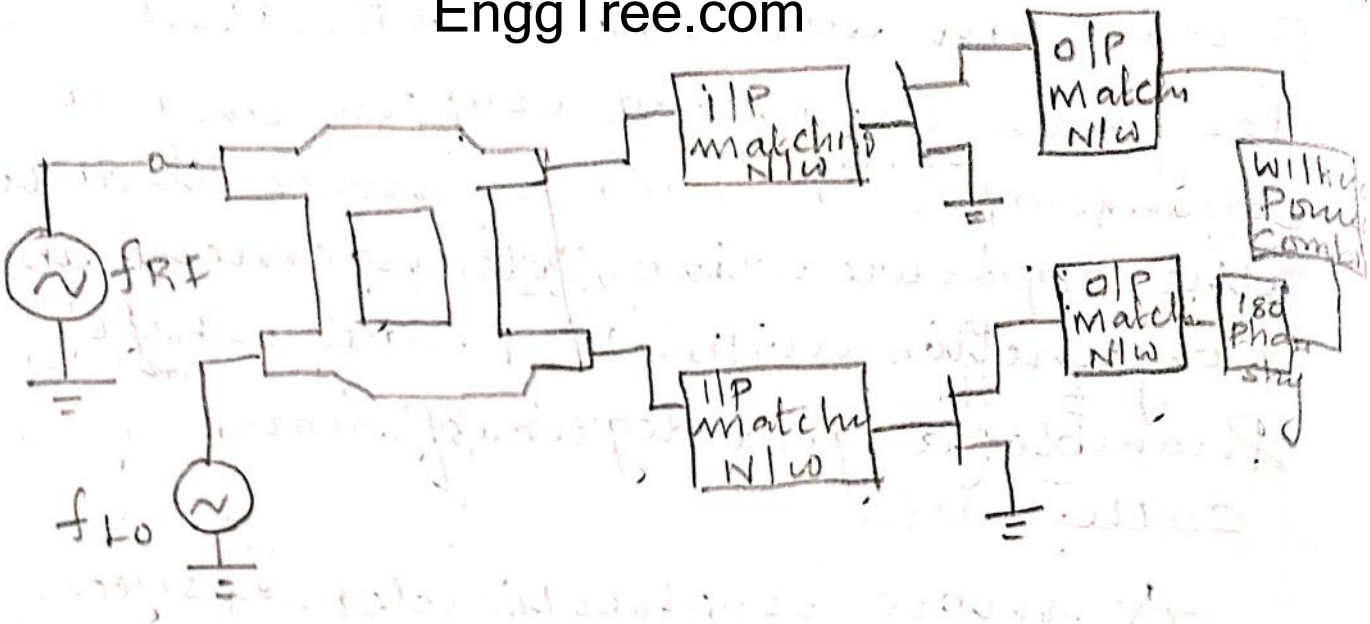
Balanced mixer employing hybrid coupler

Besides an equivalent VSWR, this design is capable of suppressing a considerable amount of noise because the opposite diode arrangement in conjunction with 90° phase shift provides a good degree of noise cancellation.

A more sophisticated design, with two MESFET and 90° and 180 hybrid coupler.

The 180° phase shift is needed since the second MESFET cannot be easily be reversed as done in anti-parallel diode configuration.

It is also important to point out that this circuit exhibits LO to RF as well as LO to IF signal isolation but no RF to IF signal isolation. For this reason, a low pass filter is typically incorporated into output matching network of each of transistor.



DOUBLE-BALANCED MIXER.

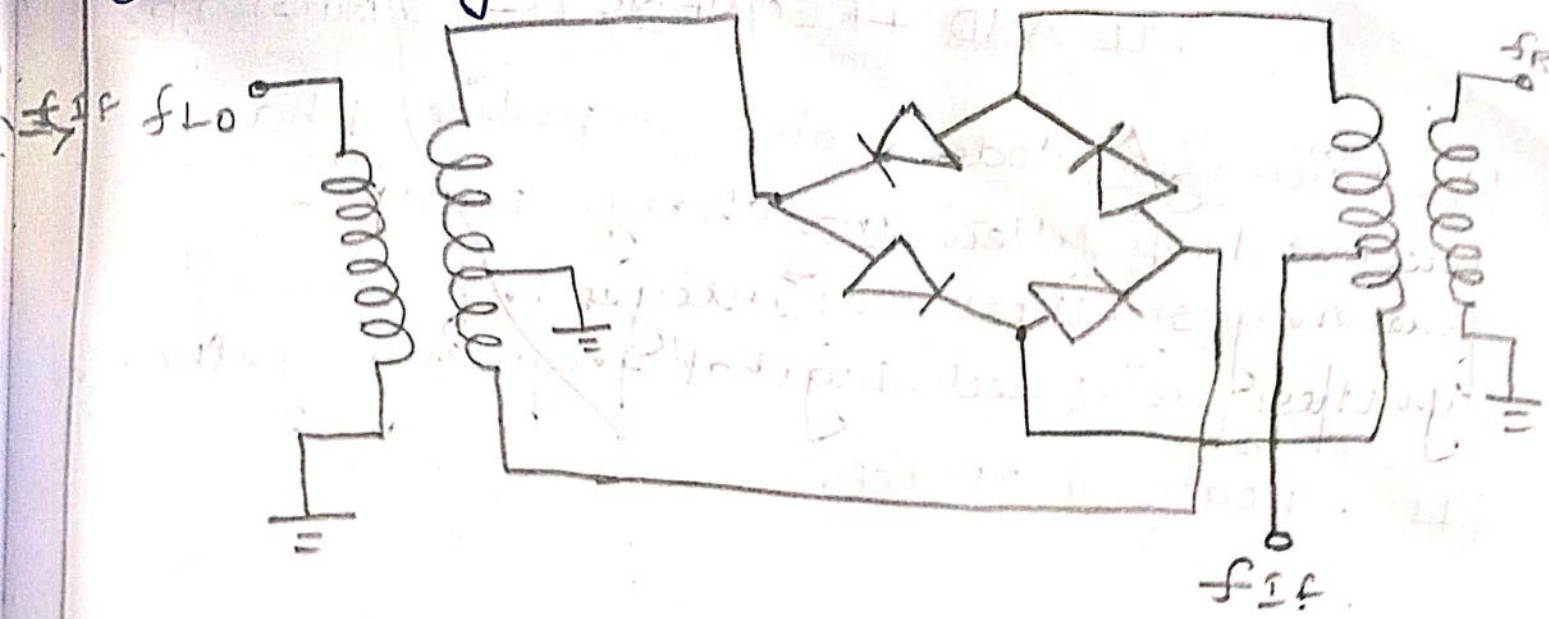
The double balanced mixer can be constructed by using four diodes arranged in rectified configuration. The additional diodes provides better isolation and an improved suppression of spurious modes.

unlike the single balanced approach, the double balanced design eliminates all even harmonics of both the LO and RF signals.

The disadvantages are higher LO drive power and increased conversion loss.

All three signals paths are decoupled and the input and output transformation enable a symmetric mixing with

signal.

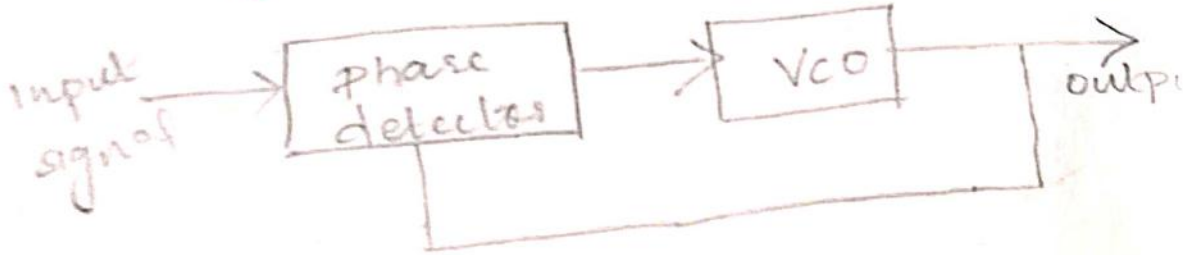


UNIT - V.

PLL AND FREQUENCY SYNTHESIZERS

PLL: Linearized Model, Noise properties, Phase detectors, Loop filters and charge pumps - frequency synthesizers: Integer-N frequency Synthesizers - Direct Digital frequency synthesis

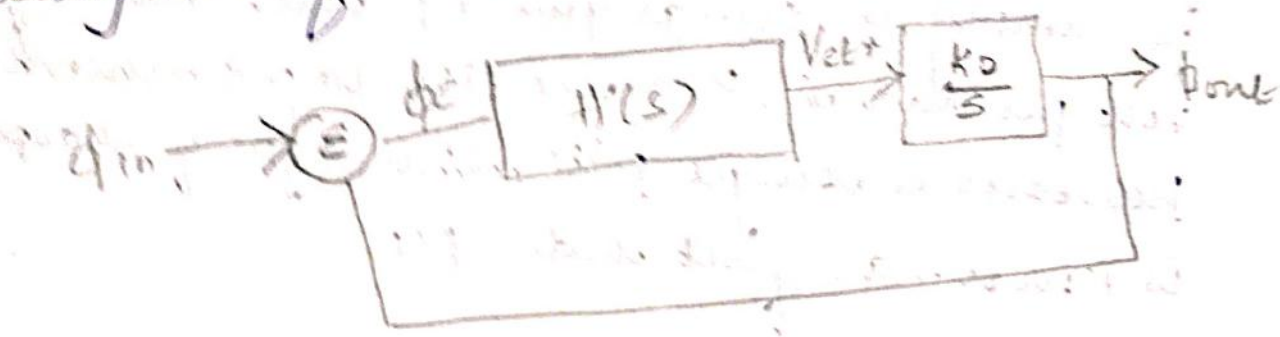
PLL: Linearized Model.



The basic PLL architecture consist of a phase detector and a Voltage Controlled Oscillator (VCO). The phase detector compares the phase of the incoming reference signal with that of VCO and produces and output that is some function of phase difference. The VCO simply generates a signal whose frequency is some function of control voltage.

The general idea is that the output of phase detector drives the VCO frequency in a direction that reduces the phase difference; that is the negative feedback system.

once the loop acquires lock, the phase of input reference and VCO output signal ideally have fixed phase relationship



The linearized PLL model as above. Because we are generally interested in phase relation between the input and output variables are phase in this model.

Another consequence of choosing Phase as input-output variable is that the VCO, whose output frequency depends on a control voltage is modelled as an integrator, since phase is the integral of frequency. The VCO gain constant K_0 has units of radians per second per volt.

The phase detector is modeled as simple subtractor that generates a phase error output ϕ_e that is the difference between the input and output phases. To accomodate gain scaling factors and the option of additional filtering in loop, a block with transfer function H(s) is included

FIRST-ORDER PLL

The simple PLL is one in which H(s) is simply a scalar gain K_D with unit of Volt per radian. Because the loop transfer... Possesses a single pole, this type of loop is known as first order PLL.

$$\frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{K_0 K_D}{s + K_0 K_D}$$

The closed loop bandwidth is

$$\omega_K = K_0 K_D.$$

$$\frac{\phi_e(s)}{\phi_{in}(s)} = \frac{s}{s + K_0 K_D}$$

We assume input signal is a constant frequency sinusoid of frequency ω_i, then the phase ramps linearly with time at rate of ω_i radians per second.

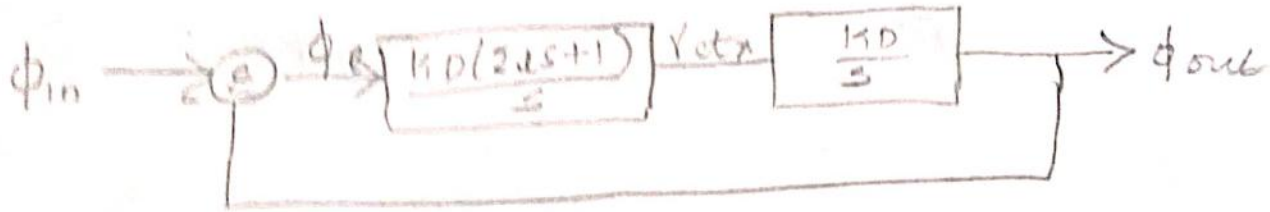
By Laplace domain representation of input signal is

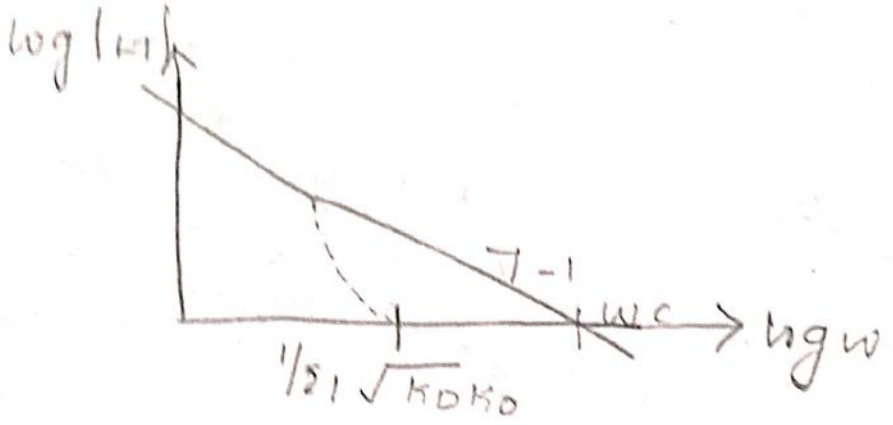
$$\phi_{in}(s) = \frac{\omega_i}{s^2}$$

$$\phi_e(s) = \frac{\omega_i}{s(s + K_0 K_D)}$$

By steady state error with constant frequency input is

$$\lim_{s \to 0} s\phi e(s) \cdot \frac{\omega i}{K_0 K_D} = \frac{\omega i}{\omega h}.$$





SECOND-ORDER PLL.

In this model the, constant K_D has units of volts per second because of extra integration.

As the loop transmission magnitude increases, the loop become progressively better damped because an increase in cross over frequency allows more of the zero's positive phase shift of negative phase shift of poles.

For very large loops transmission, one closed loop pole end up at nearly the frequency of the zero, while the other

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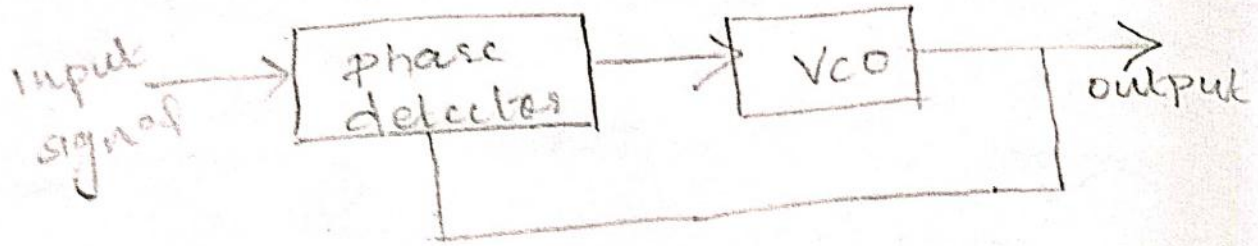

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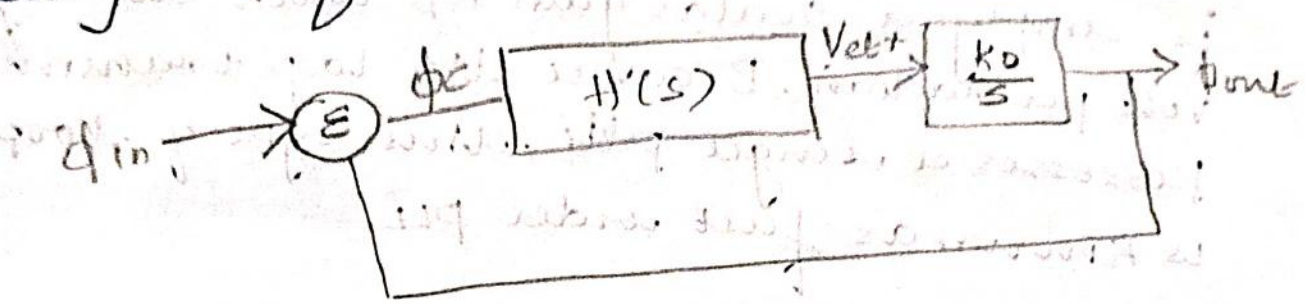

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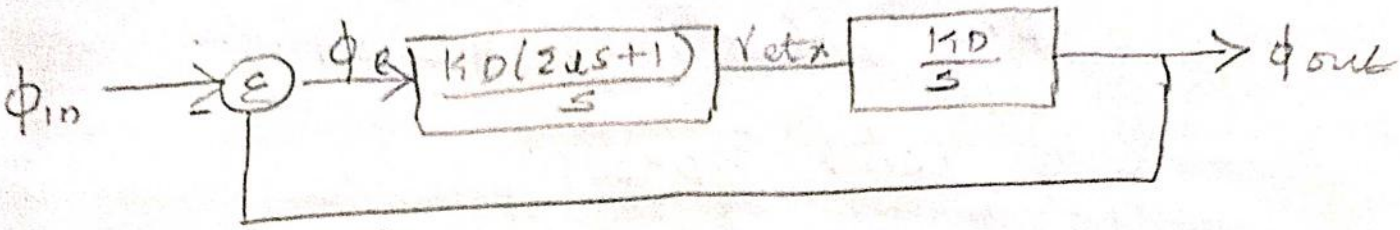

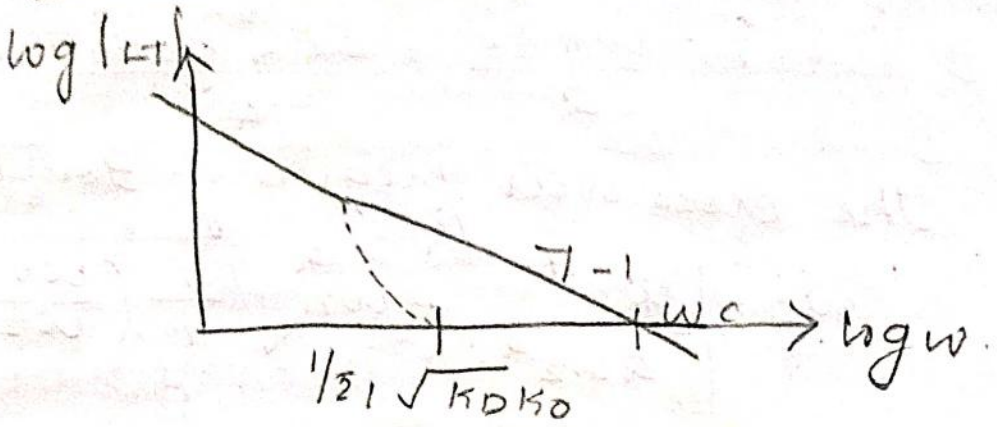

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For very large loops transmissions, one closed loop pole end up at nearly the frequency of the zero, while the other

poles heads for infinitely large frequen

It is straightforward to show that

Phase transfer function is

$$\frac{\phi_{out}}{\phi_{in}} = \frac{2\zeta s+1}{(s^2/K_D K_0)+2\zeta s+1}$$

$$\omega_n = \sqrt{K_D K_0}$$

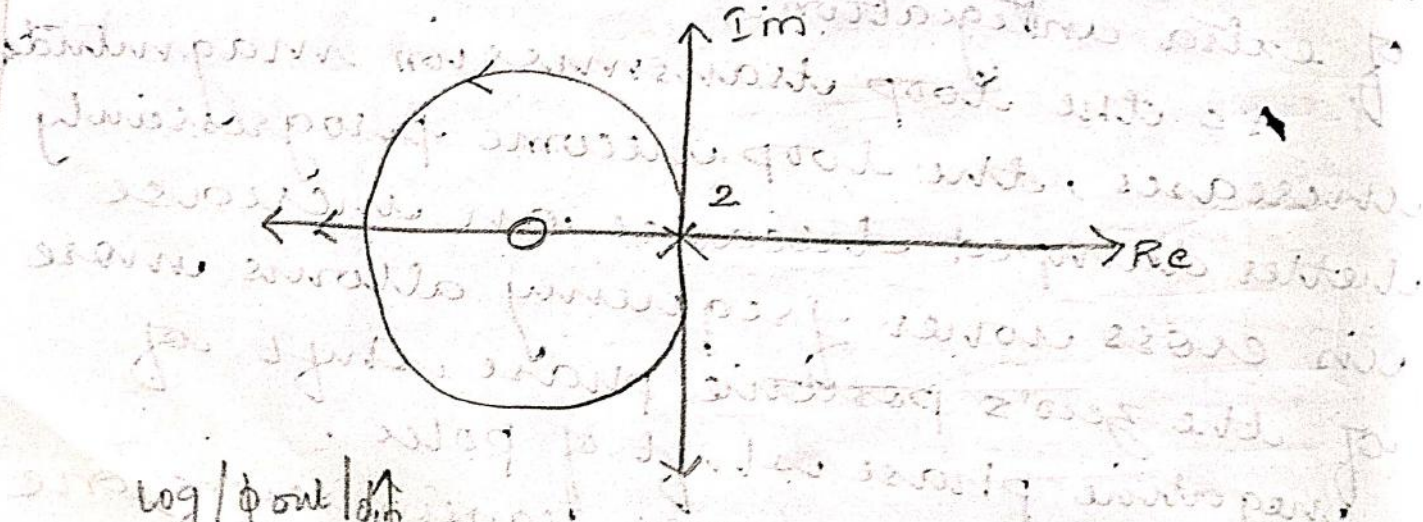
$$\zeta = \frac{\omega_n \tau_2}{2} = \frac{\tau_2 \sqrt{K_D K_0}}{2}$$

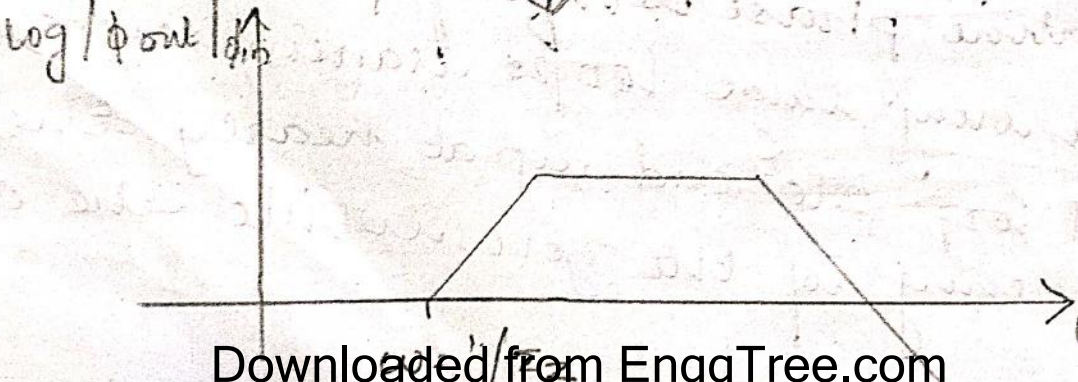
The cross over frequency for loop is

$$\omega_c = \left[\frac{\omega_n^4}{2\omega_z^2} + \omega_n^2 \sqrt{\frac{1}{4}\left(\frac{\omega_n}{\omega_z}\right)^4 + 1}\right]^{1/2}$$

$$\omega_c \simeq \frac{\omega_n^2}{\omega_z}$$

Jitter peaking in second order PLL





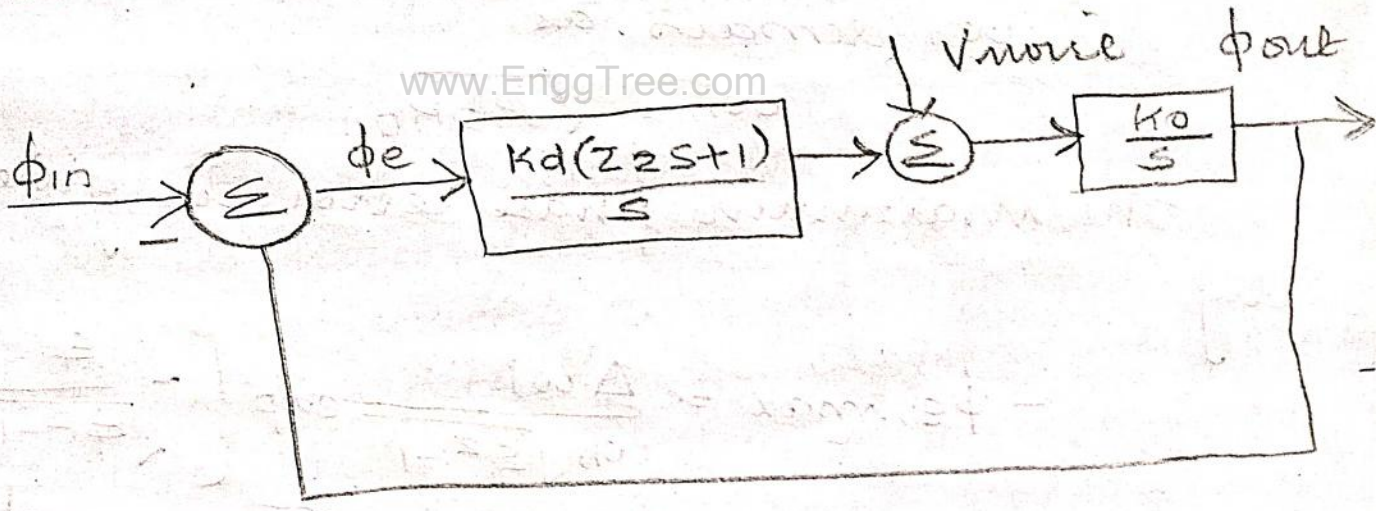
From Root locus, we see that zero is to right of pole at larger damping ratio hence the closed loop frequency response initially exceeds unity until zero's effect is cancelled by poles.

The frequency rise as starting at zero location and flattening cause by first pole.

The phase transfer function has magnitude greater than unity above zero frequency until second pole introduces sufficient roll off.

SOME NOISE PROPERTIES OF PLL's.

REJECTION OF VCO DISTURBANCES.



Consider noise as additive at the control port of the VCO. It is a relatively straight forward exercise to show that noise to phase error transfer function is

$$-\frac{\phi_\varepsilon}{V_N} = \frac{SK_0}{S^2 + SZ_2K_DK_0 + K_DK_0}$$

Assuming unit step - function noise input inverse laplace - transforming gives us the resulting phase error as function of time.

$$-\phi_\varepsilon(t) = \frac{\Delta w_i}{w_n\sqrt{\xi^2-1}} \exp(-\xi w_n t)\sinh\left(w_n\sqrt{\xi^2-1}\,t\right)$$

Δw_i - initial frequency error due to step function disturbance VN. The damping ratio ξ of closed loop poles is given by.

$$\xi = \frac{w_n \tau_2}{2}.$$

w_n remains as

$$w_n = \sqrt{K_D K_0}.$$

The maximum phase error is given by

$$-\phi_{\varepsilon,max} = \frac{\Delta w_i}{w_n\sqrt{\xi^2-1}} \exp\left[-\frac{\xi}{\sqrt{\xi^2-1}}\tanh^{-1}\frac{\sqrt{\xi^2-1}}{\xi}\right] \cdot \sinh\left(\tanh^{-1}\frac{\sqrt{\xi^2-1}}{\xi}\right)$$

occurs at a time

$$t_{max} = \frac{1}{w_n\sqrt{\xi^2-1}}\tanh^{-1}\frac{\sqrt{\xi^2-1}}{\xi}.$$

$$-\phi_{\varepsilon,max} \simeq \frac{\Delta\omega_i}{\omega_c}$$

$$t_{max} \simeq \frac{2\ln 2\varepsilon}{\omega_c}$$

ω_c is cross over frequency of loop.

REJECTION OF NOISE ON INPUT.

The bandwidth of PLL helps to minimize the influence of disturbances that alter the VCO frequency.

However, there is a potential draw back to maximizing the bandwidth, above and beyond the stability issues.

As the loop bandwidth increases, the loop gets better at tracking the input. If the input is noise-free, then there is a net improvement overall.

However if the input signal is noisier than the PLL's VCO, then the high-bandwidth loop will faithfully reproduce this input noise at the output.

Hence there is a trade off between sensitivity to noise on the input to the loop and sensitivity to noise that disturb the VCO frequency.

In general, tuned oscillators are inherently are less noisy.

PHASE DETECTORS:

THE ANALOG MULTIPLIER AS A PHASE DETECTOR:

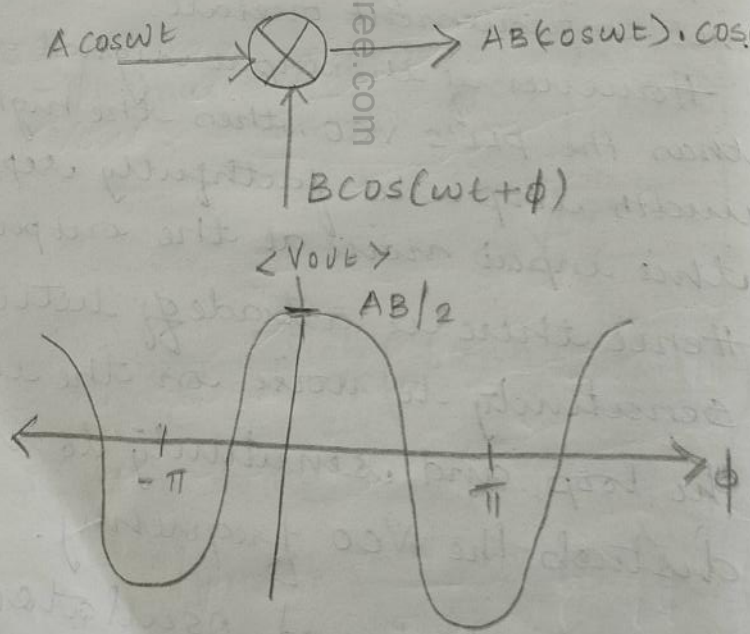
In PLLs that have sine-wave input and sine wave VCOs, the most common Phase detector is the multiplier first used with Gilbert-type topology.

The output of multiplier may be expressed as.

$$AB\cos\omega t\cos(\omega t+\phi)$$

$$=\frac{AB}{2}[\cos(\phi)-\cos(2\omega t+\phi)]$$

which is consisting of DC term and double frequency term for phase detector we are interested only in DC term.



gain 'constant' is a function of phase angle and is given by.

$$K_D = \frac{d}{d\phi}(V_{out}) = -\frac{AB}{2}[\sin(\phi)]$$

* The output is periodic.
* The phase detector gain constant is zero when the phase difference is zero and is greatest when the input phase difference is 90°.
* To maximize the useful phase detection range, the loop should be arranged to lock to a phase difference of 90°. and a multiplier is often called as quadrature phase detector.
* when loop is locked in quadrature the phase detector increase gain by.

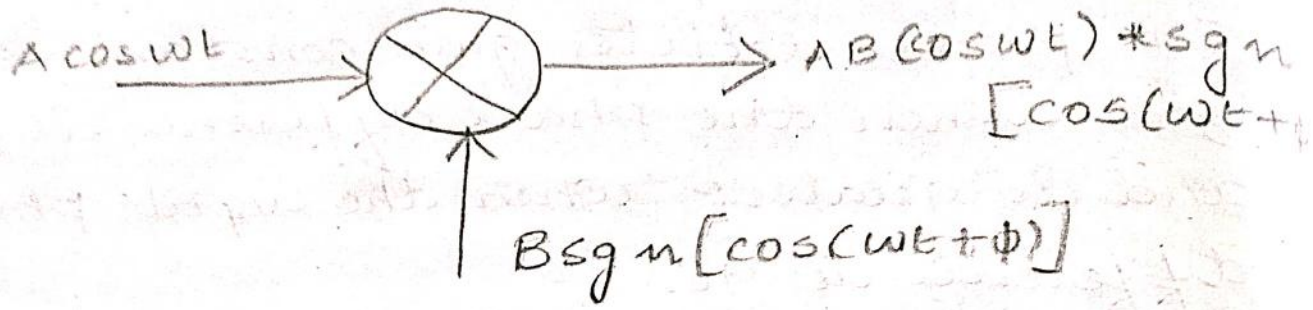
$$K_D|_{\phi=\pi/2} = \frac{d}{d\phi} V_{out}\Big|_{\phi=\pi/2}$$

$$= -\frac{AB}{2}$$

* Because there are two phase angles the result in zero output from the Phase detector; there would be two equilibrium points to which the loop could lock. one of point is stable equilibrium and other is metastable only one corresponds to negative feedback.

THE COMMUTATING MULTIPLIER AS A PHASE DETECTOR

We assumed in previous cases that both inputs to loop were sinusoidal. Here one of both of inputs may be a square wa



$$sgn(x) = 1 \quad \text{if } x > 0$$
$$sgn(x) = -1 \quad \text{if } x < 0.$$

we assum only the fundamental component of square wave, which is amplitude is $4B/\pi$.

The average output of multiplier is

$$\langle V_{out} \rangle = \frac{4}{\pi} \frac{AB}{2} [\cos(\phi)]$$

$$= \frac{2}{\pi} AB [\cos(\phi)].$$

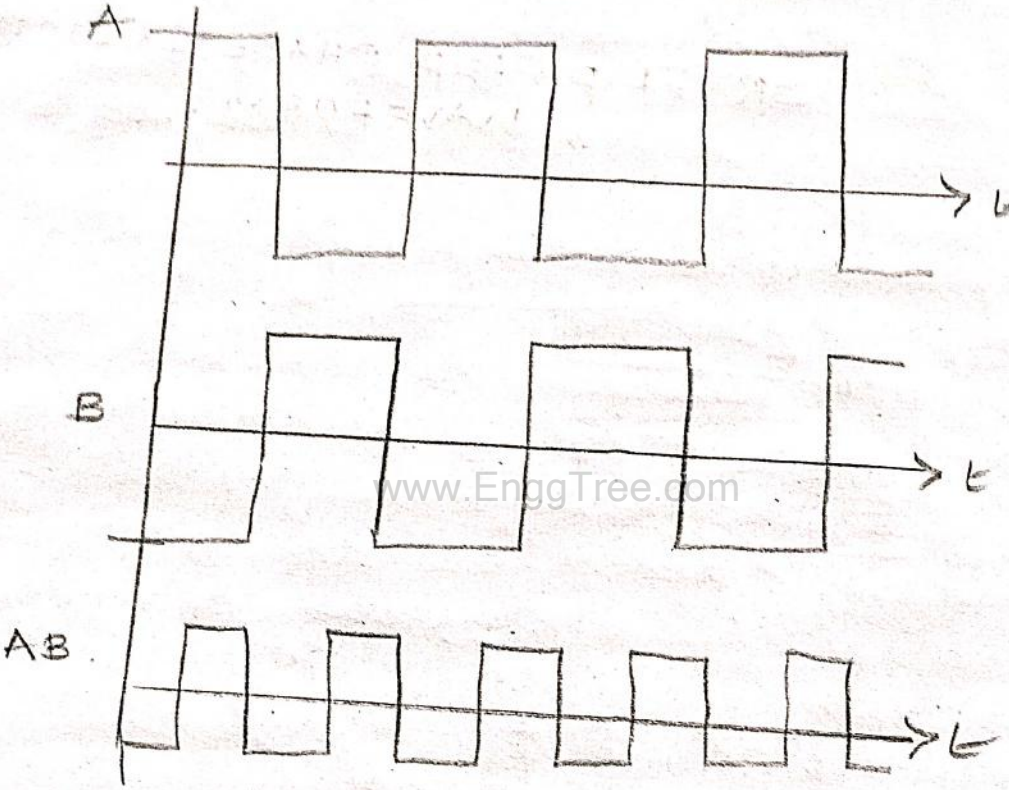
The phase detector gain is just H/π larger as in sinusoidal case:

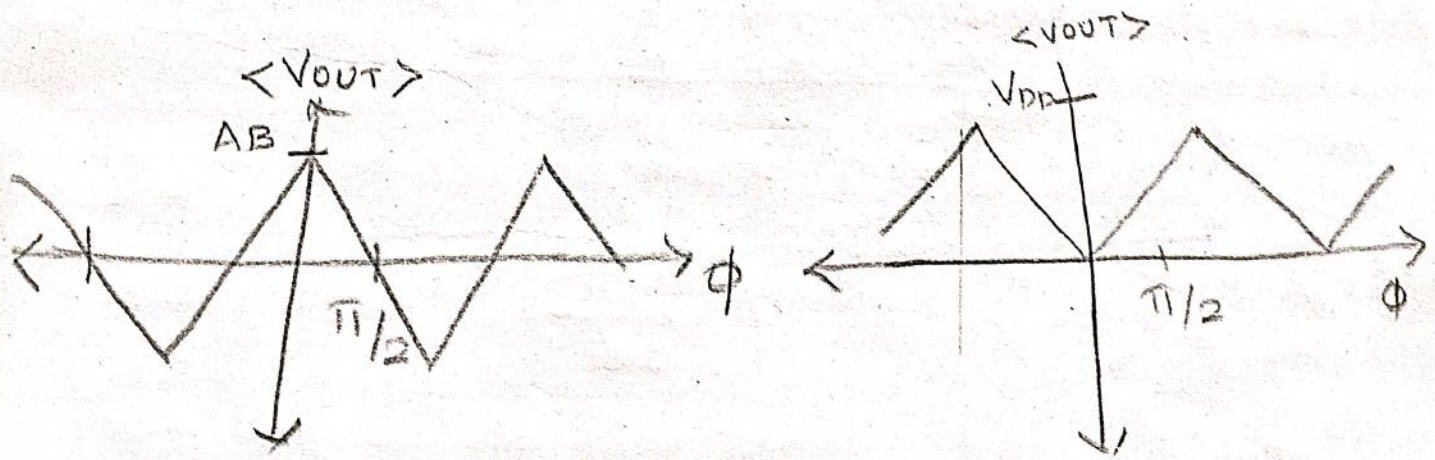
$$K_D|_{\phi = \pi/2} = \frac{d}{d\phi} \langle V_{out} \rangle \Big|_{\phi = \pi/2}$$

$$= \frac{2AB}{\pi}$$

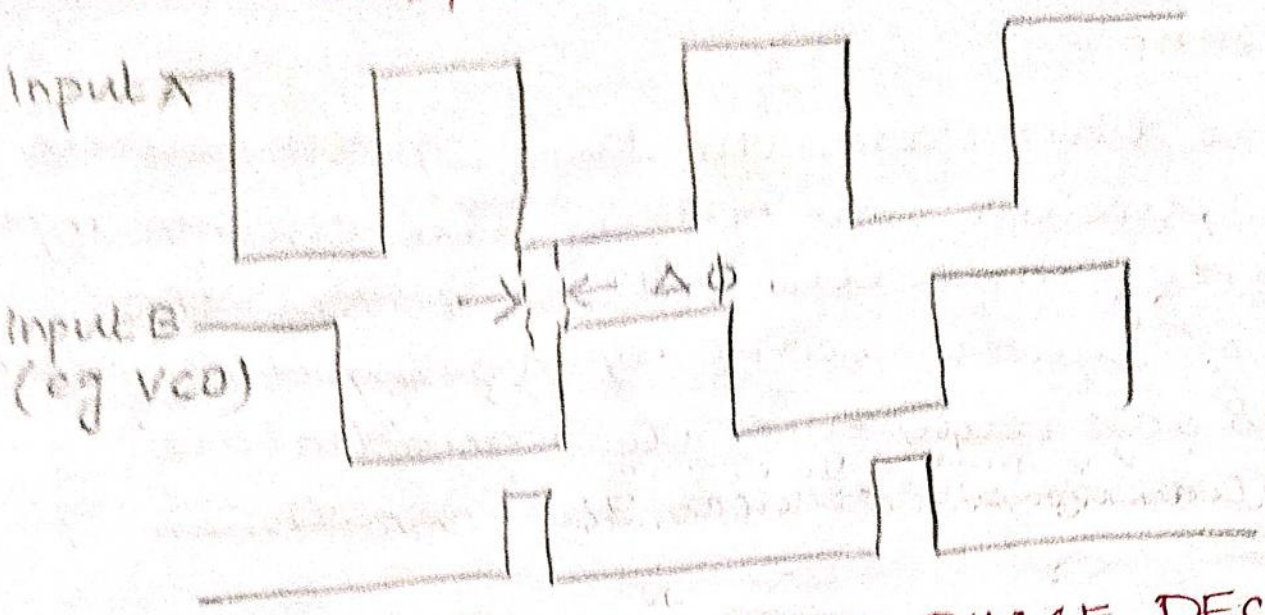
THE EXCLUSIVE -OR GATE AS A PHASE DETECTOR

In this case, the two square-wave inputs produce output as we change input phase difference, the output takes the form of square wave of varing duty cycle with 50% duty cycle to a quadrature relationship between the inputs

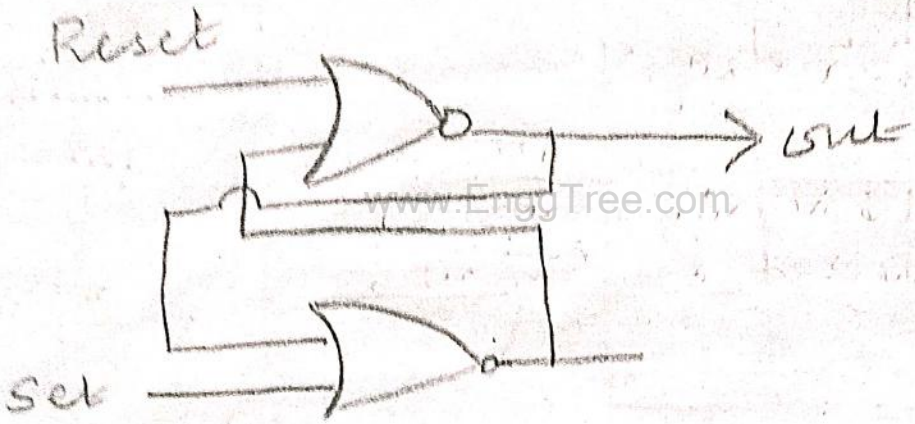


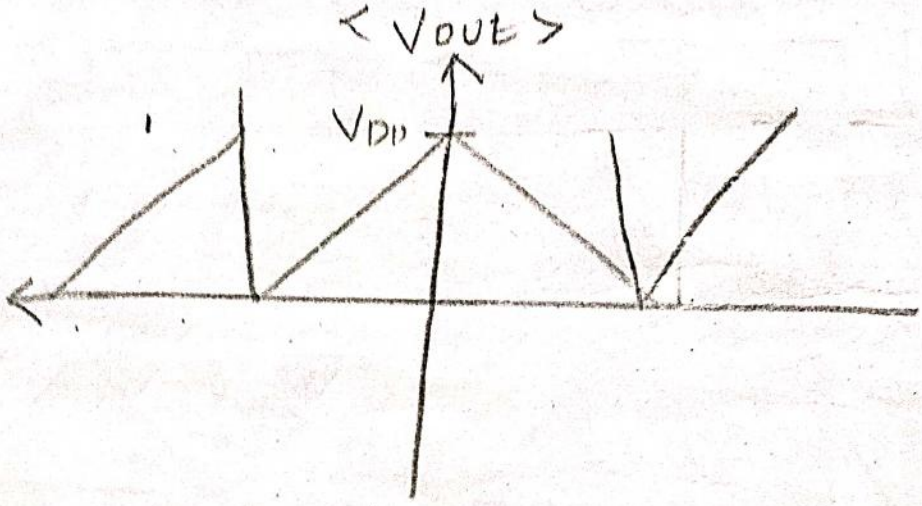


SEQUENTIAL PHASE DETECTORS :



SR FLIP FLOP PHASE DECTOR WAVEFORM.

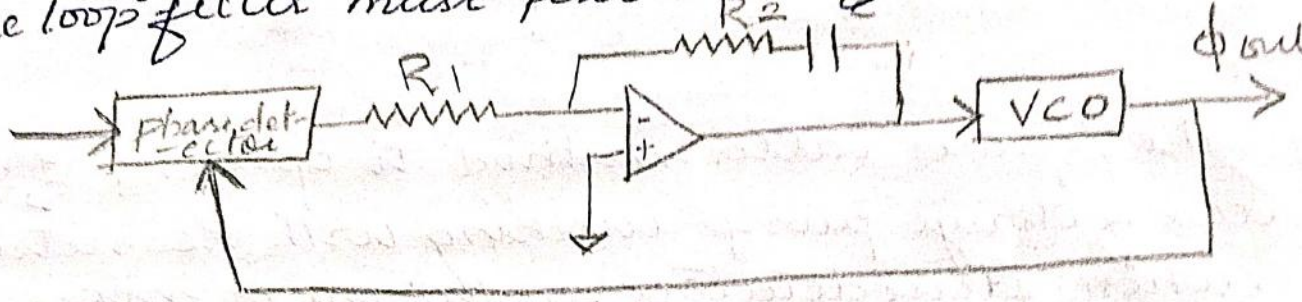


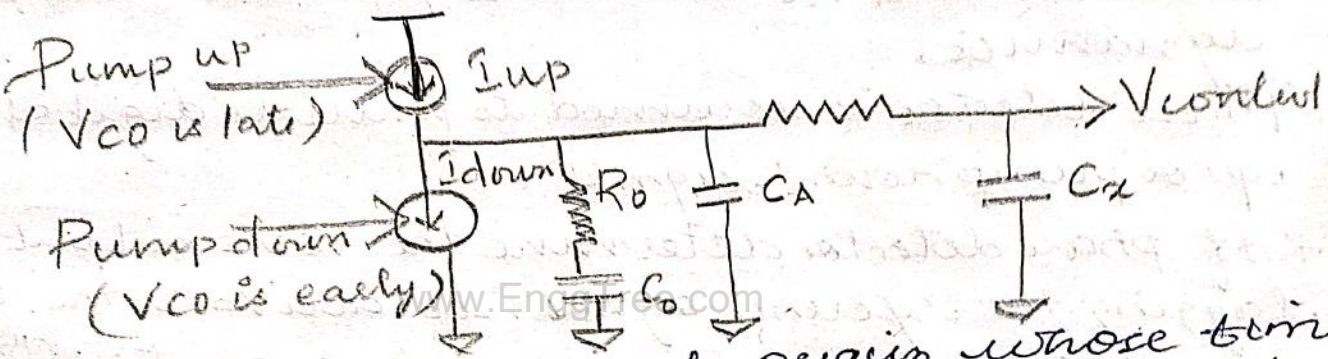


LOOP FILTERS AND CHARGE PUMPS:

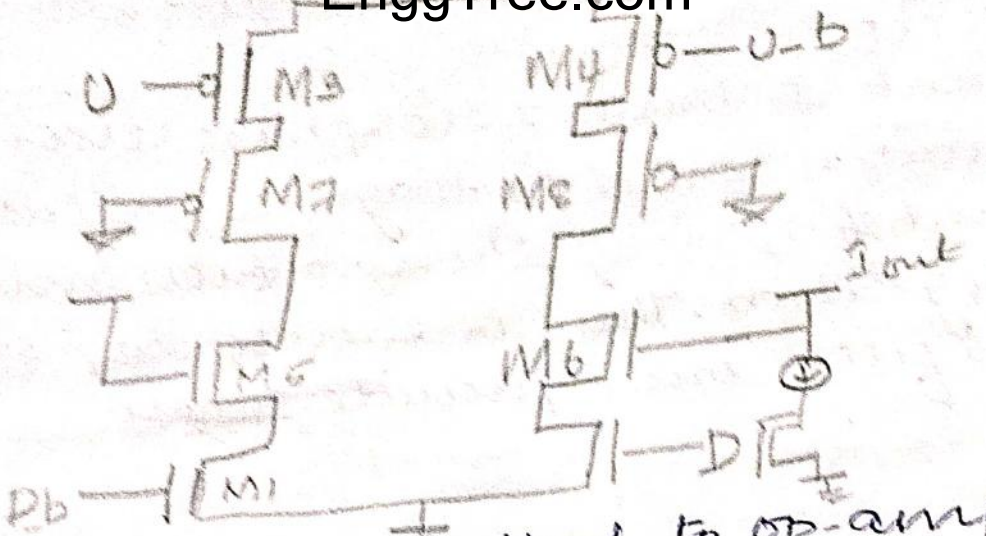
LOOP FILTERS:

we want to have zero phase error in lock. VCO requires control voltage to produce output of desired frequency, the loop filter must provide an integration. Then to ensure loop stability the loop filter must provide a zero.





* we have pole and zero at origin whose time constant is R2C. The value of R1 is adjusted to provide loop transmission magnitude.
* A RC network use to connect phase detector with VCO, where static phase error is not zero and loop band width is coupled to static phase error and used only in critical applications.
* The circuit is used in discrete implementation, but a different approach is used in most IC's.
* A considerable reduction in complexity and area can be obtained by using an element that is less general-purpose than an op-amp.



The popular alternative method to op-amp filter is use of charge pump working with RC network where phase detectors control one or more current sources and RC networks provides loop dynamics.

Phase detector is assumed to provide digital 'pump up' or 'pump down' signal.

* If phase detector determine the VCO's output is lagging the reference signal, it activates the top current source, sending charge to capacitor ("pump up). If the VCO is ahead, the bottom current source is activated with drawing charge from capacitor ('pump down').

* If there is no Resistor Ro, then we would have pure integration. As usual the series resistor provide loop-stabilising zero by forcing the high frequency asymptotic impedance to non-zero value. The pump current is given by

$$I = I_{pump} \frac{\Delta\phi}{2\pi}.$$

Transistor M1 and M4 through are dyfa switches operated by up and down commands from phase detector. Depending on state of com mands either source current Ipump or sink

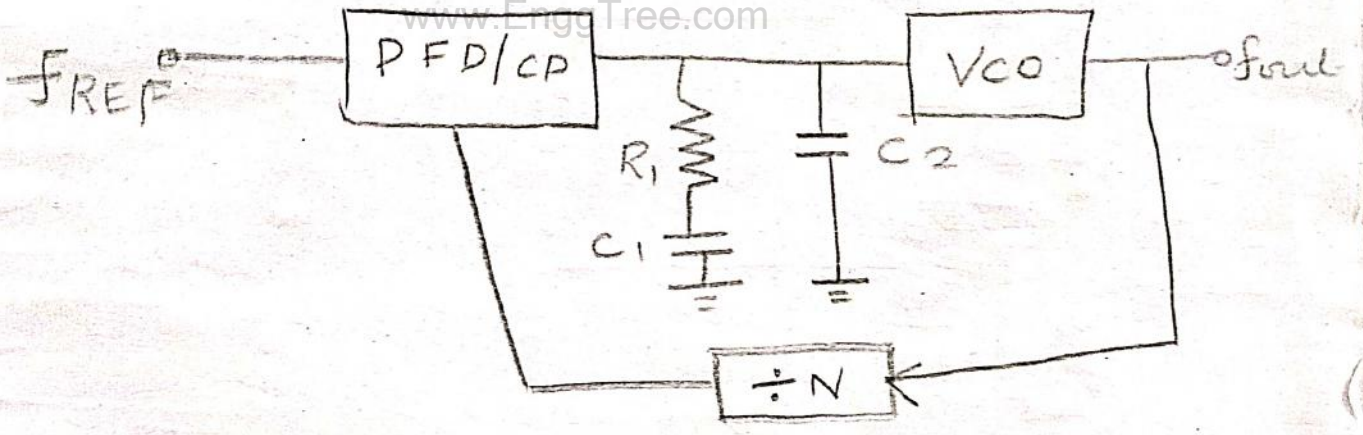
current I_{down} is steered to the output node Op. Thus I_{out} equals I_{up} or I_{down} depending on phase detector state.

FREQUENCY SYNTHESIZER:

N FREQUENCY SYNTHESIZER

BASIC INTEGER N-SYNTHESIZER

Integer-N synthesizes produce an output frequency which is an integer multiple of reference frequency. if N increases by 1 then fout increases by f_{REF} i.e; the minimum channel spacing is equal to the reference frequency.

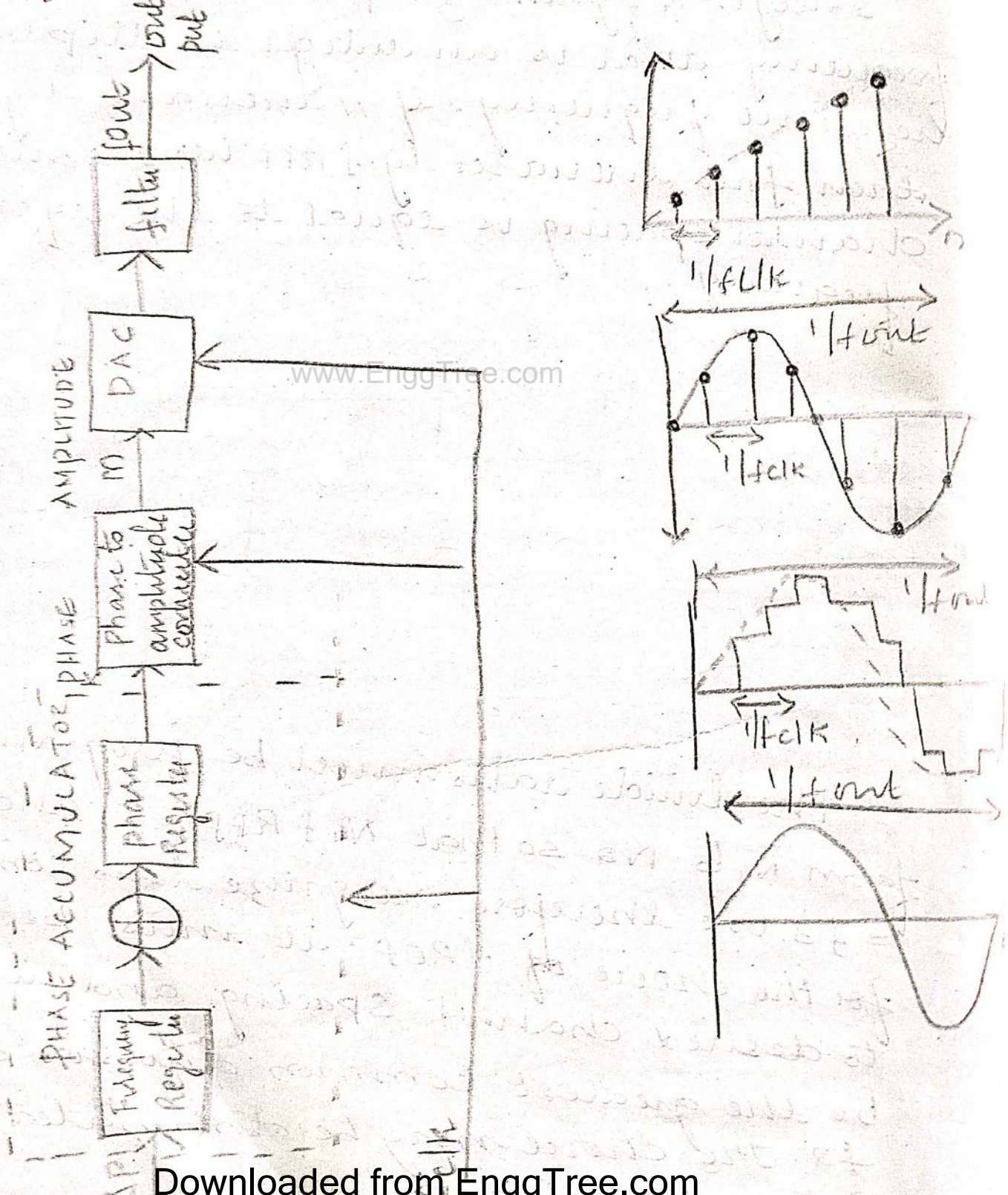


The divide ratio must be programmable from N_1 to N_2 so that $N_1 f_{REF} = f_1$ and $N_2 f_{REF} = f_3$. We therefore recognize two conditions for the choice of f_{REF}: it must be equal to desired channel spacing and it must be the greatest common divisor of f_1 and f_2. The choice may be dominated by one of two conditions

Eg: the minimum channel spacing may be smaller than the greatest common divisor of f1 and f2.

The simplicity of integer-N synthesizer makes an attractive choice. Behaving as a standard PLL.

DIRECT DIGITAL FREQUENCY SYNTHESIZER



* DDFS is a method of producing an analog waveform usually a sine wave by generating a time varying signal in digital form and then performing a digital to analog conversion.

* The operation within DDFS device are primarily digital, therefore it can offer fast switches between output frequencies fine frequency resolution and operation over a broad spectrum of frequencies.

* The digital frequency synthesis employ a stable frequency (ie) reference clock to define times at which digital sinusoidal sample values are produced.

* These samples are converted from digital to analog format and smoothed by reconstruction filter to produce analog frequency signal.

* A DDFS consist of phase Accumulator and a sine lookup table.

* The input to phase accumulator is frequency control word, which determines the periodicity of phase accumulator.

* The PA is updated to frequency word or tuning word at each clock.

the output is fed to LUT then converted to analog signal using DAC.