EC3353 - Electronic Devices and Circuits

Unit - I

Semiconductor Devices.

PN - junction diode, Zener diode, BJT, MOSFET, UJT - Structure, operation and VI characteristics, diffusion and transition Capacitance — Rectifiers — Half wave and Full wave Rectifiers, Zener as regulator.

PART - A

1. Define Static and Dynamic resistance of PN Diode.

Static resistance :-

It is resistance of PN junction diode used in d.c. circuit.

It is denoted by R_{Static}

$$R_{Static} = \frac{\text{D.C Voltage}}{\text{D.C Current}} = \frac{V_{dc}}{I_{dc}}$$

Dynamic resistance :-

It is resistance of PN junction diode used in a.c. circuit

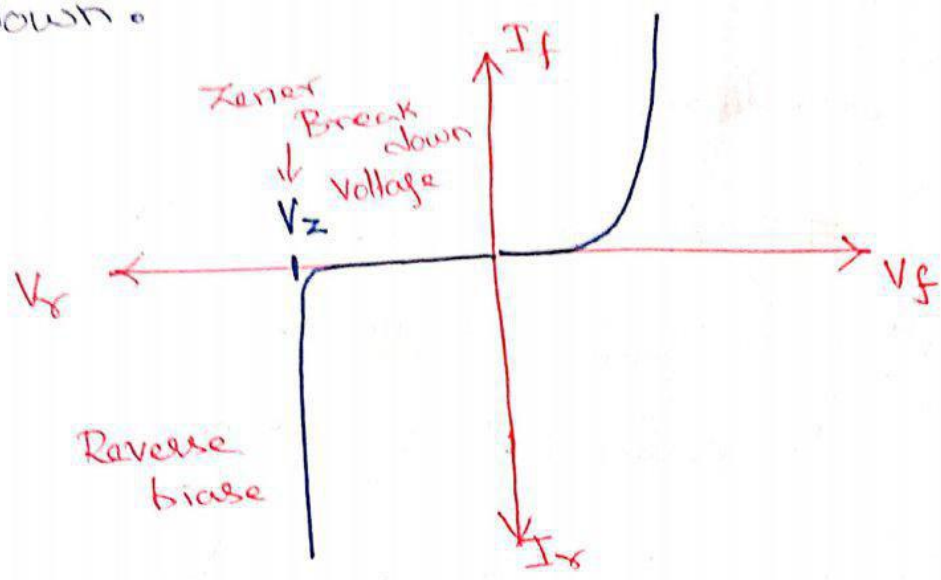
It is denoted by $R_{Dynamic}$

$$R_{dynamic} = \frac{\text{A.C. Voltage}}{\text{A.C Current}} = \frac{\Delta V_{ac}}{\Delta I_{ac}}$$

2. What is meant by Zener breakdown?

When a PN junction is heavily doped the depletion region is very narrow; under

reverse bias condition the minority carriers penetrate into narrow depletion region cause breakdown called Zener break down.



3. Define ripple factor.

It is defined as the ratio of R.M.S value of the a.c. Component to the average (or) d.c. Component. It is denoted by γ

$$\gamma = \frac{\text{R.M.S. a.c. Component}}{\text{Average (or) d.c. Component}} = \frac{I_{ac}}{I_{dc}}$$

4. what are the applications of UJT?

* It is used for triggering SCR
* It as Sawtooth wave generator
* Used as Relaxation oscillator

5. Define the Diffusion Capacitance. C_D

It is the forward bias Capacitance due to depletion region of PN diode. It is denoted by C_D

$$C_D = \frac{dQ}{dV} = \frac{\tau I}{\eta V_T}$$

6. Define the Transition Capacitance. C_T

It is the reverse bias Capacitance due to depletion region of PN junction diode. It is denoted by C_T

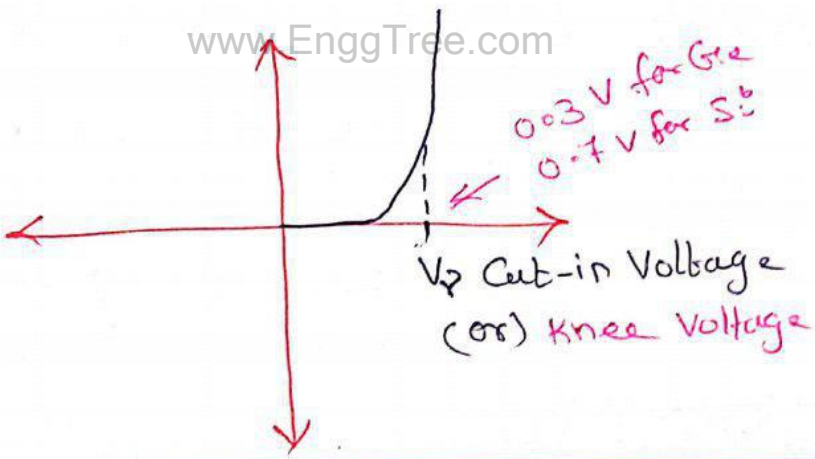
$$C_T = \frac{dQ}{dV} = \frac{\varepsilon A}{W}$$

7. Define Knee Voltage (or) Cut-in Voltage of a diode.

It is forward bias Voltage at which the depletion region Vanish and Start Conducting is called Knee Voltage (or) Cut-in Voltage

For Ge = 0.3 Volts

For Si = 0.7 Volts

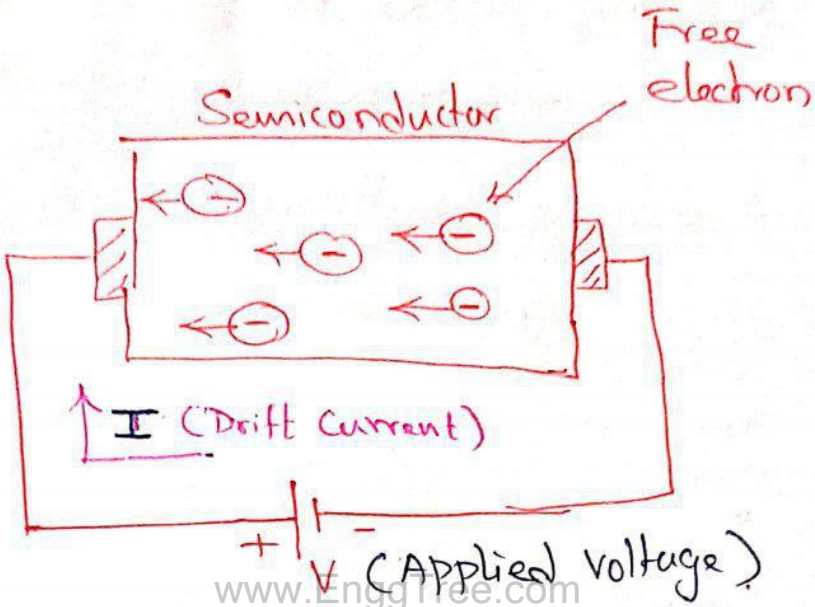


8. what is Peak Inverse Voltage?

It is maximum reverse bias voltage that can applied to a PN diode without damage the diode. It is denoted by V_{PIV} (without Breakdown)

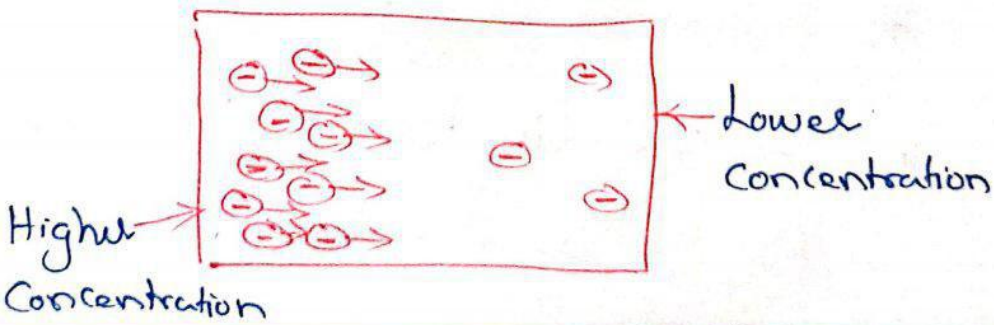
9. what is meant by drift Current?

It is Current due to motion of electron under the influence of applied voltage.



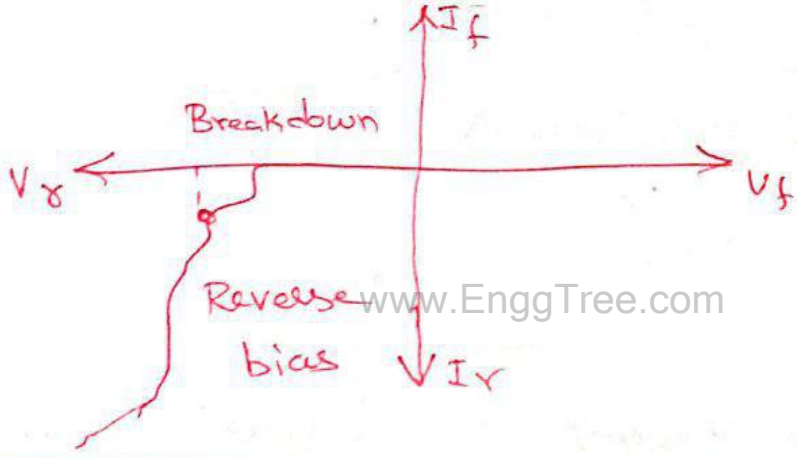
10. what is meant by diffusion Current?

It is Current due to motion of electron ~~without~~ from higher Concentration to lower Concentration without applied voltage.



11. What is meant by Avalanche breakdown?

Avalanche breakdown occurs due to Collision of electrons which generate more electron and holes pair. This increase in electron and hole pair is Called Avalanche multiplication



12. Mention the applications of Zener diode?

* Used as Voltage Regulators.
* Protection Circuits.
* Zener Limiters. (Unwated portion of the voltage waveform).

13. Give any Four applications of PN diode?

* Used as rectifiers.
* Used as Clipper and Clamper
* Used as detector
* Used as Light Emitting Diode

14. Define Transformer Utilization Factor (TUF).

The factor which indicates how much is the utilization of the transformer in the Circuit is called Transformer Utilization Factor (T.U.F).

$$T.U.F = \frac{\text{D.C. Power at load}}{\text{A.C. Power rating of the transformer.}}$$

T.U.F = 0.287 for Halfwave rectifier

T.U.F = 0.812 for Fullwave rectifier

15. Define Ripple factor (γ)

It is a ratio of R.M.S value of a.c. Component at output to the average (or) d.c. Component at output of rectifier.

$$\text{Ripple factor } \gamma = \frac{\text{R.M.S value of a.c component at o/p}}{\text{Avg (or) d.c Component at o/p}}$$

16. Define intrinsic Stand-off ratio of UJT ?

UJT intrinsic Stand off ratio is defined as

$$\eta = \left.\frac{R_{B1}}{R_{B1}+R_{B2}}\right|_{I_E=0}$$

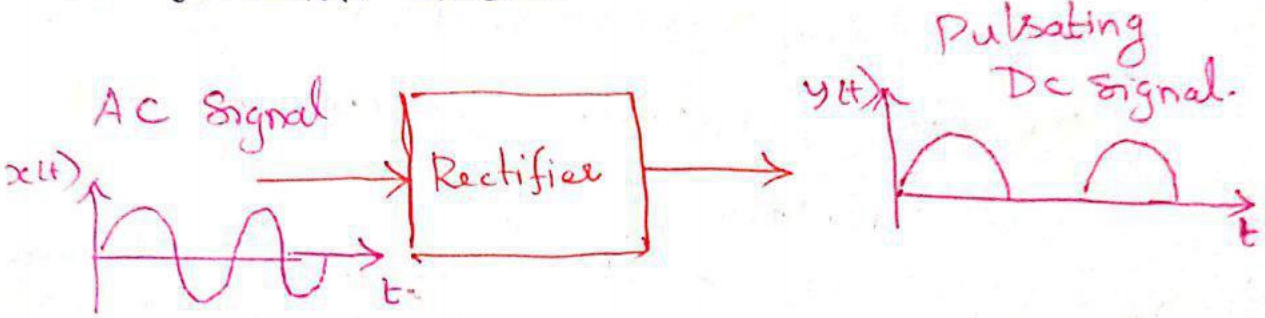
η = 0.5 to 0.8 typical range

R_{B1} - Resistance b/w Emitter & Base 1

R_{B2} - Resistance b/w Emitter & Base 2

17. What is meant by rectifier? List its types?

A rectifier is a device which converts a.c. voltage to pulsating d.c. voltage, using one (or) more PN junction diode.



Types

1. Half wave rectifier
2. Full wave rectifier
3. Bridge rectifier.

18. Define Voltage regulation.

The Voltage regulation is the factor which tells us about the change in the d.c. output voltage as load change from to full load.

$$\text{Voltage regulation} = \frac{(V_{dc})_{NL} - (V_{dc})_{FL}}{(V_{dc})_{FL}}$$

19. What is transistor (or) BJT?

Transistor is a three terminal device: Base, emitter and Collector,

Transistor – Transfer – Resistor

Base on Current in base the resistance between Collector to emitter will transfer

Two Types

* npn - transistor
* pnp - transistor

20. Why transistor called a Current Controlled device?

In BJT output Current is Controlled by input Current and hence it is a Current Controlled device.

21. State the three operating regions of transistor.

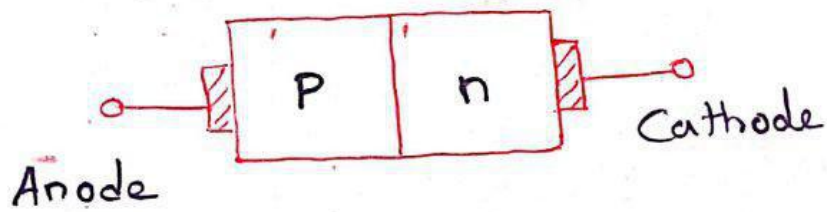
	Region	Emitter - Base	Collector-Base
1.	Cut-off	Reverse Bias	Revese Bias
2.	Active	Forward Bias	Revese Bias
3.	Saturation	Forward Bias	Forward Bias

22. Part - B

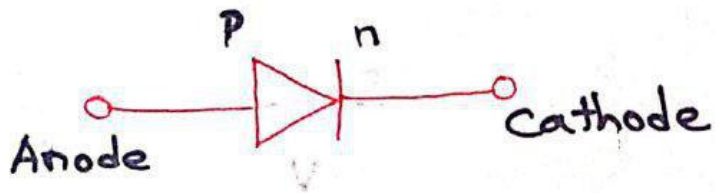
(1) Explain the Construction, operation and VI characteristics of PN Junction diode.

The PN junction diode form by Combining P-type and n-type Semicondu -ctor.

The PN junction diode Contain two terminals anode and Cathode as Shown below.



Diode Symbol :-



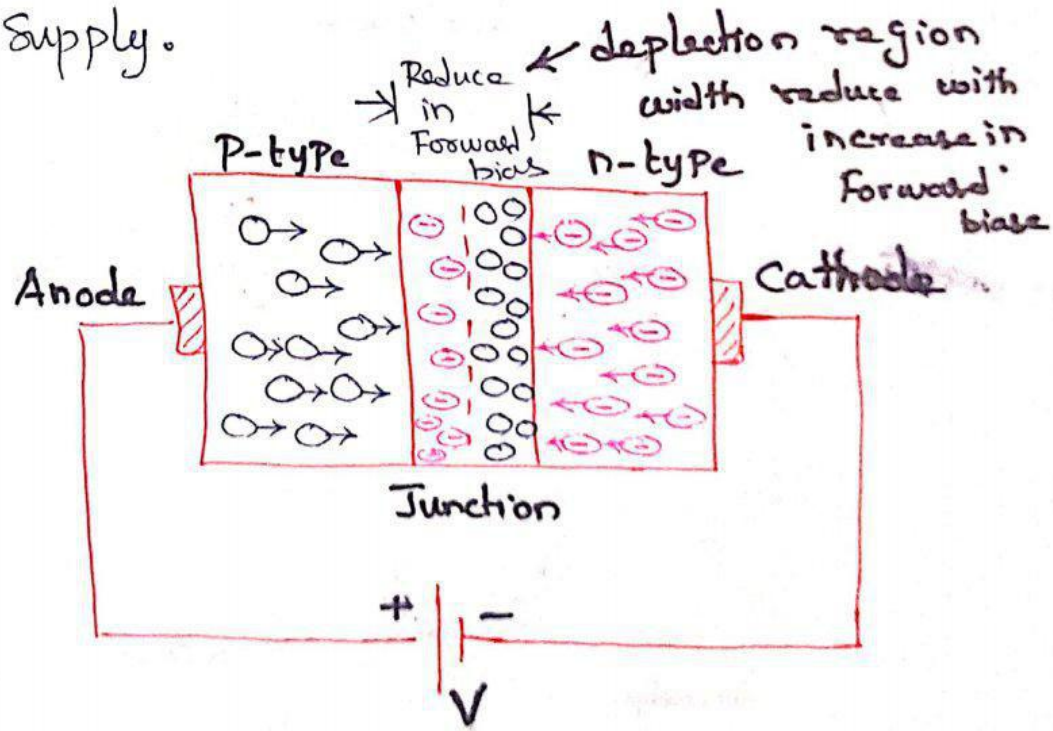
Applying external d.c. voltage to any electronic device is called biasing.

In PN junction diode biasing can be classified as

i) Forward biasing
ii) Reverse biasing

Forward biasing :-

Connecting P-type to Positive of the Supply and n-type to negative of the supply.



when the applied voltage (Forward bias) increases, the depletion region slowly decrease and when applied voltage is equal to Knee voltage (cut-in voltage) the depletion region Completely Vanish and diode start Conducti

for Silicon = 0.7 volts
Germanium = 0.3 volts
} cut-in voltage

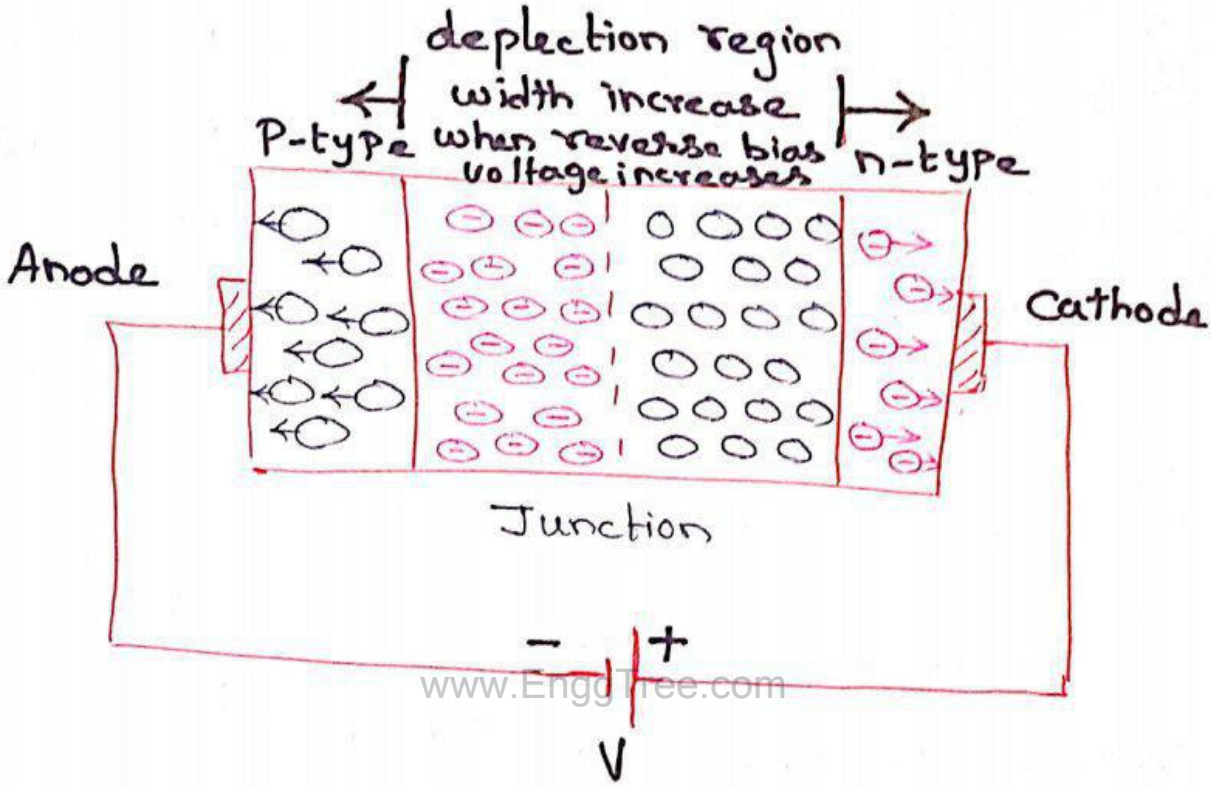
when the applied forward bias voltage > Knee (or) cut-in voltage the current increase rapidly and diode in "ON" state.

Reverse Biasing :-

Connecting P-type to negative of the Supply and n-type to Positive of the Supply

when the applied reverse bias voltage increases, the depletion region

width increases, diode wont Conduct during reverse bias until reverse breakdown occurs.



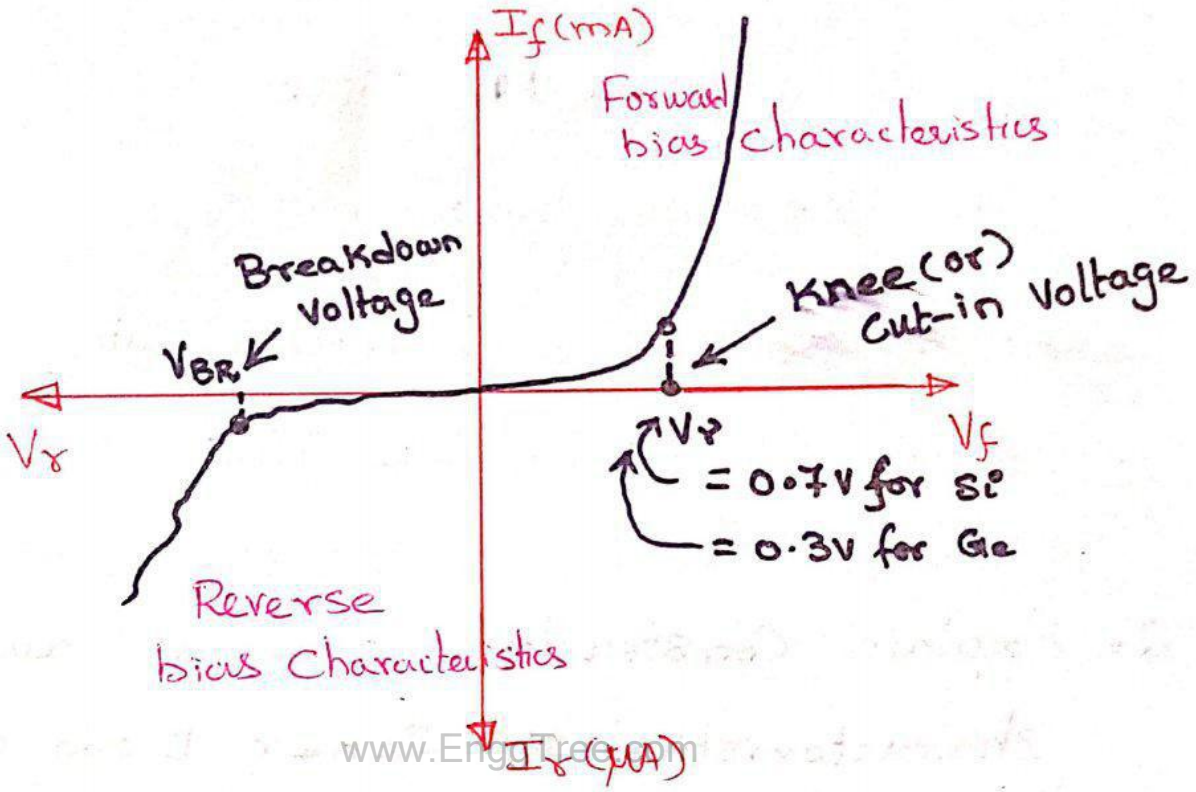
Break down :-

If reverse bias voltage is increased beyond particular voltage (Break down voltage), large reverse current will damage the diode and Causes Reverse Breakdown at revese breakdown voltage (V_{BR}).

VI Characteristics of PN diode :-

The Complete VI characteristics of PN diode is the Combination of its

forward as well as reverse characteristics. It is shown in figure below.



Advantages of PN diode :-

* It is very much compact
* It is used on-off switch (simple)
* It is cheap

Disadvantages of PN diode :-

* Temperature sensitive with effects its characteristics
* Not suitable for high speed switching
* Power dissipation capability is low.

Application of PN junction diode :-

* Used as rectifiers.
* It is used in clipper and clamper circuits
* Used as switch
* It is used in detector circuits
* It is used in Gate circuit

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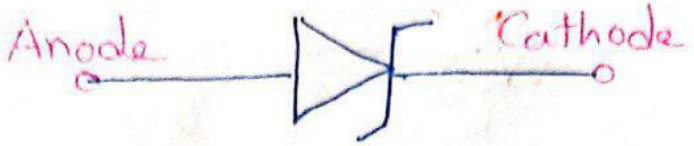
2. Explain Construction, operation and characteristics of Zener Diode and also explain avalanche and Zener Breakdown.

Zener diode is a specific type of Semi conductor diode, which is made to operate in the revesse breakdown region.

Heavily doped P-type and n-type Combined to form Zener diode.

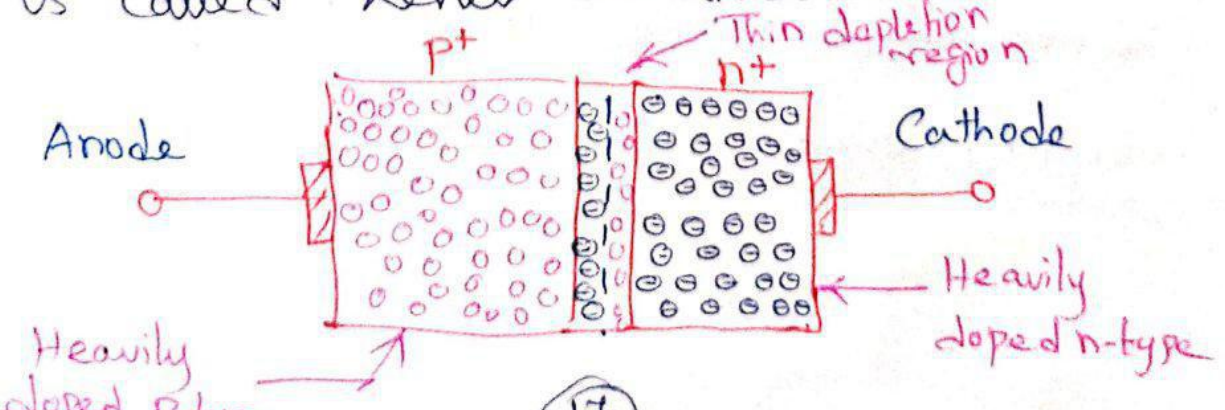
Symbol for Zener diode:



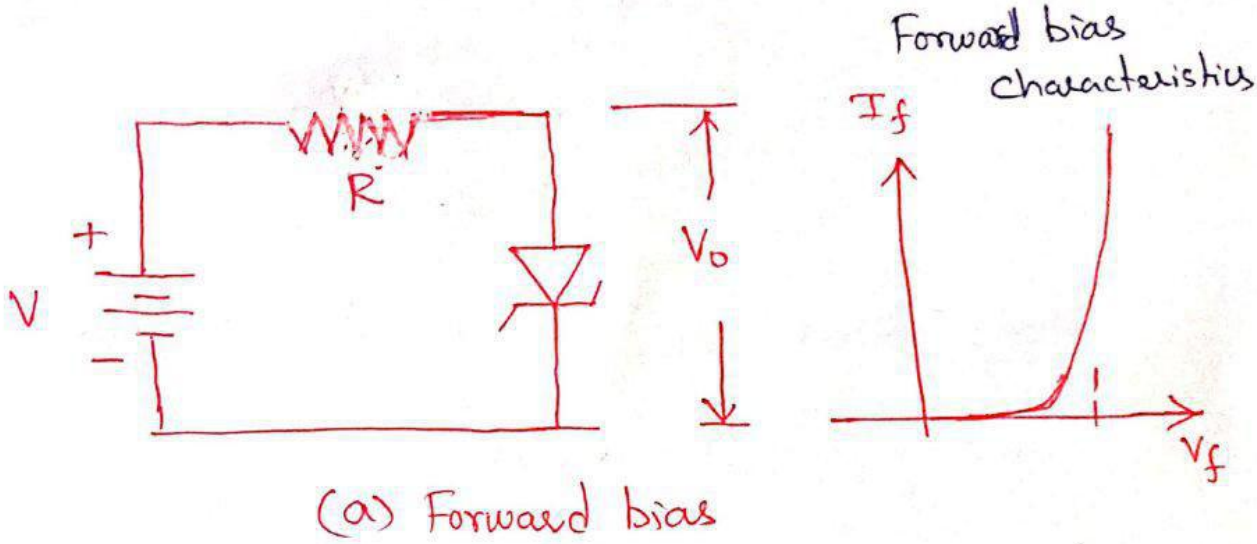
Working Zener is similar in forward bias as same as PN diode.

But in Zener diode due to heavily doped the depletion region is very narrow and thin.

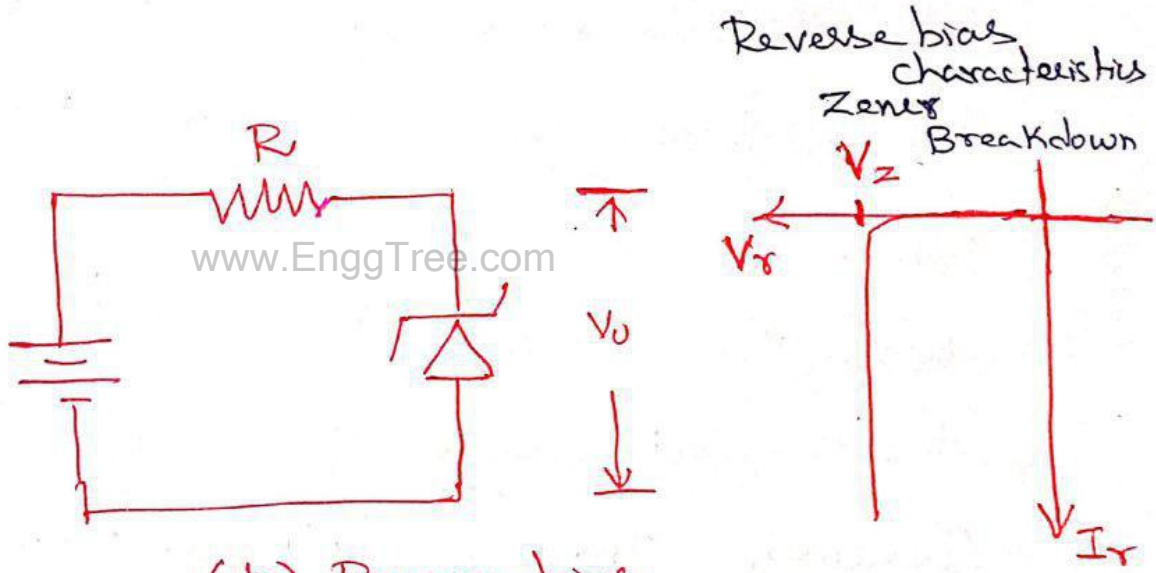
when the reverse bias voltage increases the minority carrier got enough Energy to Penetrate through thin depletion due to which breakdown occurs. It allows the reverse current to pass through it, is called Zener breakdown.



Zener diode :-



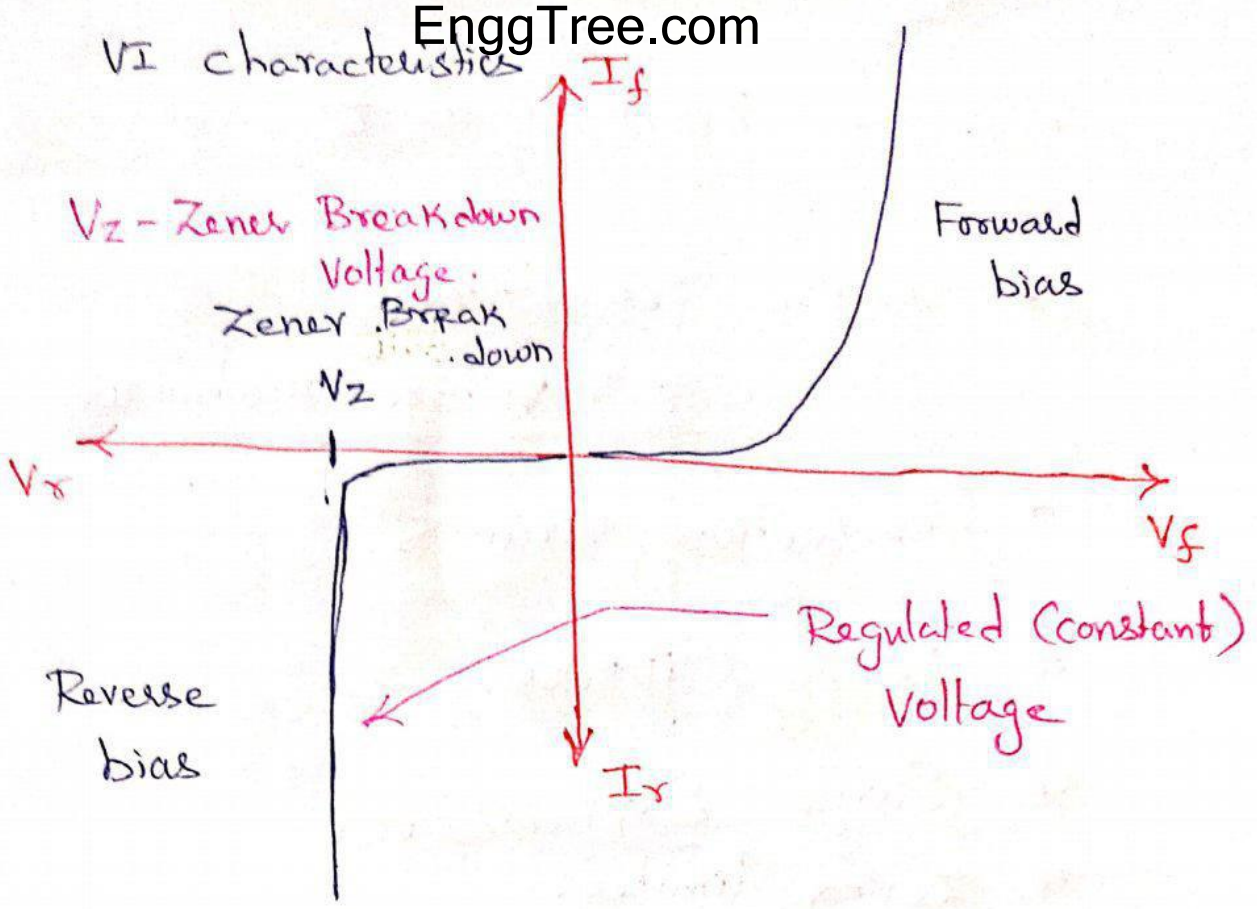
(a) Forward bias



(b) Reverse bias

VI Characteristics :-

Complete VI characteristics of Zener diode is combined characteristics of forward and reverse bias.



Zener Breakdown

Due to high electric field applied accross zener diode the minority charges got enough energy to penerate through the thin depletion region and start conduct with reverse bias voltage is called zener Breakdown.

Advantage of Zener diode :-

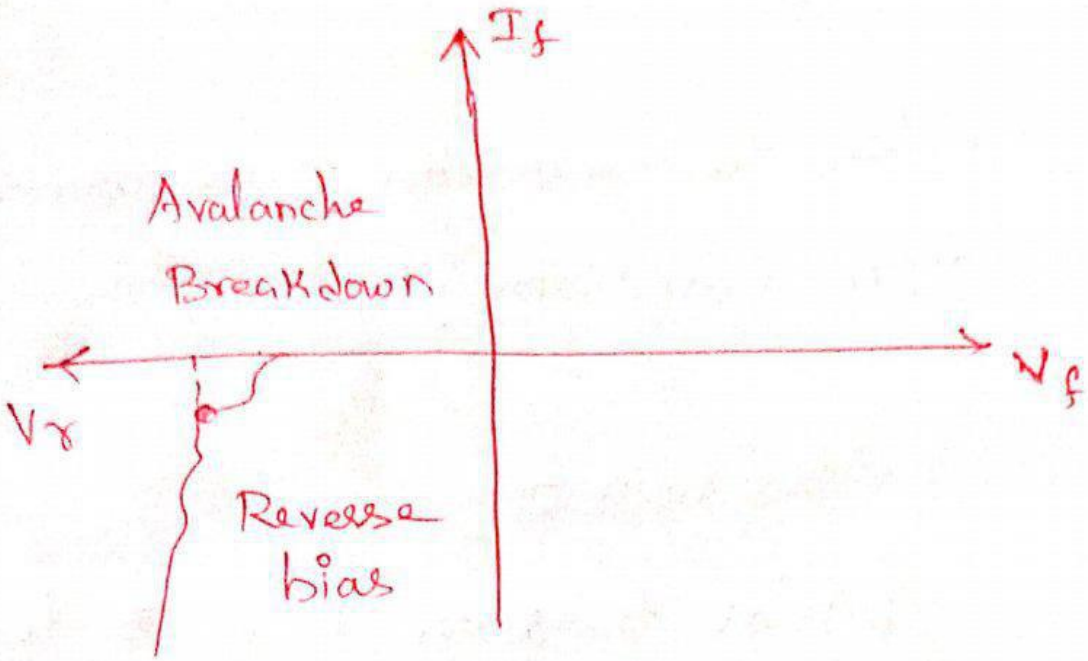
* Less expensive.
* Protection from over voltage
* Usable in smaller Circuits

Applications of Zener diode :-

* Voltage regulators
  (or) voltage Stabilizers
* Protection Circuits.
* Peak Clippers.
* Surge Suppressors.
* Zener limiter.

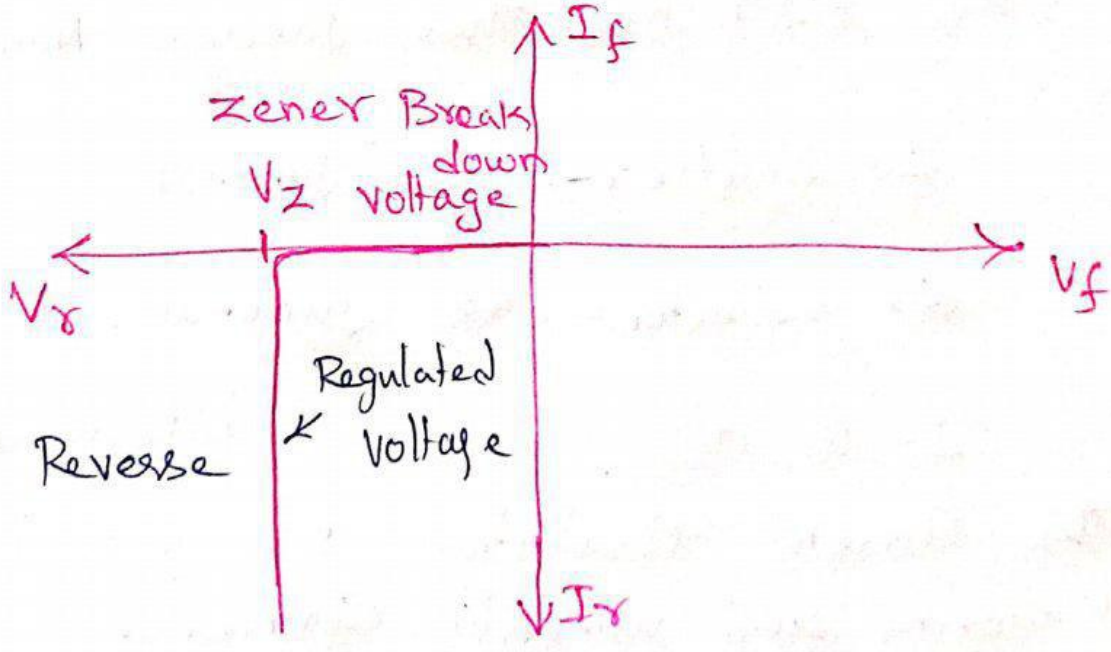
Avalanche breakdown :-

Avalanche breakdown occues due to collision of electrons which Generate more electron and hole pair. This increase in electron and hole pair is called Avalanche Multiplication. Due to this more electron, hole pair as minority Carrier Causes Conduction in reverse bias called Avalanche breakdown.



Zener breakdown :-

The process in which the electrons move across the thin barrier (junction) from the valence band of P-type material to the Conduction band of n-type material is known as Zener breakdown.



(3) Explain the Construction and working of NPN transistor?

BJT Transistor :-

Bipolar transistor is a 3 terminal Semi conductor device

The three terminals are

* Emitter (E)
* Base (B)
* Collector (C).

The BJT has two junctions namely

1. Emitter-base junction
2. Collector-bas junction.

It is also called as bipolar device. The Current Conduction is due to both majority and minority Carriers.

$$I_E = \gamma I_B$$

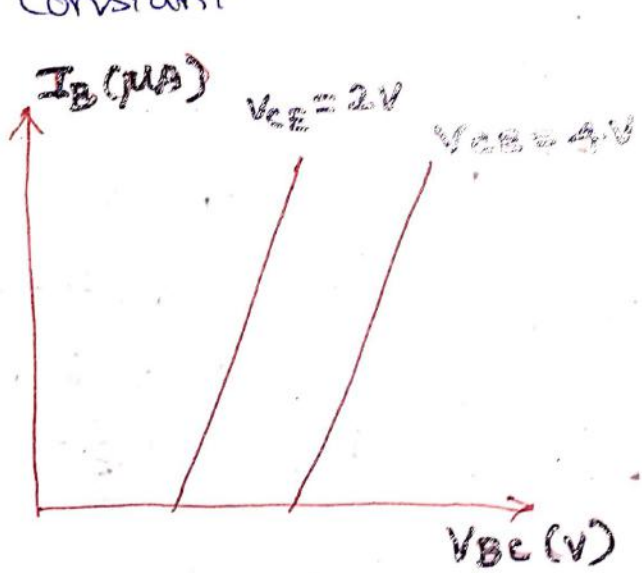
$$\gamma = \frac{I_E}{I_B}$$ forward Current Gain.

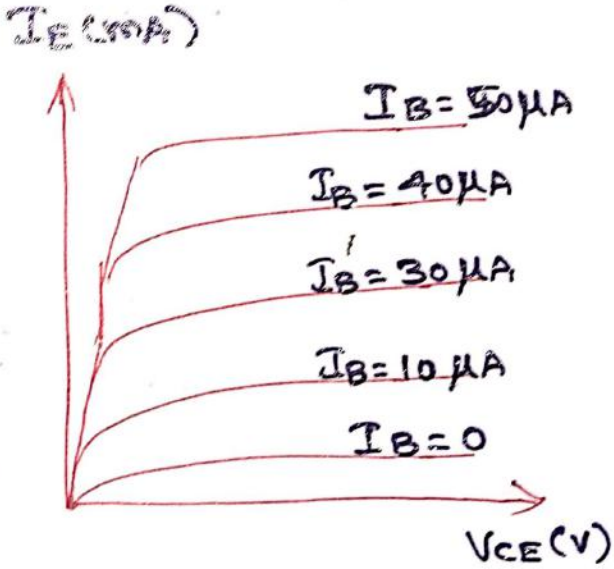
Input characteristics :-

Graph between input voltage (V_{BC}) and input current (I_B) | output voltage (V_{CE}) constant

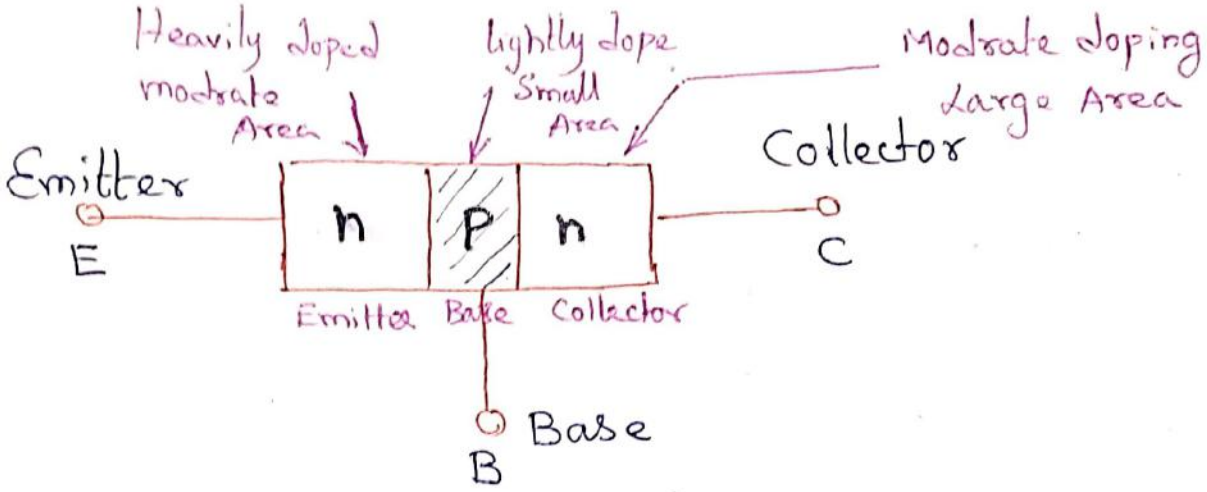
output characteristics :-

Graph between output voltage (V_{CE}) and output current (I_E) by keeping input current (I_B) Constant





Structure of npn BJT



When a transistor is formed by sandwiching a ~~Big~~ Single P-type between two n-type as Shown in above figure.

Emitter :-

It is heavily doped and Area of Emitter region is modrate. It emittes the charge carrier

Base :-

It is middle region called base of the transitor.

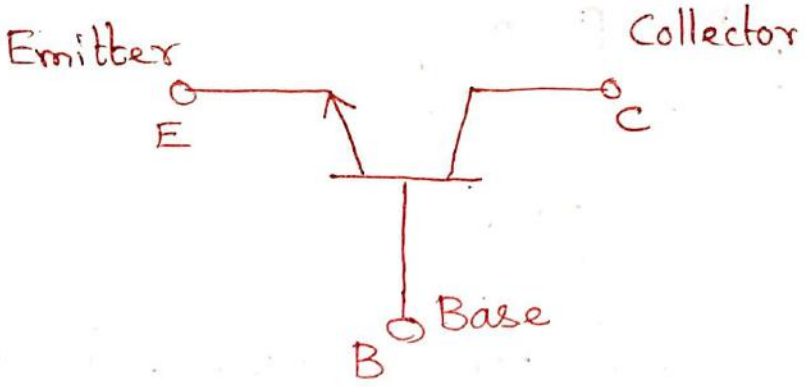
It is Very thin (Small) and lightly doped.

Collector :-

The collector region-area is high and modrate doping

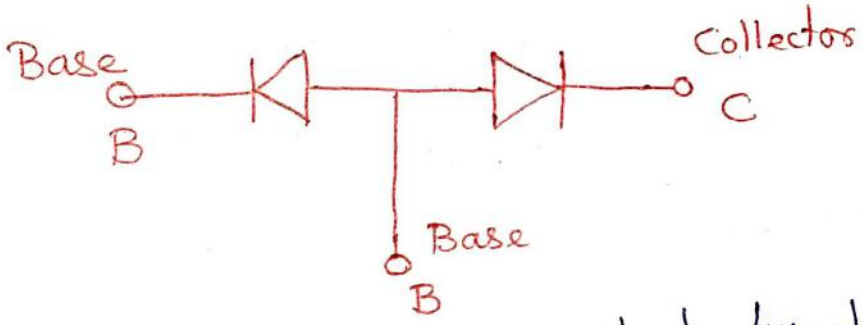
It is used to collect the charge carriers.

npn transistor Symbols :-



Arrow direction indicates the direction of current.

Diode Equivalent Circuit :-



Two back to back connected two diode form a transistor.

Operation BJT Transistor :-

The transistor can be bias to work in three important region.

* Cut-off region
* Active region
* Saturation.

Cut-off region :-

when Emitter-Base reverse bias and Collector-Base reverse bias, transistor works in cut-off region

In this region transistor act as Switch "OFF" State.

Active region :-

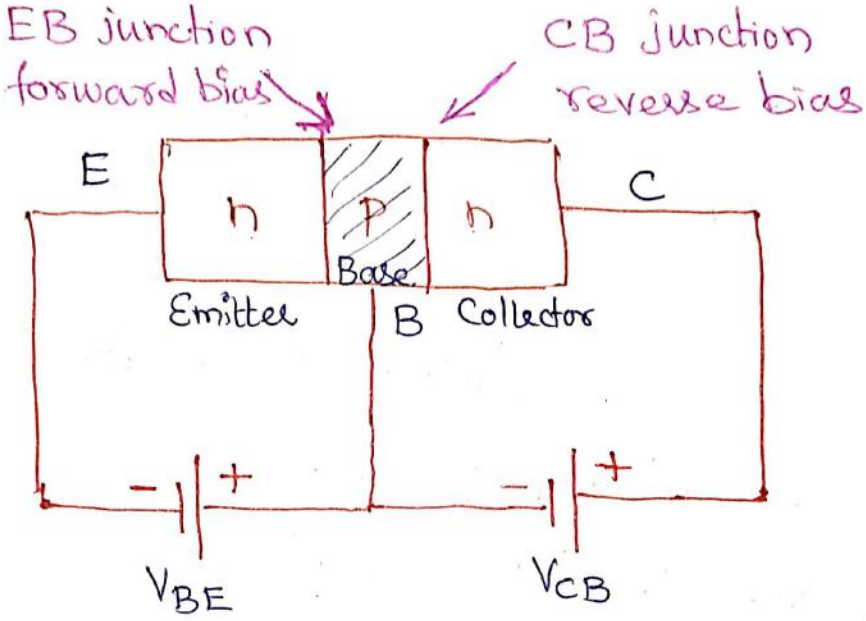
when Emitter-Base forward bias and Collector-Base reverse bias, transistor works in Active region.

In this region transistor works as amplifier, oscillator

Saturation region :-

when Emitter-Base forward bias and Collector-Base forward bias, transistor works in Saturation region.

In this region transistor act as switch "ON" State.

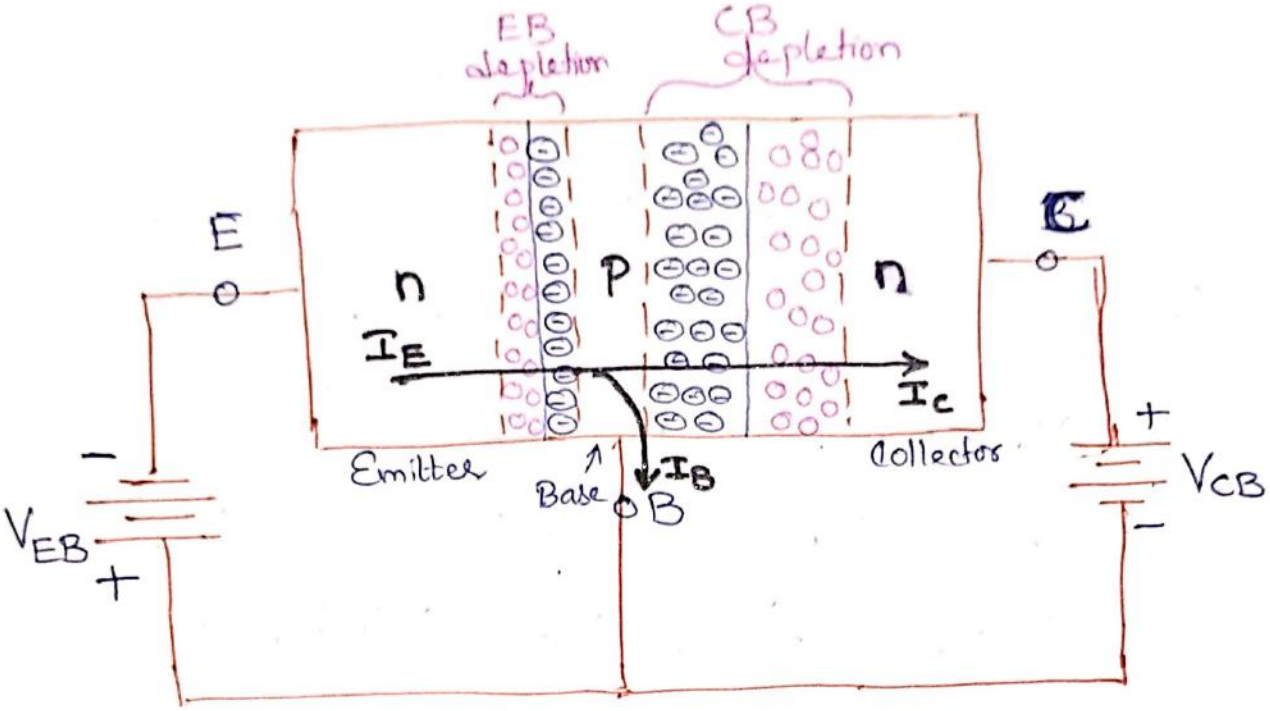


The Emitter-Base forward bias, the Width of EB junction is reduced

The Collector-Base reverse bias, the CB junction width increase.

As EB forward bias Create emitter Current I_E. A Small no. of electrons from Emitter recombine with holes in Base region Create a very Small base Current I_B. Remaining electrons follow towards collector Cause collector Cutrent I_C

$$\therefore I_E = I_B + I_C$$



the Collector Current is due to majority and minority charges so it is called Bipolar device.

3. Draw and Explain the input and output characteristics of a transistor in CE / CB / CC Configuration?

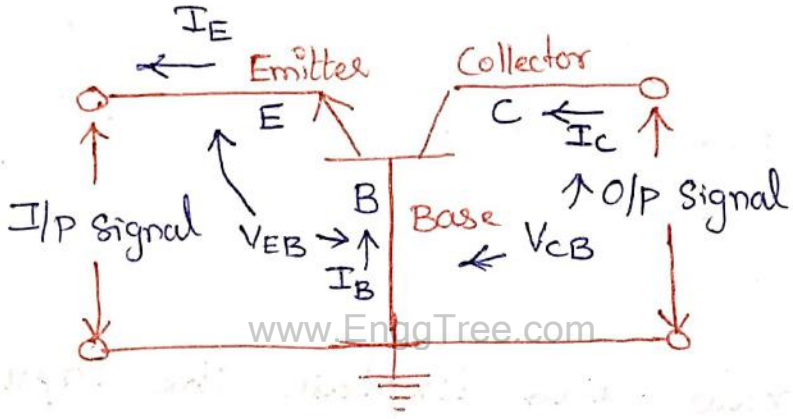
Transistor Configuration :-

The way in which transistors are connected in a Circuit is called as Configuration. The three basic Configuration are

1. Common Base [CB] Configuration
2. Common Emitter [CE] Configuration
3. Common Collector [CC] Configuration

CB Configuration :- [Common Base]

Here the Base is grounded (or) it is Common to the input and output side. The input Signal is applied between the Emitter and base and the output signal is taken between the Collector and base.



V_{EB} – Input Voltage | V_{CB} – output voltage

I_E – Input Current | I_C – output Current

Input Characteristics

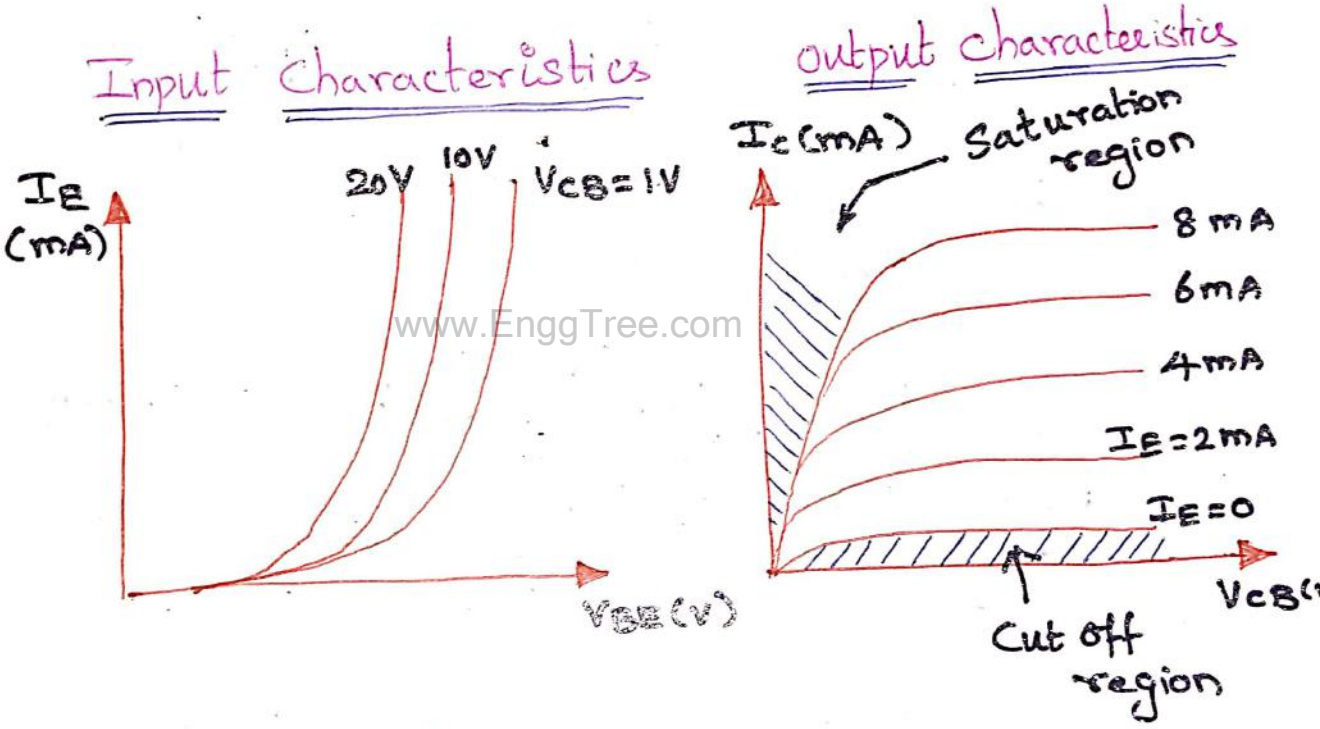
This is a graph drawn between input voltage (V_{EB}) Versus input current (I_E) by keeping output Voltage (V_{CB}) Constant.

For different Values of V_{CB} O/P voltage the Input V-I characteristics which looks like the forward characteristics

of a PN diode.

Output Characteristics

This is a graph drawn between output voltage (V_{CB}) Versus output Current (I_C) by keeping input Current (I_E) Constant.



Active Region :-

The active region of output characteristics is one in which the CB junction reverse biased and Emitter Base junction is forward biased.

when $I_E = 0mA$, only the Small Current Saturation Current I_{CBO} flows

ie, $I_C = I_{CBO}$

$$I_C = \alpha I_E \qquad \alpha = \frac{I_C}{I_E}$$

α - Forward Current Gain of Common Base Configuration.

Saturation region :-

In this both junctions Emitter-Base and Collector-Base are forward bias

In this region Small change in Collector Voltage Cause large change in Collector Current I_C.

The Collector Current exponetially increases with V_{CB}.

Cut-off region :-

In this region both Emitter-Base and Collector-Base are reverse bias.

Early effect (or) Base width modulation :-

The width of the base depends on the Base Voltage known as early effect. The easly effect leads to

(i) Increase in dc Current Gain (α_{dc})

(ii) Breakdown voltage is extremely high.

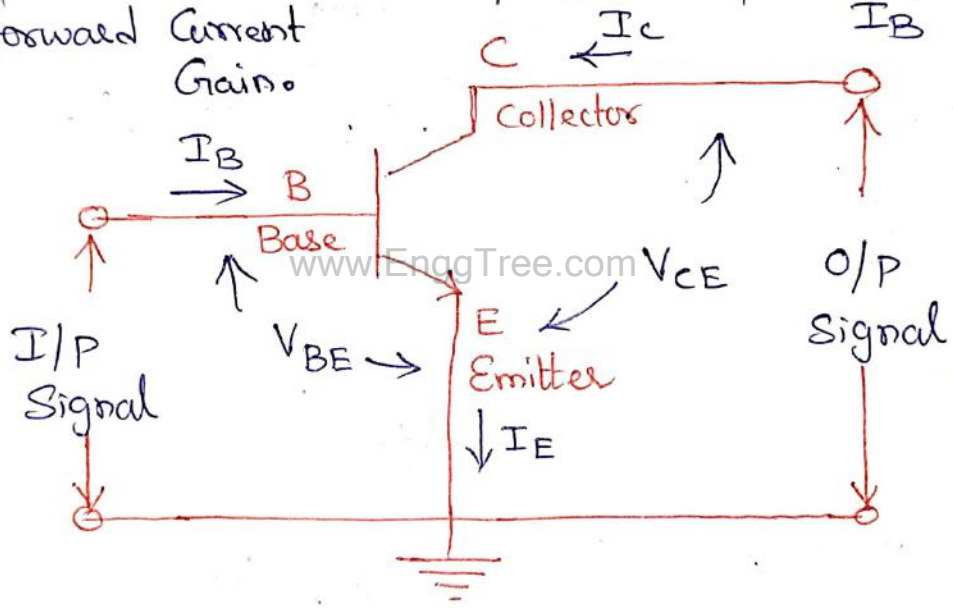
Common Emitter [CE] Configuration :-

In CE configuration, the input voltage is applied at Base and the output is taken at the Collector and Emitter is common between input and output.

$$I_C = I_E + I_B$$

$$I_C = \beta I_B \qquad \beta = \frac{I_C}{I_B}$$

β = forward Current Gain.



V_{BE} – Input Voltage | V_{CE} – output voltage

I_B – Input Current | I_C – output Current

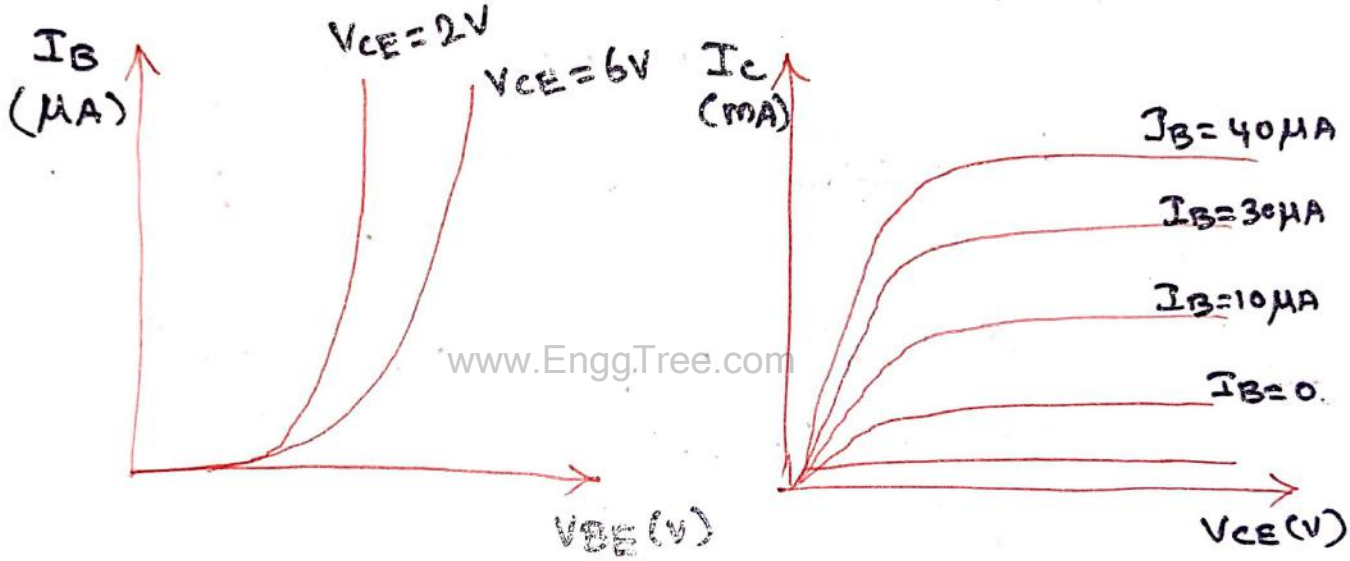
Input characteristics

The input characteristics is drawn input voltage (V_{BE}) and the input Current (I_B) by keeping output voltage (V_{CE}) is Constant.

output Characteristics

This is a graph drawn between output Voltage (V_{CE}) Versus output Current (I_C) by keeping input Current (I_B) Constant.

Input characteristics output characteristics



Common Collector Configuration :-

In Common Collector Configuration input is applied on Base and output is taken at emitter. or The Collector is Common between input and output.

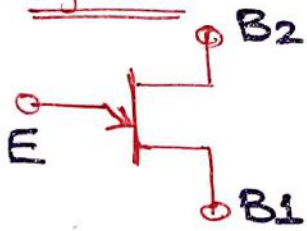
V_{BE} – Input Voltage	V_{CE} – output Voltage
I_B – Input Current	I_E – output Current.

4. Explain UJT Construction, Operation and VI Characteristics and also explain how UJT work as relaxation Oscillator.

A Unijunction transistor (UJT) is a three terminal Device.

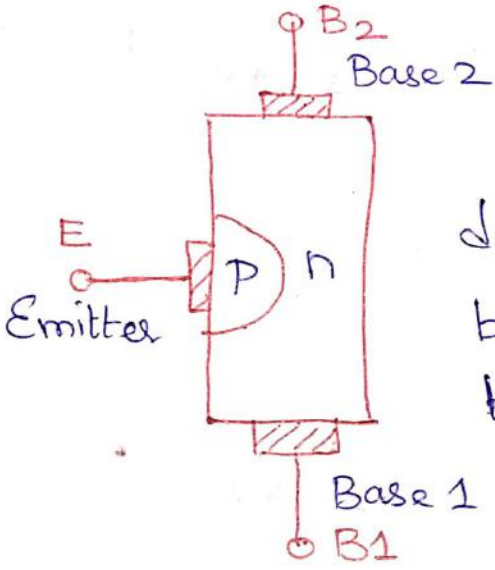
* Emitter (E)
* Base 1 (B1)
* Base 2 (B2)

Symbol



Construction and Equivalent Circuit

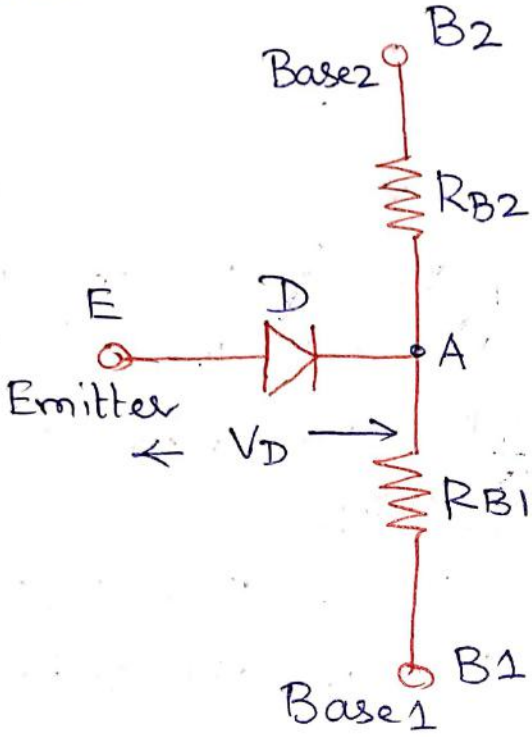
The basic Structure of UJT is shown below



Slab of lightly doped n-type between base 1 and base 2 terminal. [B1 & B2]

A P-type material is used to form PN junction with a Contact called Emitter (E)

The equivalent Circuit of UJT Shown below.

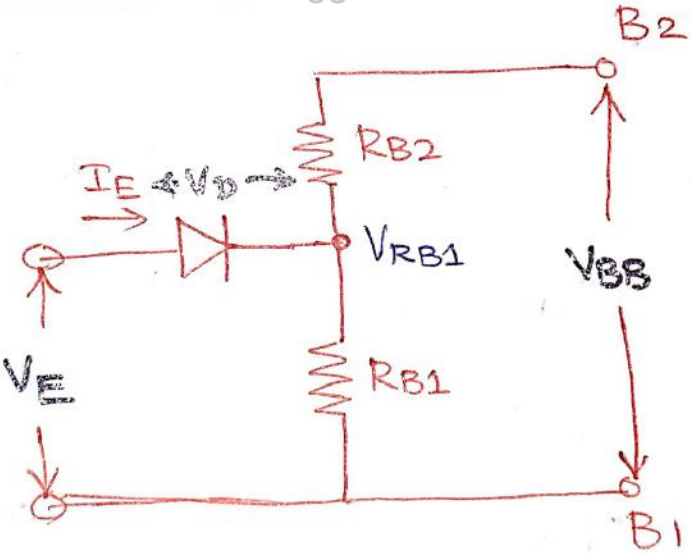


The internal resistance are R_{B1} and R_{B2}

Interbase resistance

$$R_{BB} = R_{B1} + R_{B2}$$

Intrinstic Stand off Ratio (η)



$$R_{BB} = R_{B1} + R_{B2}$$

$$V_{RB1} = \frac{R_{B1}}{R_{B1} + R_{B2}} \cdot V_{BB}$$

where

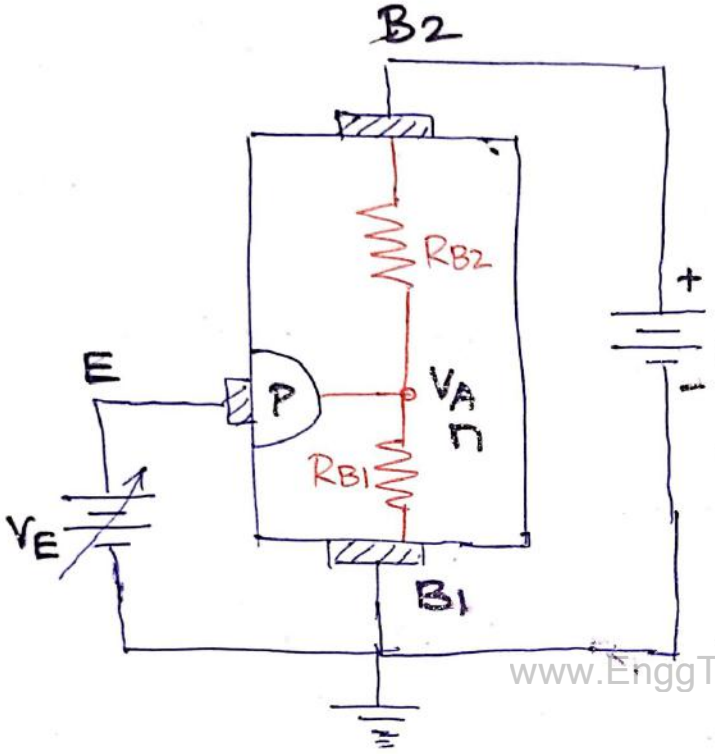
$$\eta = \frac{R_{B1}}{R_{B1} + R_{B2}}$$

$$V_{RB1} = \eta \cdot V_{BB}$$

η - Intrinsic Stand off ratio.

η = 0.5 to 0.8 typical range.

Principle of Operation



* when $V_E < V_P$

As long as V_E less than V_A the PN junction is reverse bias

Thus UJT is in OFF state.

* when $V_E \geq V_P$

$(V_P = V_A + V_D)$

Generally V_D = 0.3 for Ge and V_D = 0.7 for Si°

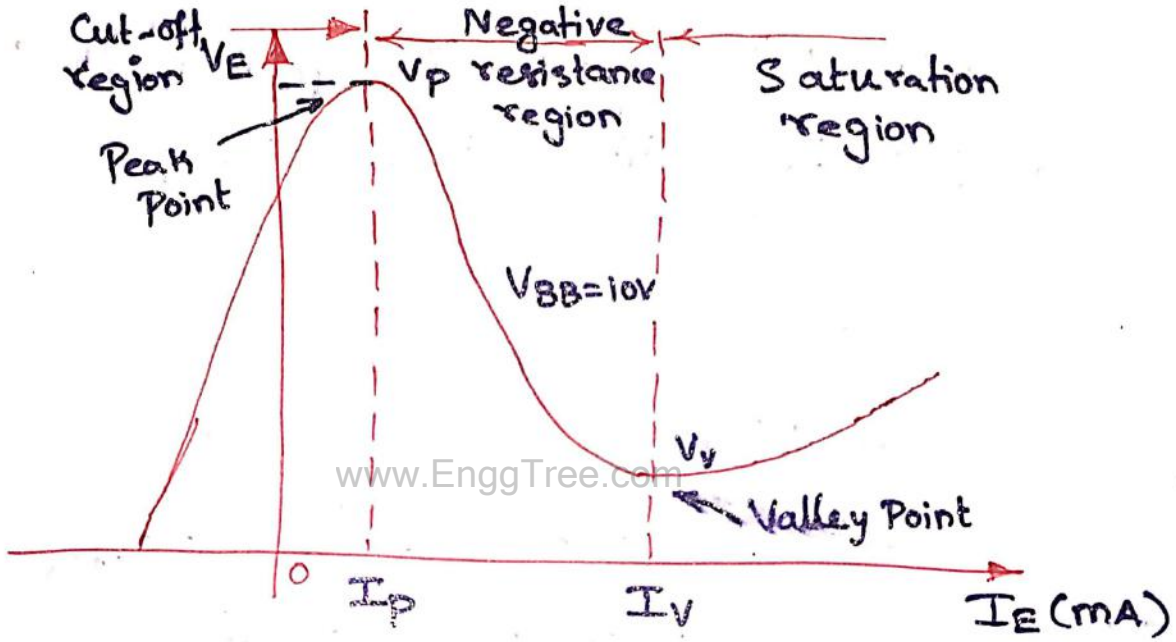
$$V_P = V_A + V_D = \eta V_{BB} + V_D$$

when $V_E >> V_P$

The PN junction becames forward biased and current I_E flows. The UJT is in "ON" State.

UJT characteristics :-

The graph drawn between emitter current and emitter voltage for a particular value of V_{BB} is called the UJT characteristics.



Cut-off region :-

When $V_E < V_p$ – PN-junction reverse biased

No current, $I_E = 0$ "OFF" state.

Negative resistance region :-

When $V_E = V_p$ the PN-junction forward biase and I_E starts to flow. The voltage accross the device decreases in this region

$\uparrow I_E$ but $\downarrow$ voltage

Hence the region is called negative resistance region. This region used in many application.

Saturation region :-

Futher increase in I_E after valley Point UJT get Saturated and Current and Voltage start increases.

Application

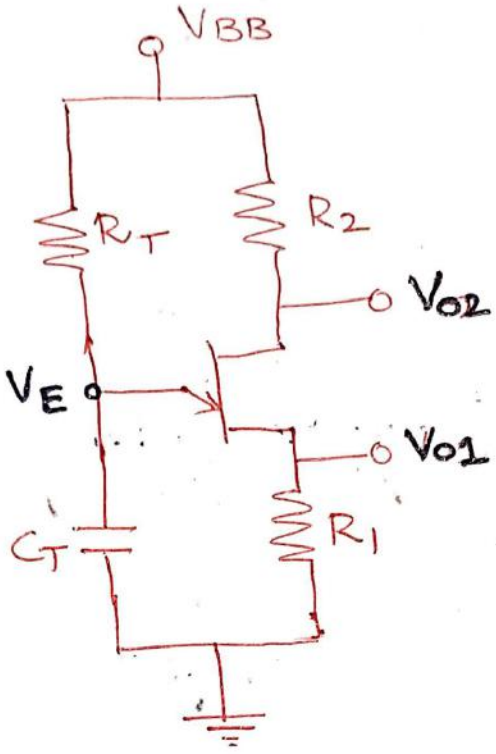
* Used as triggering SCR
* Used as relaxation oscillator
* Sawtooth wave generator.

UJT Relaxation Oscillator :-

The UJT Relaxation oscillator used to generate Sawtooth wave form.

This is also called UJT based Sawtooth oscillator.

UJT Relaxation Oscillator shown in figure



The resistance R_T and capacitance C_T decide the oscillating rate.

$$f_o = \frac{1}{R_T C_T \ln\left[\frac{1}{1-\eta}\right]}$$

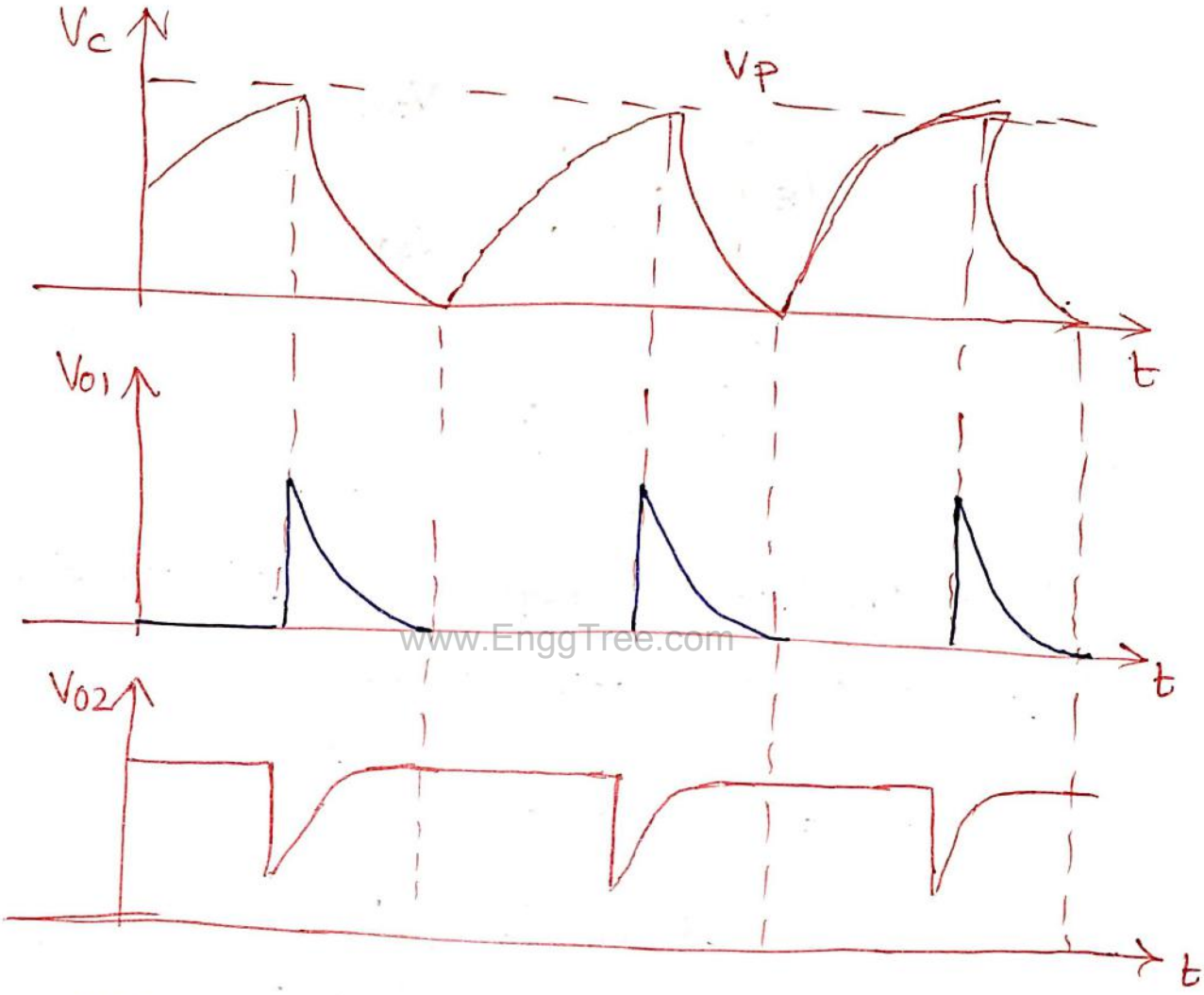
Operation :-

Capacitor C_T get charged through the resistance R_T towards V_{BB}.

When Capacitor Voltage $< V_P$. The Emitter is open Circuit.

$$V_P = \eta V_{BB} + V_D$$

when V_c capacitor voltage > V_p . The Capacitor Starts discharge through R_1 and R_{B1}



The Capacitor charging equation.

$$V_c(t) = V_v + V_{BB}\left[1 - e^{\frac{-t}{R_T C_T}}\right]$$

$$V_c(t) = V_p \quad \text{at } t = T$$

$$V_p = \eta V_{BB} + V_D = V_v + V_{BB}\left[1 - e^{\frac{-T}{R_T C_T}}\right]$$

V_D and V_v Neglected

$$\eta = 1 - e^{\frac{-T}{R_T C_T}}$$

$$T = R_T C_T \ln\left[\frac{1}{1-\eta}\right]$$

$$f_o = \frac{1}{T} = \frac{1}{R_T C_T \ln\left[\frac{1}{1-\eta}\right]}$$

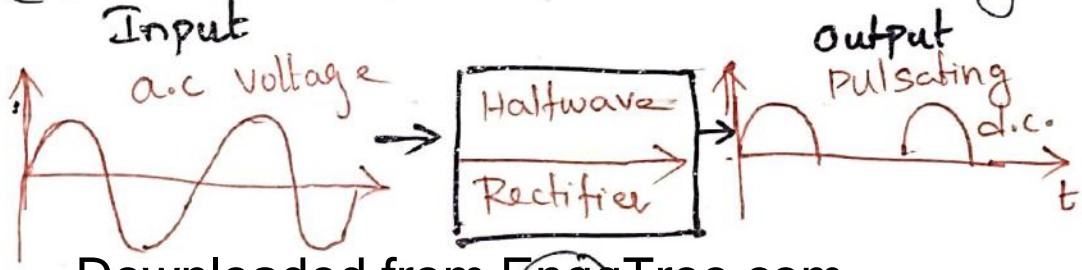
f_o = Oscillating frequency.

5. Explain the working Principle of half wave rectifier and derive the expression for ripple factor, efficiency, V_{dc}, I_{rms}, I_{dc}, V_{rms} and TUF.

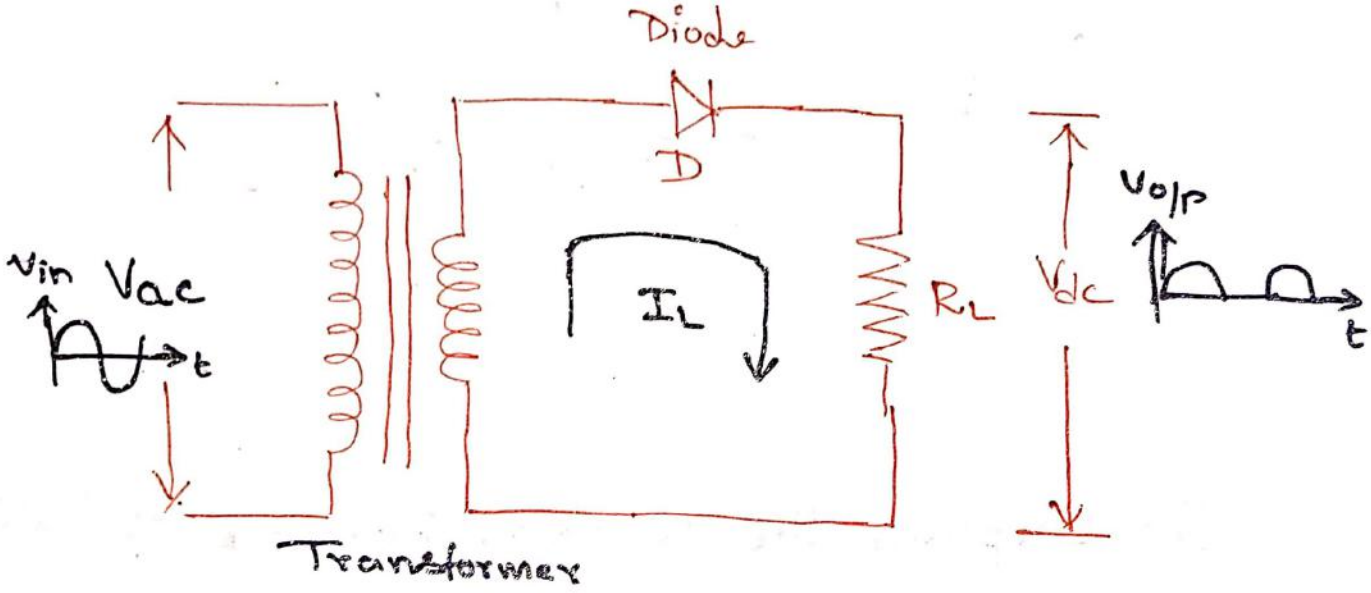
Rectifier :-

Rectifier is a Circuit which Convert a.c. Voltage to pulsating d.c. Voltage using one (or) more PN diode.

In half wave rectifier only one half cycle is rectified as pulsating dc.

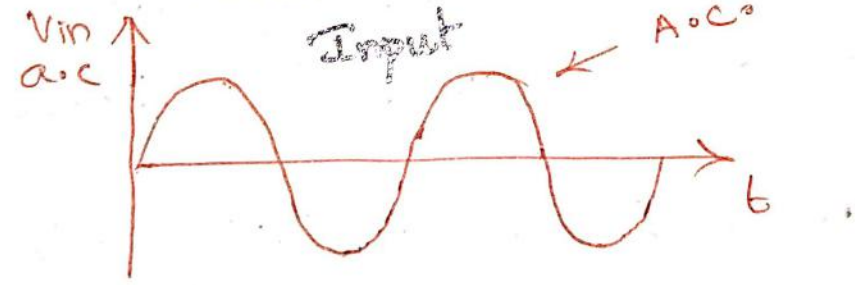


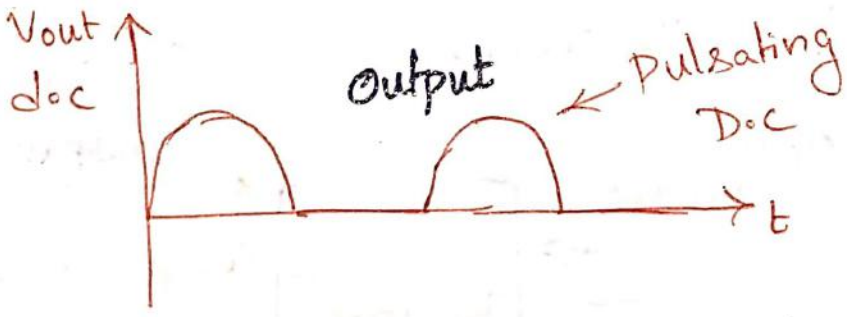
Half wave rectifier Circuit Shown below



During Positive half Cycle of input Diode D Conduct and Cause the output.

During Negative half Cycle of input Diode D "OFF" State and ~~No~~ Open Circuited So No Output at Load.





Average (or) D.C. Current (I_{dc})

The Current waveform at output is given by

$$i_L = I_m \sin(\omega t) \quad \text{for } 0 < \omega t \leq \pi$$

$$= 0 \quad \text{for } \pi < \omega t \leq 2\pi$$

$$I_{avg} = I_{dc} = \frac{1}{2\pi} \int_0^{2\pi} i_L \, d(\omega t)$$

$$= \frac{1}{2\pi} \left[\int_0^{\pi} I_m \sin(\omega t) \, d(\omega t) + \int_{\pi}^{2\pi} 0 \, d(\omega t) \right]$$

$$= \frac{I_m}{2\pi} \left[-\cos(\omega t) \right]_0^{\pi}$$

$$= \frac{I_m}{2\pi} \left[-\cos(\pi) + \cos 0 \right]$$

$$= \frac{I_m}{2\pi} \left[-(-1) + 1 \right] = \frac{I_m}{2\pi} \times 2$$

$$\boxed{I_{avg} \text{ (or) } I_{dc} = \frac{I_m}{\pi}}$$

Average (or) DC Voltage :-

$$V_{dc} \text{ (or) } V_{avg} = I_{dc} R_L$$

$$= \frac{I_m}{\pi} R_L$$

R.M.S Current (I_{RMS})

R.M.S — Root Mean Square value.

$$I_{RMS} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} i_L^2 \, d(\omega t)}$$

$$= \sqrt{\frac{1}{2\pi} \left[\int_0^{\pi} [I_m \sin(\omega t)]^2 d(\omega t) + \int_{\pi}^{2\pi} 0 \, d(\omega t) \right]}$$

$$= \sqrt{\frac{I_m^2}{2\pi} \int_0^{\pi} \sin^2(\omega t) \, d(\omega t)}$$

$$= \sqrt{\frac{I_m^2}{2\pi} \int_0^{\pi} \left[\frac{1 - \cos 2(\omega t)}{2} \right] d(\omega t)}$$

$$= \frac{I_m}{2} \sqrt{\frac{1}{\pi} \left[\omega t - \frac{\sin 2(\omega t)}{2} \right]_0^{\pi}}$$

$$= \frac{I_m}{2}\sqrt{\frac{1}{\pi}\left[\pi - \frac{\sin 2\pi}{2} - \left[0 - \frac{\sin 0}{2}\right]\right]}$$

$$= \frac{I_m}{2}\sqrt{\frac{1}{\pi}\pi}$$

$$\boxed{I_{RMS} = \frac{I_m}{2}}$$

D.C. Power at load

The d.c. Power is given by

$$P_{dc} = I_{dc}^2 \cdot R_L$$

$$= \left[\frac{I_m}{\pi}\right]^2 R_L$$

$$\boxed{P_{dc} = \frac{I_m^2 R_L}{\pi^2}}$$

$$\because I_m = \frac{V_{sm}}{R_f + R_L + R_s}$$

$$\boxed{P_{dc} = \frac{V_{sm}^2 R_L}{\pi^2 (R_f + R_L + R_s)^2}}$$

A.C. Power at load :-

The A.C. Power is given by

$$P_{ac} = I_{rms}^2 [R_L + R_f + R_s]$$

$$= \left(\frac{I_m}{2}\right)^2 (R_L + R_f + R_s)$$

$$\boxed{P_{ac} = \frac{I_m^2}{4} [R_L + R_f + R_s]}$$

Rectifier Efficiency (η) :-

It is ratio of D.C Power at o/p to A.C Power at input

$$\eta = \frac{\text{D.C. output power}}{\text{A.C. Input Power.}} = \frac{P_{dc}}{P_{ac}}$$

$$\eta = \frac{\frac{I_m^2}{\pi^2} R_L}{\frac{I_m^2}{4} [R_f + R_L + R_s]} = \frac{\frac{4}{\pi^2} R_L}{R_f + R_L + R_s}$$

$$\boxed{\eta = \frac{0.406 \, R_L}{[R_f + R_L + R_s]} \times 100\%}$$

$R_f + R_s \ll R_L$ $R_f + R_s$ is neglected

$$\eta = \frac{0.406}{R_L} \times R_L \times 100\ \%$$

$$\boxed{\eta = 40.6\ \%}$$

Very less (Poor) efficiency.

Ripple factor :-

It is ratio of R.M.S a.c component at output to Average (or) d.c component at output

$$\gamma = \frac{\text{R.M.S Value of a.c component at o/p}}{\text{Average (or) d.c component at o/p}}$$

$$= \frac{I_{ac}}{I_{dc}}$$

$$I_{rms} = \sqrt{I_{ac}^2 + I_{dc}^2}$$

$$I_{ac} = \sqrt{I_{rms}^2 - I_{dc}^2}$$

$$\gamma = \frac{\sqrt{I_{rms}^2 - I_{dc}^2}}{I_{dc}} = \sqrt{\frac{I_{rms}^2}{I_{dc}^2} - 1}$$

$$\gamma = \sqrt{\frac{\left(\frac{I_m}{2}\right)^2}{\left(\frac{I_m}{\pi}\right)^2} - 1}$$

$$= \sqrt{\frac{\pi^2}{4} - 1} = \sqrt{1.4674}$$

$$\gamma = 1.211$$

It indicate more a.c component than d.c Component at output.

Peak Inverse Voltage (PIV)

It is Maximum reverse bias voltage that can with stand by diode without breakdown (or) damage.

Transform Utilization Factor [T.U.F]

It is ratio of D.C. Power delivered to the load to A.C. Power rating of the transformer

$$T.U.F = \frac{\text{D.C Power delivered to the load}}{\text{A.C. Power rating of the transformer}}$$

$$T.U.F = \frac{\left(\frac{I_m}{\pi}\right)^2 R_L}{\left[\frac{V_{sm} I_m}{2\sqrt{2}}\right]}$$

Note

$V_{sm} = I_m R_L$

$$T.U.F = \frac{\frac{I_m^2}{\pi^2} R_L}{\frac{I_m \cdot I_m \cdot R_L}{2\sqrt{2}}} = \frac{2\sqrt{2}}{\pi^2}$$

$$\boxed{T.U.F = 0.287}$$

Voltage Regulation :-

Voltage Regulation is given by

$$= \frac{(V_{dc})_{NL} - (V_{dc})_{FL}}{(V_{dc})_{FL}}$$

$$(V_{dc})_{FL} = I_{dc} R_L = \frac{I_m}{\pi} R_L$$

$$(V_{dc})_{NL} = \frac{V_{sm}}{\pi} =$$

$$(V_{dc})_{FL} = \frac{V_{sm}}{\pi [R_f + R_s + R_L]} \times R_L$$

$$\% \text{ Voltage Regulation} = \frac{\frac{V_{sm}}{\pi} - \frac{V_{sm}}{\pi [R_f + R_s + R_L]} \times R_L}{\frac{V_{sm}}{\pi [R_f + R_s + R_L]} \times R_L} \times 100\%$$

$$= \frac{1 - \frac{R_L}{R_f + R_s + R_L}}{\frac{R_L}{R_f + R_s + R_L}} \times 100\%$$

$$\text{Voltage Regulation} = \frac{R_f + R_s}{R_L} \times 100\ \%$$

$$\%$$

$$R\ \%$$

Neglecting winding resistance

$$R\ \% = \frac{R_f}{R_L} \times 100\ \%$$

R_f = Diode forward Resistance

R_L – Load Resistance

6. Explain the working Principle of Full wave rectifier and derive the expression for I_{dc}, V_{dc}, I_{rms}, V_{rms}, ripple factor, efficiency and TUF.

A Circuit which Convert the a.c Voltage into Pulsating Voltage (or) current during both half cycle of input is known as "Full Wave Rectifier".

Two types of full wave rectifiers are

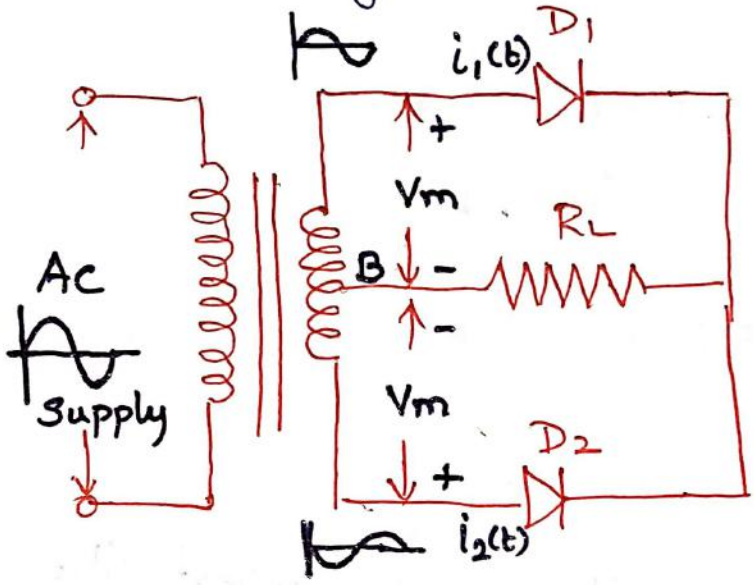
(1) Centre tapped transformer Full wave rectifier [FWR]

(2) Bridge retifier [FWR]

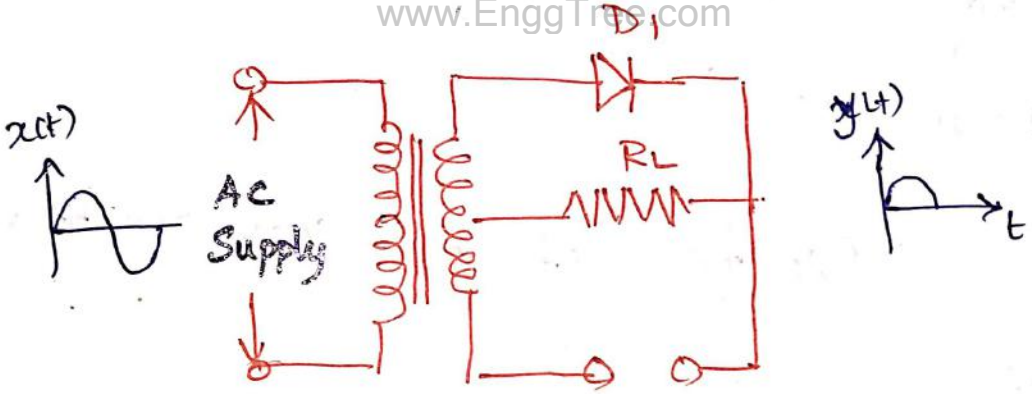
Centre tapped ~~Full~~ Transformer Full Wave rectifier [FWR]

It Contian two diodes to Convert a.c both half cycle to pulsating d.c..

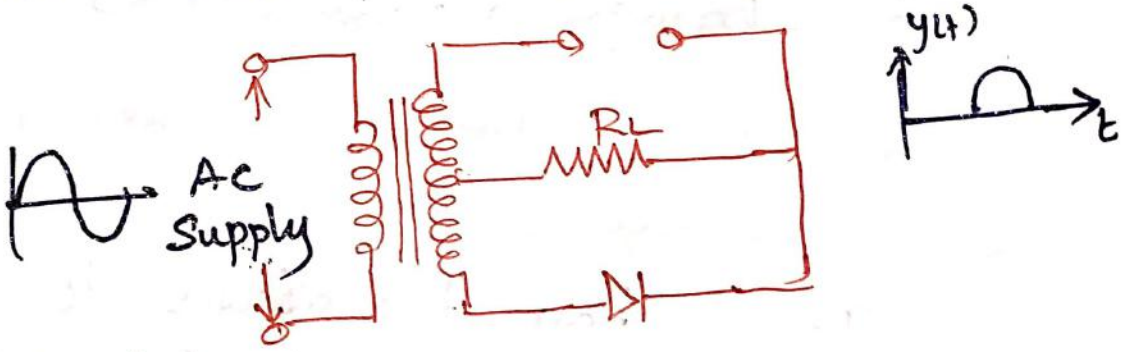
The centre tapped transformer FWR is shown in figure.

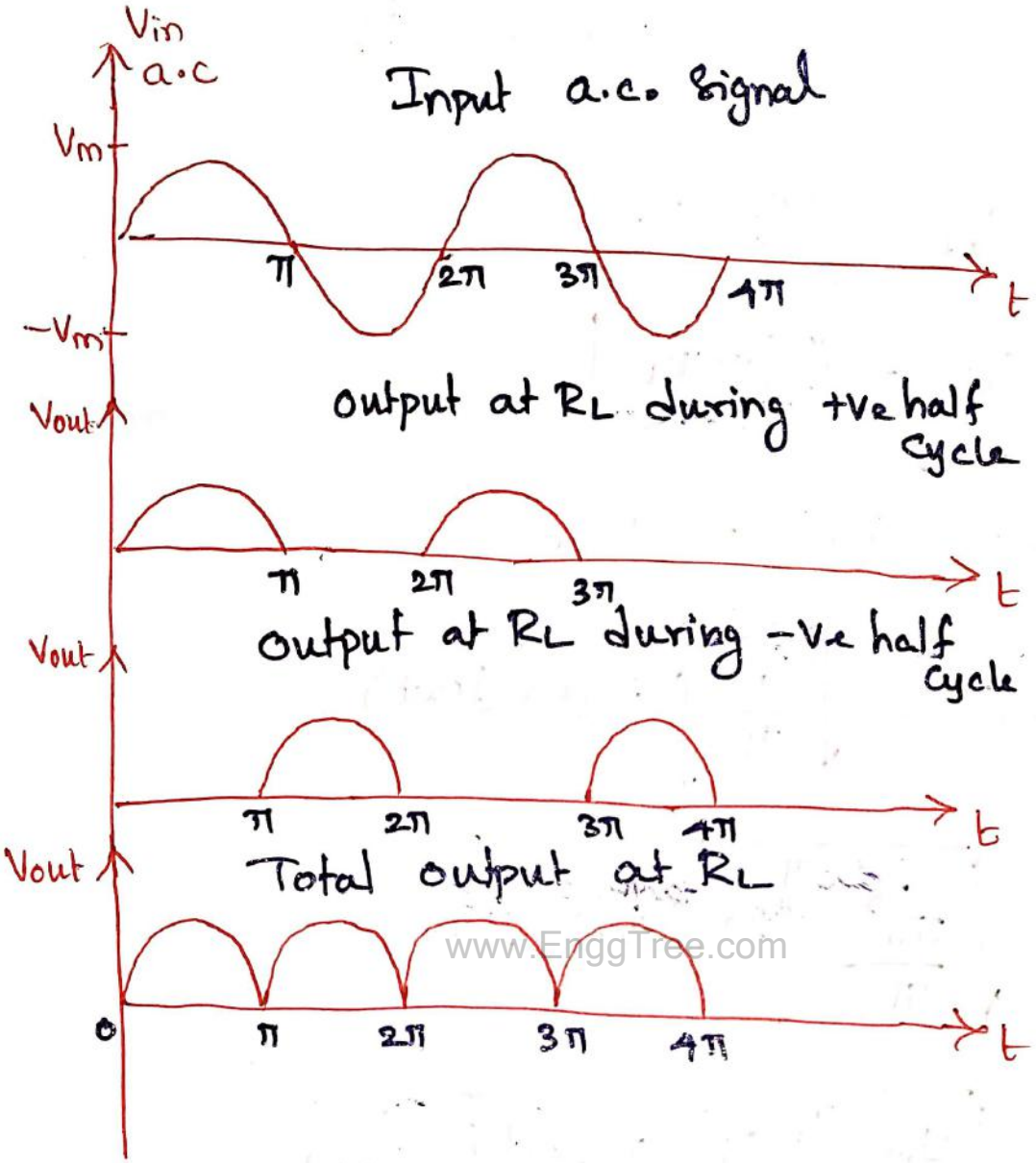


During Positive half cycle Diode D_1 conduct "ON" and Diode D_2 "OFF"



During negative half cycle Diode D_2 conduct "ON" and Diode D_1 "OFF"





Average (or) Dc Current $\frac{e}{o}$

$$I_{dc} = \frac{1}{\pi}\int_0^{\pi} I_m \sin(\omega t)\, d(\omega t)$$

$$= \frac{I_m}{\pi}\left[-\cos(\omega t)\right]_0^{\pi} = \frac{I_m}{\pi}\left[-\cos\pi + \cos 0\right]$$

$$= \frac{I_m}{\pi}\left[-(-1) + 1\right]$$

$$\boxed{I_{dc} = \frac{2I_m}{\pi}}$$

D.C. Voltage (or) Average Voltage $I_{d.c}$

$$V_{dc} = I_{dc} R_L$$

$$\boxed{V_{dc} = \frac{2 I_m}{\pi} R_L}$$

R.M.S. Current I_{rms}

$$I_{rms} = \sqrt{\frac{1}{\pi} \int_0^{\pi} i^2(t)\, d(\omega t)}$$

$$= \sqrt{\frac{I_m^2}{\pi} \int_0^{\pi} \sin^2(\omega t)\, d(\omega t)}$$

$$= \sqrt{\frac{I_m^2}{\pi} \int_0^{\pi} \left[\frac{1 - \cos(2\omega t)}{2}\right] d(\omega t)}$$

$$= \sqrt{\frac{I_m^2}{2\pi} \left[(\omega t) - \frac{\sin 2\omega t}{2}\right]_0^{\pi}}$$

$$= \sqrt{\frac{I_m^2}{2\pi} \left[\pi - \frac{\sin 2\pi}{2} - 0 + \frac{\sin 0}{2}\right]}$$

$$= \sqrt{\frac{I_m^2}{2\pi} [\pi]} \Rightarrow \boxed{I_{rms} = \frac{I_m}{\sqrt{2}}}$$

DC output Power :-

$$P_{dc} = I_{dc}^2 R_L = \left(\frac{2I_m}{\pi}\right)^2 R_L$$

$$\boxed{P_{dc} = \frac{4 I_m^2}{\pi^2} R_L}$$

Efficiency :-

$$\eta = \frac{P_{dc}}{P_{ac}}$$

$$P_{ac} = I_{rms}^2 (R_f + R_L)$$

$$P_{ac} = \frac{I_m^2}{2}(R_f + R_L)$$

$$\eta = \frac{\frac{4 I_m^2}{\pi^2} R_L}{\frac{I_m^2}{2}(R_f + R_L)}$$

$$= \frac{8}{\pi^2} \frac{R_L}{R_f + R_L}$$

$$\boxed{\eta = \frac{0.81}{1 + \frac{R_f}{R_L}} \times 100\ \%}$$

when $R_f \ll R_L$

$\frac{R_f}{R_L} \approx 0$

$$\boxed{\eta = 81\%}$$

Ripple factor :-

$$\gamma = \frac{I_{rrms}}{I_{dc}} = \frac{\sqrt{I_{rms}^2 - I_{dc}^2}}{I_{dc}^2}$$

$$= \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

$$= \sqrt{\frac{\left(\frac{I_m}{\sqrt{2}}\right)^2}{\left(\frac{2I_m}{\pi}\right)^2} - 1}$$

$$= \sqrt{\frac{\pi^2}{8} - 1}$$

$$\boxed{\gamma = 0.48}$$

Peak inverse voltage :-

$$\boxed{PIV = 2V_m}$$

Regulation :-

$$\text{Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\%$$

$$V_{NL} = V_{dc} = \frac{2V_m}{\pi}$$

$$V_{FL} = V_{dc} - I_{dc}(R_s + R_f)$$

$$\% \text{ Regulation} = \frac{V_{dc} - [V_{dc} - I_{dc}(R_s + R_f)]}{V_{dc} - I_{dc}[R_s + R_f)}$$

$$\% \text{ Regulation} = \frac{I_{dc}(R_s + R_f)}{I_{dc}(R_s + R_f + R_L) - I_{dc}(R_s + R_f)} \times 100$$

$$\% \text{ Regulation} = \frac{R_s + R_f}{R_L} \times 100\ \%$$

Transformer Utilisation factor :-

$$SUF = (TUF)_s = \frac{P_{dc}}{P_{ac\ rated}}$$

↑ Secondary Utilisation Factor

$$P_{ac\ rated} = V_{ac\ rated} \cdot I_{ac\ rated}$$

$$= V_{rms} \cdot I_{rms}$$

$$SUF = \frac{I_{dc}^2 R_L}{V_{rms} \cdot I_{rms}} = \frac{\left(\frac{2I_m}{\pi}\right)^2 \times R_L}{\frac{V_m I_m}{\sqrt{2}\sqrt{2}}}$$

$$= \frac{\frac{4 I_m^2}{\pi^2} R_L}{\frac{I_m^2}{2}(R_L + R_f)} \qquad \because V_m = I_m(R_L + R_f)$$

$$= \frac{8}{\pi^2}\left[\frac{R_L}{R_L + R_f}\right]$$

$$= \frac{8}{\pi^2}\left[\frac{1}{1 + \frac{R_f}{R_L}}\right] \times 100\%$$

$R_f << R_L \Rightarrow \frac{R_f}{R_L} \approx 0$

$$SUF = \frac{8}{\pi^2} \times 100\ \%$$

$$SUF = 81.1\ \%.$$

Advantage of FULL-WAVE Rectifier.

* Output voltage & transformer efficiency is high
* Lower ripple factor.

* Better voltage regulation.

Disadvantage :-

* bulky transformer
* PIV of diode is high.

Ec 3353 - Electronic Devices and Circuits

Unit - II Amplifiers

Load line, operating Point, biasing methods for BJT and MOSFET, BJT Small Signal model - Analysis of CE, CB, CC amplifier Gain and frequency response - MOSFET Small Signal model - Analysis of CS, CG and Source follower - Gain and frequency response - High frequency analysis.

PART - A

1. What are the different biassing techniques of BJT?

* Fixed Bias (or) Base Bias
* Collector to Base Bias
* Voltage divider Bias (or) Self Bias

---

2. What are the different regions of transistor?

* Cut-off region — Emitter bias reverse biase Collector bias forward bias
* Active region - Emitter bias forward bias Collector bias reverse bias
* Saturation region - Emitter-bias forward bias Collector bias forward bias

---

3. List the uses of emitter follower.

* Used for Impedance matching
* Used as a last stage amplifier in signal generator Circuits
* Current amplification without voltage gain.

4. Define alpha and beta of a transistor.

Alpha α :-

Alpha (α) is forward Current gain of Common Base Configuration

$$h_{fb} = \alpha = \frac{\text{output Current [CB config]}}{\text{input Current [CB Config]}}$$

$$\boxed{\alpha = \frac{I_C}{I_E}}$$

Beta β :-

Beta (β) is forward Current gain of Common Emitter Configuration

$$h_{fe} = \boxed{\beta = \frac{I_C}{I_B}}$$

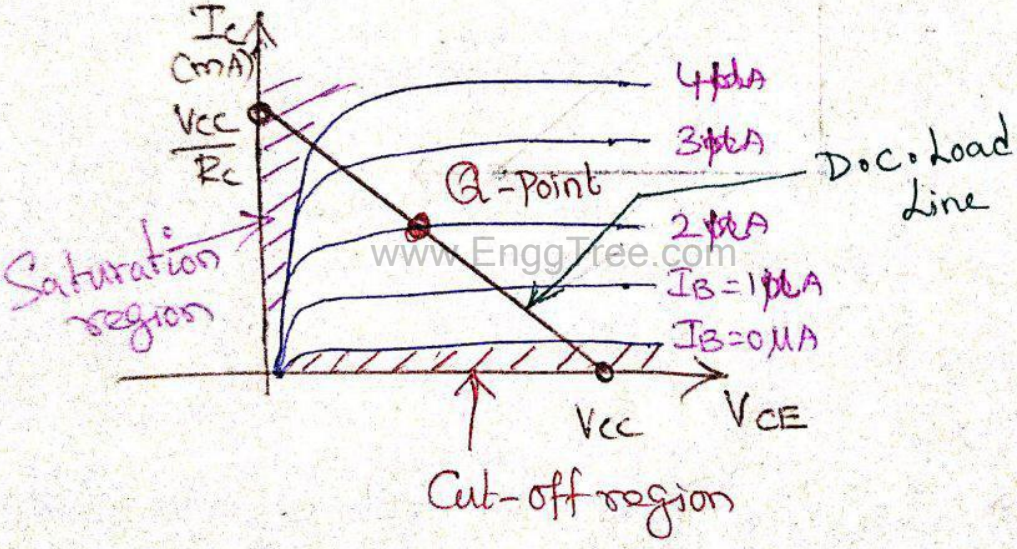
5. List out the different Configuration of BJT?

* Common Emitter Configuration
* Common Collector Configuration
* Common Base Configuration

6. what is operating Point?

It is a transistor operating Point in the d.c load line at output Characteristics of transistor at certain current [o/p current] and output voltage

It is also called as d.c. operating Point (or) quiescent point (or) bias point.

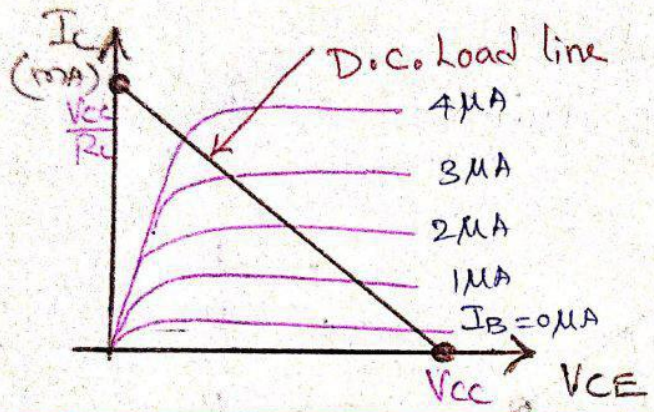


7. what are the advantages of fixed bias?

* Very simple circuit which uses very few components.
* The operating Point can be fixed anywhere in the active region by simply changing the value of R_B.

8. What is D.C Load line?

It is line drawn in the output characteristics of BJT. D.C. Load line is drawn by considering only d.c. supply [without a.c. signal at Input]

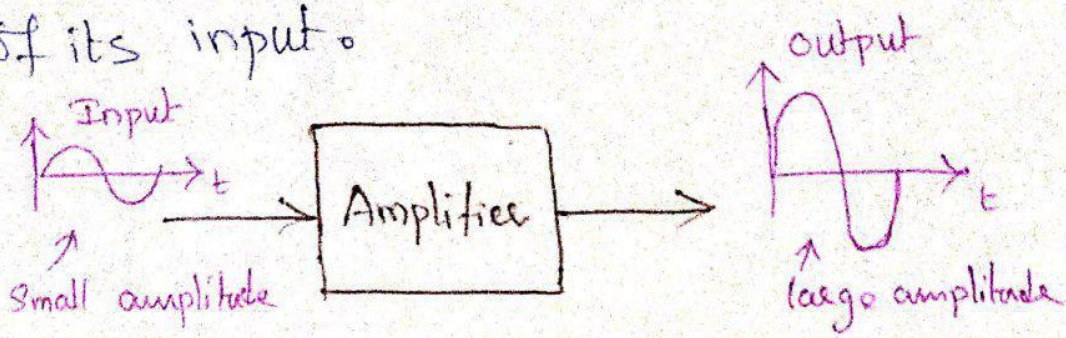


9. What is the necessary of Coupling Capacitor?

* Coupling Capacitor allow A.C. Input Signal to amplifier at input side
* Coupling Capacitor allow amplified A.C. Signal from amplifier to output [Load Resistor].
* Coupling not allow d.c. voltage Vcc to input and output side.

10. Define amplifier

Amplifier is a circuit that uses an external power supply to generate an output signal that is a large replica of its input.



11. How the MOSFET does has high input Impedance.

SiO_2 layer between Gate and Channel act as insulator, therefore only a small drain current flows, which means input impedance of a MOSFET is very high.

12. Define Stability factor for BJT.

It measures how Q-Point is stable at operating point

$$S = \frac{\partial I_C}{\partial I_{CBO}}\Big|_{\substack{V_{BE}\\ \beta \text{ constant}}} \qquad S' = \frac{\partial I_C}{\partial V_{BE}}\Big|_{\substack{I_{CBO}\\ \beta \text{ Constant}}} \qquad S'' = \frac{\partial I_C}{\partial \beta}\Big|_{\substack{V_{BE}\\ \beta \text{ Constant}}}$$

13. Why do you fix the operating point in the middle of the DC load line?

With Ac input signal operating point move along the load line

If Q-Point is fixed at middle of Load line we can Prevent Q-point moved to Cut-off and Saturation region with a.c. input signal. make transistor to stay in active region.

14. What are hybrid Parameters?

It is mixer of all Parameter.

h_i = input impedance

$h_i = \frac{\text{I/p voltage}}{\text{I/p current}}$

h_o = output admittance

$h_o = \frac{\text{output current}}{\text{output voltage}}$

h_r = reverse voltage gain

$h_r = \frac{\text{I/p voltage}}{\text{O/p voltage}}$

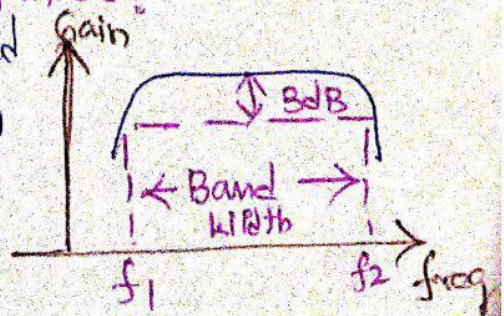
h_f = forward Current gain.

$h_f = \frac{\text{O/p Current}}{\text{I/p Current}}$.

15. What is bandwidth of amplifier?

Bandwidth of amplifier is defined as the difference between f_2 and f_1

$BW = f_2 - f_1$



Part - B

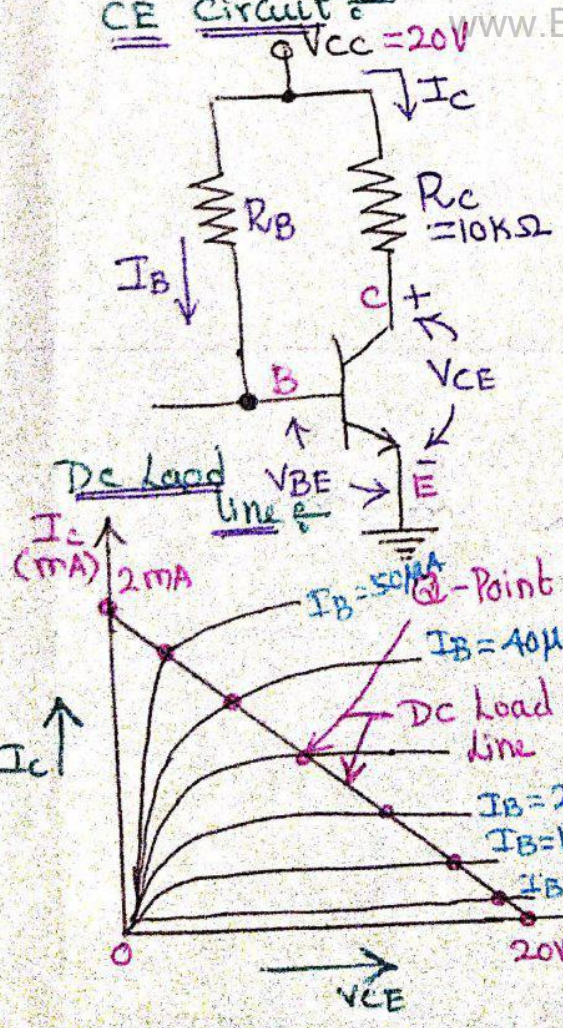
4. With a neat diagram explain DC Load Line and Bias Point for Q-Point?

DC Load Line

The dc load line for a transistor Circuit is a straight line drawn on the transistor output chasa -cteristics.

For a Common Emitter (CE) Circuit, the load line is a graph of collector Current (I_C) versus collector-emitter voltage (V_{CE}), for a given value of collector Resistance (R_C) and a given Supply Voltage(V_{CC})

CE Circuit



Consider the CE Circuit shown in figure. The dc load line for that CE Circuit is shown below to the Circuit.

From Figure - CE Circuit

$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CE} = V_{CC} - I_C R_C$$

when $I_C = 0$

$$V_{CE} = V_{CC} - 0 R_C$$

$$V_{CE} = V_{CC} = 20\,V$$

$\boxed{V_{CE} = 20\,V}$

when $V_{CE} = 0$

$$0 = V_{CC} - I_C R_C$$

$$I_C R_C = V_{CC}$$

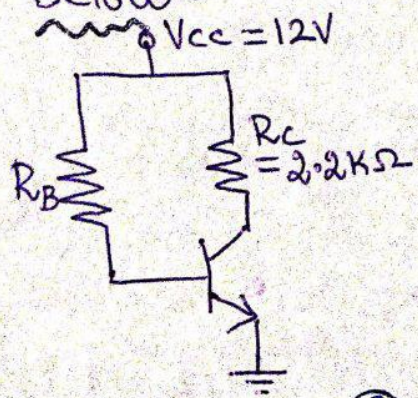
$$I_C = \frac{V_{CC}}{R_C} = \frac{20\,V}{10 \times 10^3\,\Omega}$$

$$I_C = 2 \times 10^{-3}$$

$\boxed{I_C = 2\,mA}$

Problem 1 :-

Draw a DC Load line of Circuit Shown below.



Given :- $V_{CC} = 12V$, $R_C = 2.2K\Omega$

$V_{CC} = I_C R_C + V_{CE}$

when $V_{CE} = 0$

$12 = I_C\ 2.2K\Omega + 0$

$I_C = \frac{12}{2.2K\Omega} = 5.45\ mA$

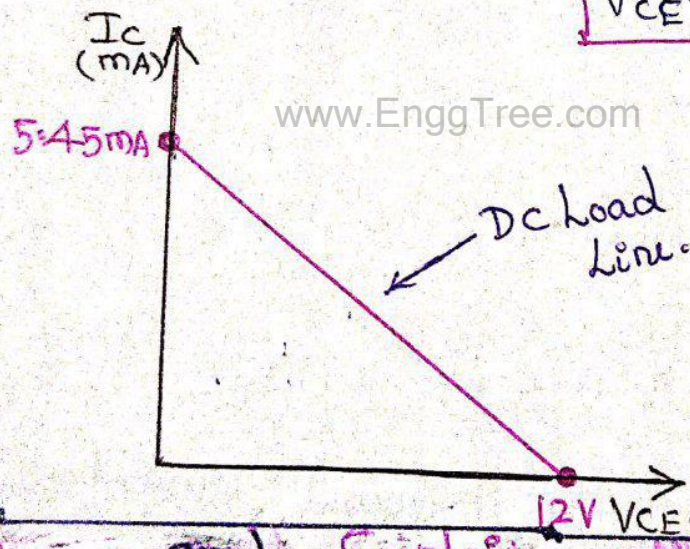
$I_C = 5.45mA$

when $I_C = 0$

$12 = 0 \times 2.2K\Omega + V_{CE}$

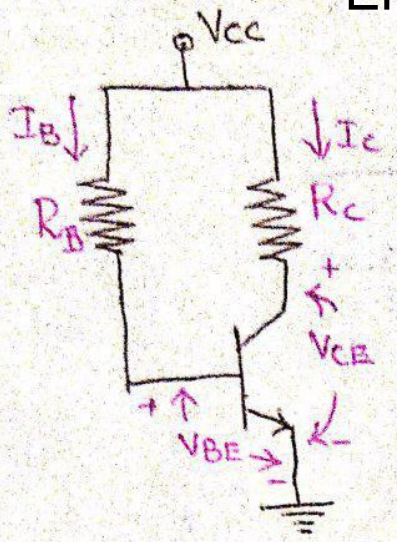
$V_{CE} = 12V$

$V_{CE} = 12V$



2. Draw and Explain with a neat diagram the Fixed Bias (or) Base Bias. Also derive the Stability factors.

The transistor bias arrangement shown in figure is known as fixed current bias and also base bias.



From the figure

$$V_{cc} = I_C R_C + V_{CE} \quad -(1)$$

$$V_{cc} = I_B R_B + V_{BE} \quad -(2)$$

$$I_B = \frac{V_{cc} - V_{BE}}{R_B}$$

$$I_C = \frac{V_{cc} - V_{CE}}{R_C}$$

The base-emitter Voltage V_{BE} is taken as 0.7V for a Silicon transistor and as 0.3V for a germanium transistor.

The Collector Current is given by

$$I_C = h_{fe} I_B = \beta I_B$$

$I_C = \beta I_B + (1+\beta) I_C$

h_{fe} (or) β is forward Current gain is given as $\beta = \frac{I_C}{I_B}$

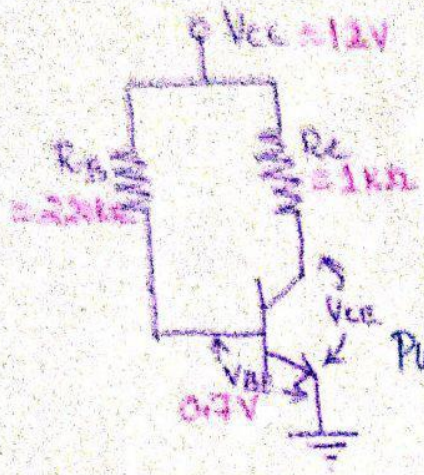
Problem 2 :

The base bias Circuit has $R_B = 220k\Omega$, $R_C = 1k\Omega$, $V_{cc} = 12V$ and transistor has $h_{fe} = 100$. Assume $V_{BE} = 0.7V$ Determine I_B, I_C and V_{CE} also Draw DC load line & Q Point.

(10) (10)

Solution :-

Given $R_B = 220k\Omega$, $R_C = 1k\Omega$, $V_{CC} = 12V$ and $h_{fe} = 100$. $V_{BE} = 0.7V$



$V_{CC} = I_C R_C + V_{CE}$

To find Dc load line

Put $V_{CE} = 0$

$V_{CC} = I_C R_C + 0$

$12 = I_C 1k\Omega$

$I_C = \frac{12}{1k\Omega} = 12mA$

$I_C = 12mA$

Put $I_C = 0$

$V_{CC} = 0 R_C + V_{CE}$.

$12 = V_{CE}$

$V_{CE} = 12V$.

We know that

$V_{CC} = I_B R_B + V_{BE}$.

$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 - 0.7}{220k\Omega}$

$= \frac{11.3}{220k\Omega} = 5.136\mu A$

$I_B = 5.136\mu A$

(11)

$I_C = \beta I_B$

$= 100 \times 51.36\ \mu A$

$I_C = 5.136\ mA$

At Q-Point $I_C \Rightarrow I_{CQ} = 5.136\ mA$

$V_{CC} = I_C R_C + V_{CE}$.

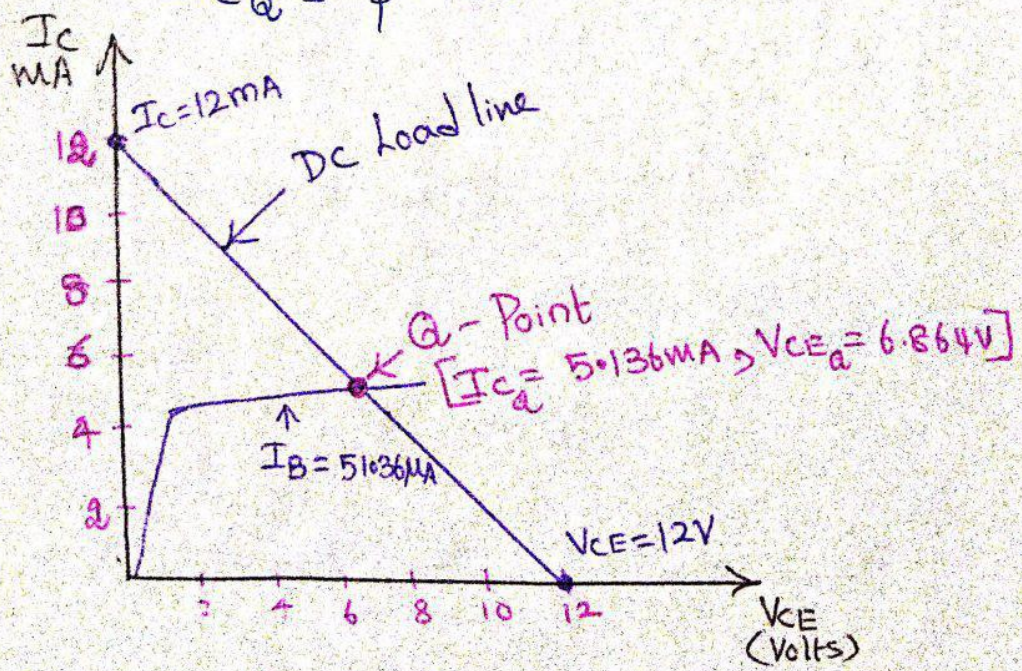
$12 = 5.136\ mA \times 1\ K\Omega + V_{CE}$

$V_{CE} = 12 - 5.136 \times 10^{-3} \times 1 \times 10^{3}$

$V_{CE} = 6.864\ V$

Thus Q-Point is

$I_{CQ} = 5.136\ mA$ $V_{CEQ} = 6.864V$



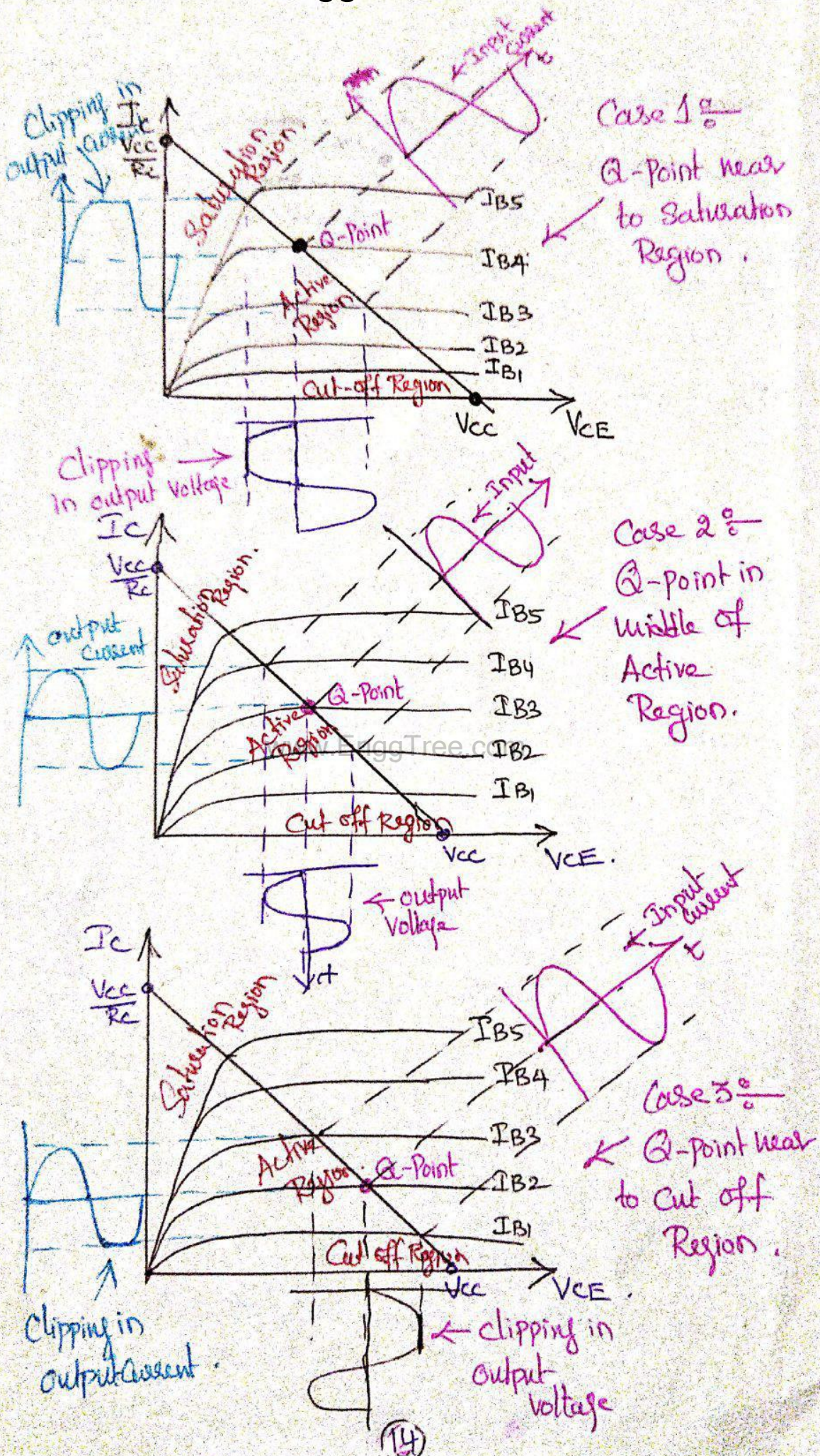
Dc Bias Point (or) Q-Point (or) dc operating Point (or) quiescent Point

Q-Point identifies the transistor Collector Current and Collector-emitter Voltage when there is no input signal at the base terminal.

The operating Point must be stable for Proper operation of the transistor. However, the Q-Point vary with temperature (I_{CBO} (Collector-base leakage Current, β forward Current gain, V_{BE} Base-Emitter Voltage).

when transistor is used as an amplifier, the Q-Point Should be selected at the Center of the dc load line to Prevent any Possible distortion in the amplified output signal. unwanted clipping Can be avoided in the output.

This is well-understood by three different diagram with three different Q-Points.



Stability Factor

The Stability factor indicates the degree of change in Operating Point due to Variation in temperature [which Causes the Variation of β, I_{CBO} and V_{BE}]

∴ The change in temperature affect the following Parameters of the transistor

* I_{CBO}
* V_{BE}
* β

and Stability factor for this three Parameters as below.

$$S = \frac{\partial I_C}{\partial I_{CBO}} \Big|_{V_{BE}, \beta \text{ Constant}}$$

$$S' = \frac{\partial I_C}{\partial V_{BE}} \Big|_{I_{CBO}, \beta \text{ Constant}}$$

$$S'' = \frac{\partial I_C}{\partial \beta} \Big|_{I_{CBO}, V_{BE} \text{ Constant}}$$

Stability S for Fixed bias :-

For a Common emitter Configuration Collector Current is given as

$$I_c = \beta I_B + (1+\beta) I_{CBO}$$

Diff. w.r.t I_{CBO}

$$\frac{\partial I_c}{\partial I_{CBO}} = \beta \frac{\partial I_B}{\partial I_{CBO}} + (1+\beta)\frac{\partial I_{CBO}}{\partial I_{CBO}}$$

÷ by ∂I_c

$$1 = \beta \frac{\partial I_B}{\partial I_c} + (1+\beta)\frac{\partial I_{CBO}}{\partial I_c}$$

$$1 - \beta \frac{\partial I_B}{\partial I_c} = (1+\beta)\frac{\partial I_{CBO}}{\partial I_c}$$

$$\frac{\partial I_{CBO}}{\partial I_c} = \frac{1 - \beta \frac{\partial I_B}{\partial I_c}}{1+\beta} = \frac{1}{S}$$

$$\frac{1}{S} = \frac{1 - \beta \frac{\partial I_B}{\partial I_c}}{1+\beta}$$

$$S = \frac{1+\beta}{1 - \beta \frac{\partial I_B}{\partial I_c}}$$

We Know that

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_B \approx \frac{V_{CC}}{R_B}$$

$$\frac{\partial I_B}{\partial I_C} = 0$$

Substituting this Value in Stability equ

$$S = \frac{1+\beta}{1-\beta\left(\frac{\partial I_B}{\partial I_C}\right)} = \frac{1+\beta}{1-\beta(0)}$$

$$\boxed{S = 1+\beta}$$

Stability S' for Fixed bias $\frac{0}{0}$

$$S' = \frac{\partial I_C}{\partial V_{BE}}\Big|_{I_{CBO},\ \beta \text{ Constant}}$$

$$I_C = \beta I_B + (1+\beta) I_{CBO}$$

$$I_C = \beta \frac{(V_{CC} - V_{BE})}{R_B} + (1+\beta) I_{CBO}$$

$$I_C = \beta \frac{V_{CC}}{R_B} - \beta \frac{V_{BE}}{R_B} + (1+\beta) I_{CBO}$$

Diff. w.r.t V_{BE}

$$\frac{\partial I_C}{\partial V_{BE}} = 0 - \frac{\beta}{R_B} + 0$$

$$S' = \frac{-\beta}{R_B}$$

Stability Factor S'' for fixed bias :-

$$S'' = \left.\frac{\partial I_C}{\partial \beta}\right|_{V_{BE}, I_{CBO}\ \text{Constants.}}$$

$$I_C = \beta I_B + (1+\beta) I_{CBO}$$

$$I_C = \beta\left(\frac{V_{CC} - V_{BE}}{R_B}\right) + (1+\beta) I_{CBO}$$

$$I_C = \beta \frac{V_{CC}}{R_B} - \beta \frac{V_{BE}}{R_B} + (I_{CBO} + \beta I_{CBO})$$

diff. w.r. to β

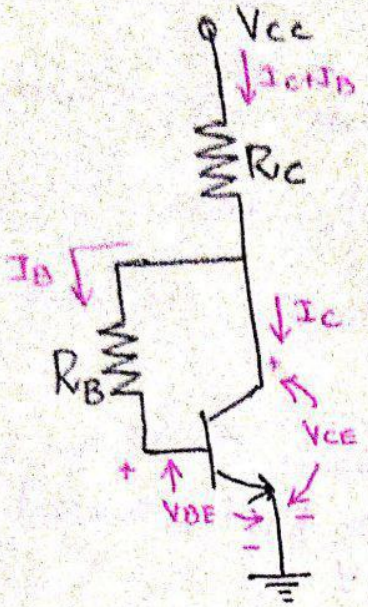
$$\frac{\partial I_C}{\partial \beta} = \frac{V_{CC}}{R_B} - \frac{V_{BE}}{R_B} + 0 + I_{CBO}$$

$$\frac{\partial I_C}{\partial \beta} = \frac{V_{CC} - V_{BE}}{R_B} + I_{CBO}$$

$$S'' = I_B + I_{CBO} = \frac{I_C}{\beta} + \cancel{I_{CBO}}$$ (neglected)

$$S'' = \frac{I_C}{\beta}$$

2. Draw a Neat Diagram and Explain Collector to Base Bias? Find its Stability [Self Bias]



It is also called as Base bias with collector feedback (or) Collector feedback bias.

$$V_{CC} = (I_C + I_B)R_C + V_{CE} \quad -(1)$$

$$V_{CE} = V_{BE} + I_B R_B \quad -(2)$$

$$I_B = \frac{V_{CE} - V_{BE}}{R_B} \quad -(3)$$

$$V_{CE} = V_{CC} - R_C(I_C + I_B) \quad -(4)$$

$$h_{fe} = \beta = \frac{I_C}{I_B}$$

$$V_{BE} + I_B R_B = V_{CC} - (I_C + I_B)R_C.$$

$$I_C = h_{fe} I_B.$$

$$V_{BE} + I_B R_B = V_{CC} - (h_{fe} I_B + I_B)R_C$$

$$(1 + h_{fe})I_B R_C + I_B R_B = V_{CC} - V_{BE}$$

$$I_B [R_C(1 + h_{fe}) + R_B] = V_{CC} - V_{BE}.$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + R_C[1+h_{fe}]}$$

Problem 3 :-

Calculate the maximum & minimum levels of I_C, and V_{CE} for the bias Circuit use for Collector to Base bias. when

$\beta_{(min)} = 50$ and $\beta_{(max)} = 200$.

$[R_C = 2.2K\Omega$ & $R_B = 270K\Omega]$

$V_{CC} = 18V$

Solution :-

Given

$R_C = 2.2K\Omega$ | $\beta_{(min)} = 50$

$R_B = 270K\Omega$ | $\beta_{(max)} = 200$

For maximum value

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + R_C(\beta+1)} = \frac{18 - 0.7}{270K\Omega + 2.2K\Omega(50+1)}$$

$$I_B = 45.26\mu A$$

$$I_C = \beta I_B = 50 \times 45.26\mu A$$

$$I_{C_{MAX}} = 2.26mA$$

$$V_{CE} = V_{cc} - R_c(I_c + I_B)$$

$$= 18 - 2.2\,K\Omega\,(2.26\,mA + 19.26\,\mu A)$$

$$V_{CE_{Max}} = 12.9\,V$$

For minimum Value

$$I_B = \frac{V_{cc} - V_{BE}}{R_B + R_c(\beta+1)} = \frac{18 - 0.7}{270K + 2.2K(200+1)}$$

$$I_B = 24.3\,\mu A$$

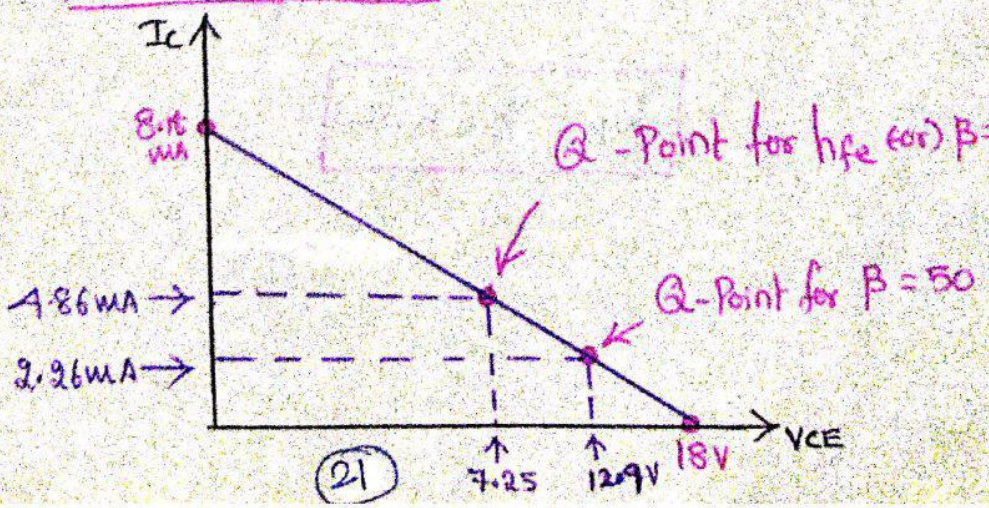
$$I_c = \beta I_B = 200 \times 24.3\,\mu A$$

$$I_c = 4.86\,mA$$

$$V_{CE} = V_{cc} - R_c(I_c + I_B)$$

$$= 18 - 2.2K\,(4.86\,mA + 24.3\,\mu A)$$

$$V_{CE} = 7.25\,V$$



Problem 4 :-

Design a Collector to base bias Circuit for the Specified Conditions :

$V_{CC} = 15V$, $V_{CE} = 5V$, $I_C = 5mA$ and $\beta = 100$

Solution :-

$$I_B = \frac{I_C}{\beta} = \frac{5mA}{100} = 50\mu A$$

$$V_{CE} = V_{CC} - (I_B + I_C) R_C$$

$$R_C = \frac{V_{CC} - V_{CE}}{I_B + I_C} = \frac{15 - 5}{50 \times 10^{-6} + 5 \times 10^{-3}}$$

$$\boxed{R_C = 1.98K\Omega}$$

$$V_{CE} - I_B R_B - V_{BE} = 0$$

$$R_B = \frac{V_{CE} - V_{BE}}{I_B} = \frac{5 - 0.7}{50 \times 10^{-6}}$$

$$\boxed{R_B = 86K\Omega}$$

Stability factor for Collector to Base bias ckt

$$S = \frac{\partial I_c}{\partial I_{CBO}} \Big|_{V_{BE}, \beta \text{ are Constant}}$$

$$S' = \frac{\partial I_c}{\partial V_{BE}} \Big|_{I_{CBO}, \beta \text{ are Constant}}$$

$$S'' = \frac{\partial I_c}{\partial \beta} \Big|_{I_{CBO}, V_{BE} \text{ are Constant.}}$$

Stability S ckt

$$S = \frac{\partial I_c}{\partial I_{CBO}}$$

$$I_c = \beta I_B + (1+\beta) I_{CBO}$$

diff. w.r.t I_c

$$1 = \beta \frac{\partial I_B}{\partial I_c} + (1+\beta) \frac{\partial I_{CBO}}{\partial I_c}$$

$$1 - \beta \frac{\partial I_B}{\partial I_c} = (1+\beta) \frac{1}{S}$$

$$S = \frac{1+\beta}{1 - \beta \frac{\partial I_B}{\partial I_c}} \quad \text{——} (1)$$

$$V_{cc} = I_C R_C + (I_B R_C + I_B R_B + V_{BE}$$

Diff. w.r.t I_C

$$0 = R_C + \frac{\partial I_B}{\partial I_C}(R_C + R_B) + 0$$

$$-R_C = \frac{\partial I_B}{\partial I_C}(R_C + R_B)$$

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_C}{R_C + R_B} \quad \text{——} (2)$$

Sub (2) in (1)

$$S = \frac{1+\beta}{1 + \frac{R_C}{R_C + R_B}\beta}$$

Stability $S' \to \frac{0}{0}$

$$S' = \frac{\partial I_C}{\partial V_{BE}} \Big| \; I_{CBO}, \beta \text{ Constant.}$$

$$V_{cc} = (R_B + R_C) I_B + I_C R_C + V_{BE}.$$

$$I_B = \frac{V_{cc} - I_C R_C - V_{BE}}{R_C + R_B} \quad (24)$$

$$\frac{I_c}{\beta} = \frac{V_{cc} - I_c R_c - V_{BE}}{R_c + R_B}$$

$$\frac{I_c}{\beta} + \frac{I_c R_c}{R_c + R_B} = \frac{V_{cc} - V_{BE}}{R_c + R_B}$$

$$I_c \left[\frac{1}{\beta} + \frac{R_c}{R_c + R_B} \right] = \frac{V_{cc} - V_{BE}}{R_c + R_B}$$

$$I_c \left[\frac{(R_c + R_B) + \beta R_c}{\beta (R_c + R_B)} \right] = \frac{V_{cc} - V_{BE}}{(R_c + R_B)}$$

$$I_c = \frac{\beta \left[V_{cc} - V_{BE} \right]}{\beta R_c + (R_c + R_B)}$$

Diff. w.r.t V_{BE}

$$\frac{\partial I_c}{\partial V_{BE}} = \frac{-\beta}{R_c(1+\beta) + R_B}$$

$$S' = \frac{-\beta}{R_B + (1+\beta) R_c}$$

Stability factor S'' $\frac{0}{0}$

$$S'' = \frac{\partial I_c}{\partial \beta} \Big| \; I_{CBO}, V_{BE} \text{ are Constant.}$$

$$V_{CC} - (I_C + I_B)R_C - I_B R_B = 0$$

$-V_{BE}$

$$V_{CC} = (I_C + I_B)R_C + I_B R_B + V_{BE}$$

$$= (\beta I_B + I_B)R_C + I_B R_B + V_{BE}$$

$$= I_B(\beta R_C + R_C + R_B) + V_{BE}$$

$$V_{CC} - V_{BE} = I_B((1+\beta)R_C + R_B)$$

$$I_B = \frac{V_{CC} - V_{BE}}{(1+\beta)R_C + R_B}$$

$$I_C = \beta\left[\frac{V_{CC} - V_{BE}}{(1+\beta)R_C + R_B}\right]$$

$$\frac{\partial I_C}{\partial \beta} = \frac{[(1+\beta)R_C + R_B][V_{CC} - V_{BE}] - \beta[V_{CC} - V_{BE}](0+1)R_C}{[(1+\beta)R_C + R_B]^2}$$

Note

$$\frac{u}{v}' = \frac{vu' - uv'}{v^2}$$

$$S'' = \frac{[R_C + \beta R_C + R_B][V_{CC} - V_{BE}] - \beta R_C[V_{CC} - V_{BE}]}{[(1+\beta)R_C + R_B][(1+\beta)R_C + R_B]}$$

$$S'' = \frac{R_C(V_{CC} - V_{BE}) + \beta R_C(V_{CC} - V_{BE}) + R_B(V_{CC} - V_{BE}) - \beta R_C(V_{CC} - V_{BE})}{[(1+\beta)R_C + R_B][(1+\beta)R_C + R_B]}$$

$$S'' = \frac{I_c}{\beta}$$

$$S'' = \frac{(R_c + R_B)\left(\frac{I_c}{\beta}\right)}{((1+\beta)R_c + R_B)}$$

$$S'' = \frac{(R_c + R_B)(V_{CC} - V_{BE})}{((1+\beta)R_c + R_B)}$$

$$\boxed{S'' = \frac{I_c (R_c + R_B)}{\beta[(1+\beta)R_c + R_B]}}$$

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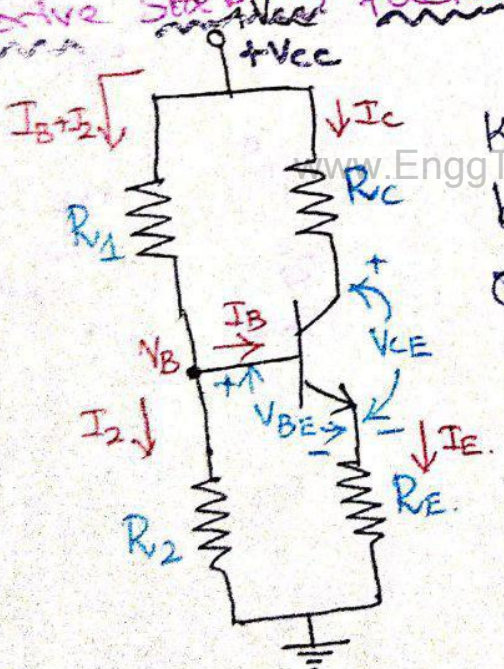
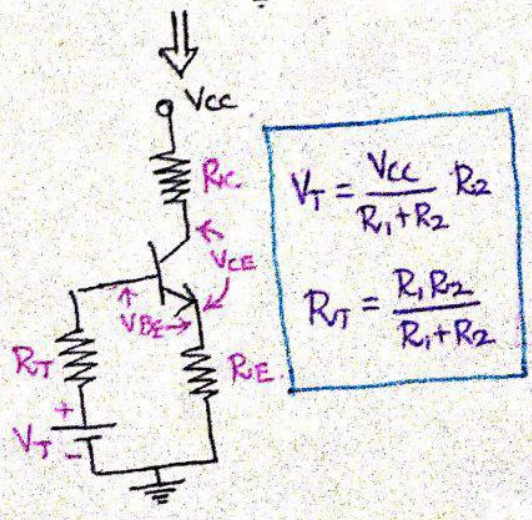
4. Draw Voltage Divider Bias and Explain? Also Derive Stability factor.



Voltage divider Bias, also known as emitter current bias, is the most stable of the three basic transistor bias circuits.

$$V_{CC} = I_c R_c + V_{CE} + I_E R_E \quad \text{—(1)}$$

$$V_{CC} = (I_B + I_2) R_1 + I_2 R_2 \quad \text{—(2)}$$



$$V_T = \frac{V_{CC}}{R_1 + R_2} R_2$$

$$R_T = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_B = \frac{V_{CC}}{R_1 + R_2} R_2 \quad \text{—(3)}$$

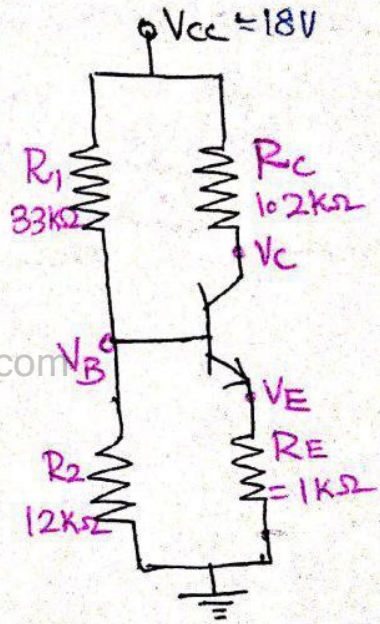
$$V_E = V_B - V_{BE} \quad \text{—(4)}$$

$$I_E = \frac{V_B - V_{BE}}{R_E} \quad \text{—(5)}$$

Problem 5°

Analyse the Voltage divider bias Circuit with $R_C = 1.2K\Omega$, $R_E = 1K\Omega$, $R_1 = 33K\Omega$ and $R_2 = 12K\Omega$ when the transistor $h_{fe} = 100$. Determine V_B, V_E, I_E, I_C, V_C and V_{CE}.

Solution °



$$V_T = V_B = \frac{V_{CC} R_2}{R_1 + R_2} =$$

$$= \frac{18V \times 12 \times 10^3}{(33 \times 10^3 + 12 \times 10^3)}$$

$$\boxed{V_T = V_B = 4.8V}$$

$$V_E = V_B - V_{BE}$$

$$= 4.8 - 0.7$$

$$\boxed{V_E = 4.1V}$$

$$R_T = \frac{R_1 R_2}{R_1 + R_2} = \frac{33 \times 10^3 + 12 \times 10^3}{(33 \times 10^3 + 12 \times 10^3)}$$

$$\boxed{R_T = 8.8K\Omega}$$

$$I_B = \frac{V_T - V_{BE}}{R_T + R_E(1+h_{fe})} = \frac{4.8V - 0.7}{8.8\times10^3 + 1\times10^3(1+100)}$$

$$I_B = 37.3\ \mu A$$

$$I_C = \beta I_B = h_{fe} I_B = 100 \times 37.3\mu A$$

$$I_C = 3.73\ mA$$

$$I_E = I_B + I_C = 37.3\mu A + 3.73\ mA$$

$$I_E = 3.77\ mA$$

$$V_E = I_E R_E = 3.77mA \times 1\times10^3$$

$$V_E = 3.77V$$

$$V_C = V_{CC} - I_C R_C$$

$$= 18V - (3.73\times10^{-3}\times1.2\times10^3)$$

$$V_C = 13.52\ V$$

$$V_{CE} = V_C - V_E$$

$$= 13.52 - 3.77$$

$$V_{CE} = 9.75$$

Stability factor

$$S = \frac{\partial I_C}{\partial I_{CBO}}\Bigg|_{V_{BE},\beta \text{ Constant}}$$

$$S = \frac{1+\beta}{1+\beta\left(\frac{\partial I_B}{\partial I_C}\right)}$$

$$V_{Th} = I_B R_B + V_{BE} + (I_B + I_C) R_E.$$

Diff. w.r.t I_C

$$0 = \frac{\partial I_B}{\partial I_C} R_B + 0 + \left(\frac{\partial I_B}{\partial I_C} + 1\right) R_E.$$

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_B + R_E}.$$

$$S = \frac{1+\beta}{1+\beta\left[\frac{R_E}{R_B+R_E}\right]}$$

Stability Factor S'

$$S' = \frac{\partial I_C}{\partial V_{BE}}\Bigg|_{I_{CBO},\beta \text{ Constant}}$$

$$I_C = (1+\beta) I_{CBO} + \beta I_B$$

$$I_B = \frac{I_C - (1+\beta) I_{CBO}}{\beta}$$

$$V_{BE} = V_{th} - (R_E + R_B) I_B - R_E I_C$$

$$V_{BE} = V_{th} - \frac{(R_E + R_B)\left[I_C - (1+\beta) I_{CBO}\right]}{\beta} - R_E I_C$$

$$= V_{th} - \frac{(R_E + R_B) I_C}{\beta} + \frac{(R_E + R_B)(1+\beta) I_{CBO}}{\beta} - R_E I_C$$

$$V_{BE} = V_{th} - \frac{\left[(1+\beta) R_E + R_B\right] I_C}{\beta} + \frac{\left[R_E + R_B\right](1+\beta) I_{CBO}}{\beta}$$

Diff. w.r.t. V_{BE}.

$$1 = 0 - \frac{\left[R_B + (1+\beta) R_E\right]}{\beta} \frac{\partial I_C}{\partial V_{BE}} + 0$$

$$\boxed{\frac{\partial I_C}{\partial V_{BE}} = S' = \frac{-\beta}{R_B + (1+\beta) R_E}.}$$

Stability factor S'' :-

$$S'' = \left.\frac{\partial I_C}{\partial \beta}\right|_{I_{CBO},\ V_{BE}\ \text{Constant}}$$

We know that

$$V_{BE} = V_{th} - \frac{\left[R_B + (1+\beta) R_E\right]}{\beta} I_C + \frac{\left[R_E + R_B\right](1+\beta) I_{CBO}}{\beta}$$

$$V_{BE} = V_{th} - \frac{[R_B + (1+\beta) R_E]}{\beta} I_C + V'$$

where

$$V' = \left[\frac{(R_B + R_E)(\beta+1)}{\beta}\right] I_{CBO}$$

$$V' \simeq [R_B + R_E] I_{CBO}$$

$$I_C = \beta \frac{(V_{th} + V' - V_{BE})}{R_B + R_E (1+\beta)}$$

diff. w.r.t. β.

$$\frac{u}{v} = \frac{vu' - uv'}{v^2}$$

$$\frac{\partial I_C}{\partial \beta} = \frac{[R_B + R_E(1+\beta)][V_{th} + V' - V_{BE}] - \beta(V_{th} + V' - V_{BE}) R_E}{[R_B + R_E(1+\beta)]^2}$$

$\times (1+\beta)$ in numerator and denominator

$$= \frac{(1+\beta)(R_B + R_E)(V_{th} + V' - V_{BE})}{(1+\beta)[R_B + R_E(1+\beta)][R_B + R_E(1+\beta)]}$$

$$\frac{\partial I_C}{\partial \beta} = \frac{S (V_{th} + V' - V_{BE})}{(1+\beta)[R_B + R_E(1+\beta)]} \times \frac{\beta}{\beta}$$

$$S'' = \frac{S I_C}{\beta(1+\beta)}$$

Problem 6 :-

Design a voltage divider bias circuit for the specified condition $V_{cc} = 12\,V$, $V_{CE} = 6\,V$, $I_C = 1\,mA$, $S = 20$, $\beta = 100$ and $V_E = 1\,V$

Solution :-

$$I_B = \frac{I_C}{\beta} = \frac{1 \times 10^{-3}}{100} = 10\,\mu A$$

$$I_E = I_B + I_C = 10\,\mu A + 1\,mA$$

$$I_E = 1.01\,mA$$

$$R_E = \frac{V_E}{I_E} = \frac{1\,V}{1.01\,mA} = 990\,\Omega.$$

$$R_C = \frac{V_{cc} - V_{CE} - V_E}{I_C} = \frac{12 - 6 - 1}{1\,mA} = 5\,K\Omega$$

$$S = \frac{1+\beta}{1+\beta \frac{R_E}{R_E + R_B}}$$

$$20 = \frac{1+100}{1+100\left(\frac{990}{990+R_B}\right)}$$

$$\therefore \quad R_B = 23454\,\Omega \quad (33)$$

$$\frac{R_1 R_2}{R_1 + R_2} = 23454\ \Omega$$

$$V_B = V_E + V_{BE} = 1.7\ V$$

$$R_1 = \frac{V_{CC} - V_B}{I + I_B} \qquad R_2 = \frac{1.7}{I}$$

$$R_B = 23454 = \frac{\left(\frac{10.3}{I+I_B}\right)\left(\frac{1.7}{I}\right)}{\frac{10.3}{I+I_B} + \frac{1.7}{I}}$$

$$23454 = \frac{\frac{17.51}{\cancel{I(I+I_B)}}}{\frac{10.3I + 1.7I + 1.7I_B}{\cancel{I(I+I_B)}}}$$

$$241576.2\,I + 398711.8\,I + 398711.8\,I_B = 17.51$$

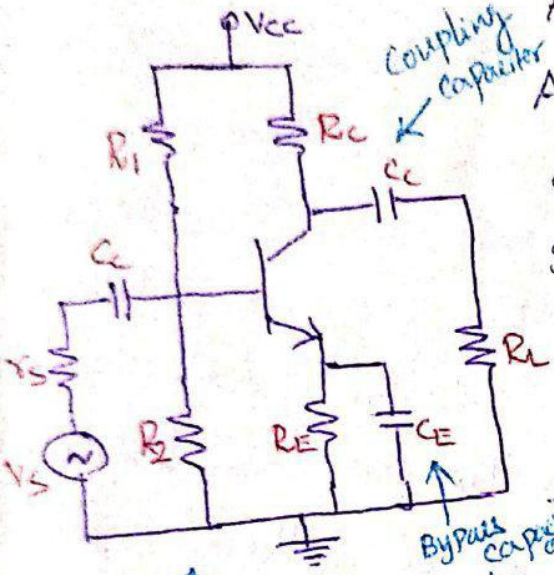
$$I = 60.797\ \mu A$$

$$R_1 = \frac{10.3}{I + I_B} = \frac{10.3}{60.797 \times 10^{-6} + 10 \times 10^{-6}} = 145.486\ k\Omega$$

$$R_2 = \frac{1.7}{60.797 \times 10^{-6}} = 27961.9\ \Omega$$

5. Explain AC equivalent circuit with neat diagram for Common Emitter Amplifier?

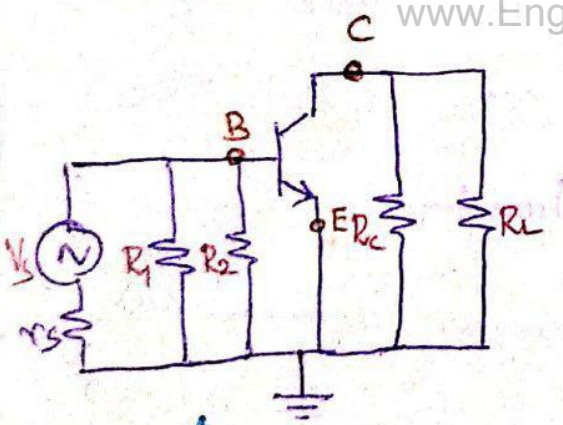
AC Equivalent Circuit of Common Emitter Amplifier.



CE Amplifier Circuit.

A Simple Common Emitter Amplifier with Coupling and bypass capacitor is shown in figure.

To get a AC equivalent Circuit capacitor behaves as short-circuits and dc supply voltage is not affected by ac so dc power supplies also behave as short-circuit So all capacitor & dc supply are short circuited to get ac equivalent circuit and it is shown in figure.



AC Equivalent Circuit for CE Amplifier

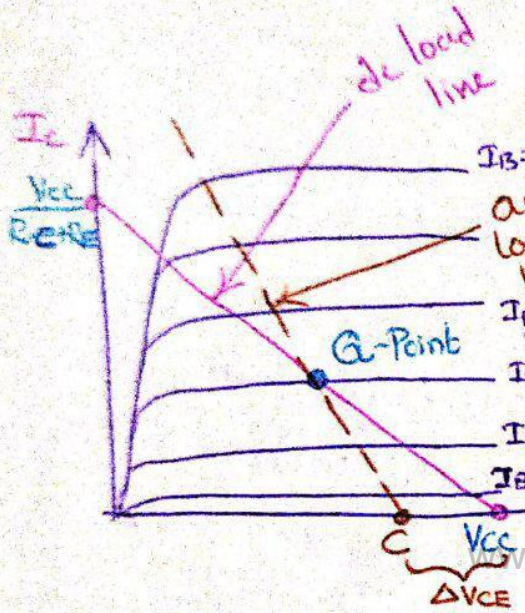
[Power supply and capacitor are Short Circuited]

AC load line :-

The dc load line for the circuit is shown in figure with total Resistance of $(R_C + R_E)$. Because Emitter Resistor is bypassed

by capacitor, resistor R_E is not a part of the circuit in ac load line.

when there is no input ac signal the transistor Q-Point is lies in dc load line. when ac signal is applied causes the transistor Voltage and Currents levels to vary above and below. So another point is found on the ac load line by taking a Collector Current Chage ΔI_C and Collector Emitter Voltage chage ΔV_{CE}.



$$\Delta V_{CE} = \Delta I_C \times R_C.$$

Voltage Swing Limitation :-

The maximum Symmetrical output voltage Swing is ($\pm V_{o(max)}$) that depends on Q Point Present in ac load line.

6. Explain Transistor Models and Parameters for CE, CC, CB Configuration?

It is easy to Analysis a amplifier by replacing BJT to equalant Transistor models. Different models used to get equivalent of Transistor are

* T-equivalent (or) r-parameter equivalent circuit.
* π Equivalent (or) h-parameter equivalent Circuit.

The h-Parameter are much more Convenient for BJT Circuit Analysis.

h_i – Input Impedance
[input voltage / input current]

h_r – reverse Voltage gain.
[input voltage / output voltage]

h_o – output Impedance
[output voltage / output current]

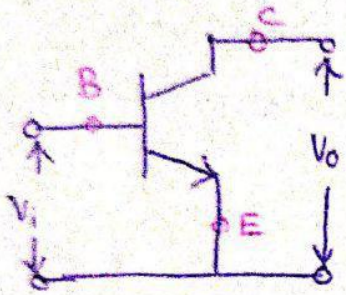
h_f – forward Current gain.
[output Current / input Current]

Using the above four h-parameter BJT device can be Converted to hybrid model.

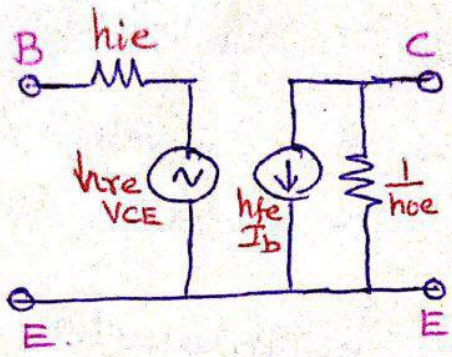
hybrid Parameter and h-parameter equivalent Circuit

Configuration.	h-parameter Equivalent Circuit	h-Parameter

CE Configuration



hybrid model



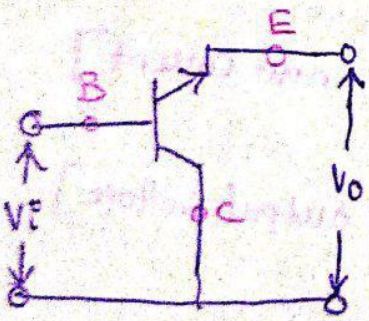
$h_{ie} = \frac{V_{BE}}{I_B}$

$h_{re} = \frac{V_{BE}}{V_{CE}}$

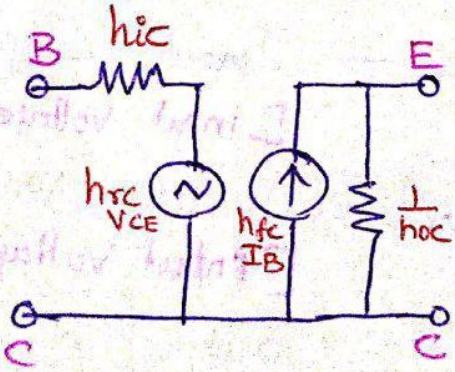
$h_{fe} = \frac{I_c}{I_B}$

$h_{oe} = \frac{I_c}{V_{CE}}$.

CC Configuration



hybrid model



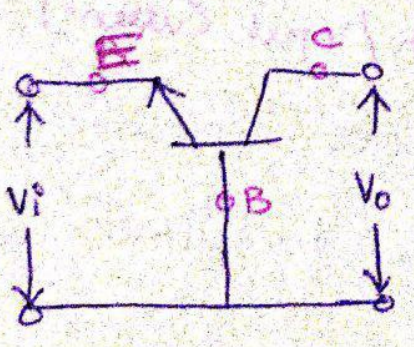
$h_{ic} = \frac{V_i}{I_b}$

$h_{rc} = \frac{V_i}{V_{CE}}$

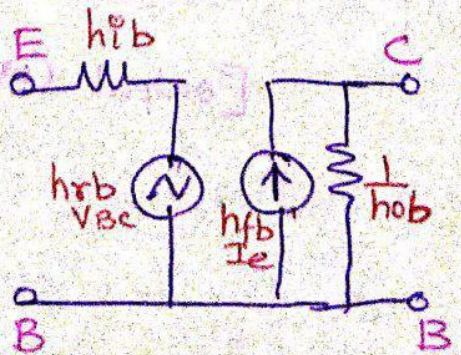
$h_{fc} = \frac{I_e}{I_b}$

$h_{oc} = \frac{I_e}{V_{CE}}$.

CB Configuration



hybrid model



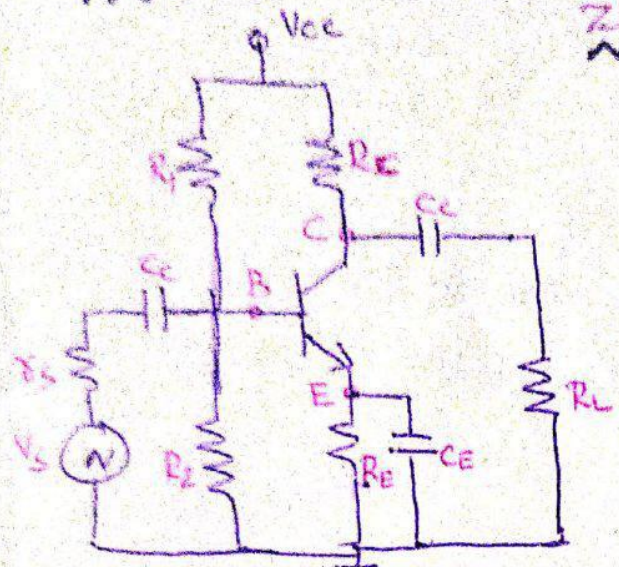
$h_{ib} = \frac{V_{BE}}{i_e}$

$h_{rb} = \frac{V_i}{V_o}$

$h_{fb} = \frac{I_c}{I_e}$

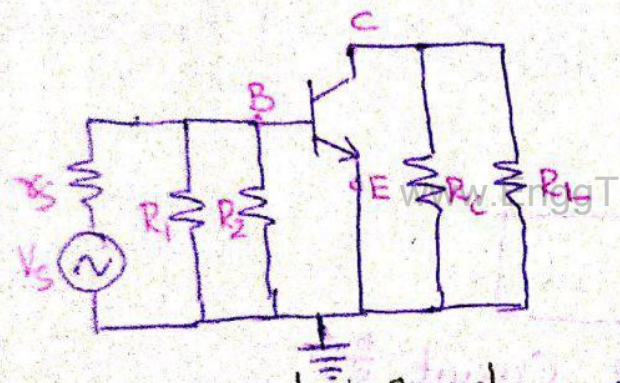
$h_{ob} = \frac{I_c}{V_o}$

7. Explain Ac Analysis of Common Emitter Amplifier with hybrid Parameter model? Find Zi, Zo and Av



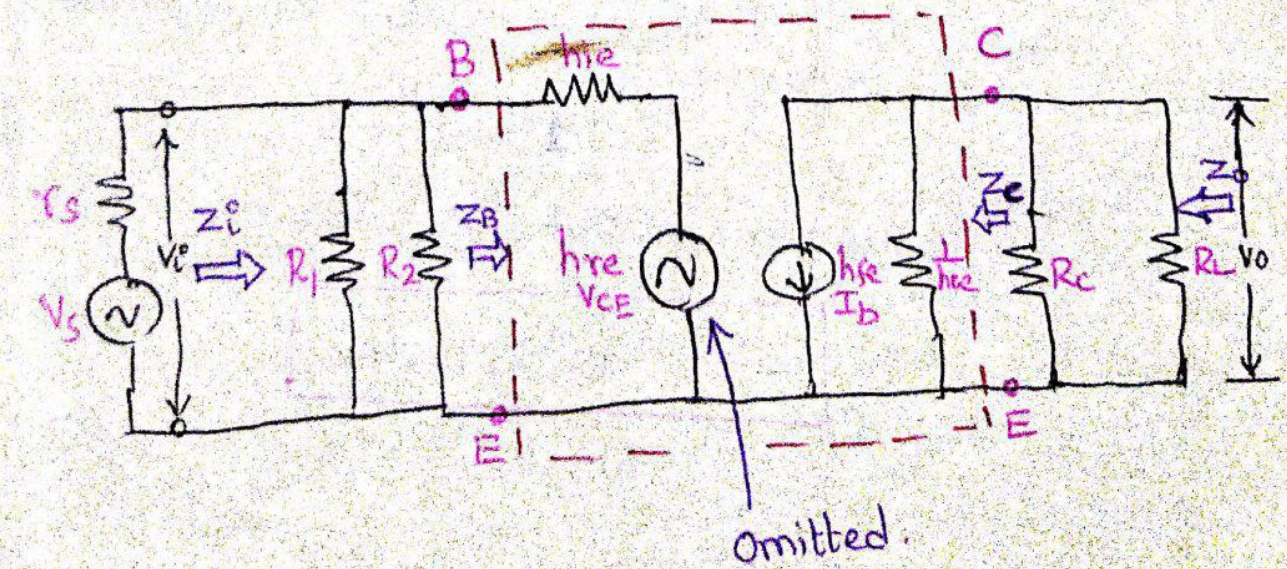
CE Amplifier Circuit

The Common Emitter Amplifier is shown in figure. To get a Ac equivalent Circuit all Capacitor are short Circuited and dc Supply are short Circuited.



Ac equivalent Circuit.

From this Ac equivalent Circuit, h-Parameter equivalent Circuit is drawn by replacing Transistor by Corresponding hybrid Parameter model and it is shown below.



where

$$h_{ie} = \frac{V_{BE}}{I_B}, \quad h_{fe} = \frac{I_c}{I_B}, \quad h_{re} = \frac{V_{BE}}{V_{CE}}$$

$$h_{oe} = \frac{I_c}{V_{CE}}$$

We can omitte $h_{re} V_c$ in CE Circuit Because It is unimportant for most partical Purpose.

Input Impedance ~~of~~ Device :-

The input Impedance at transistor i/p teminal is

$$Z_b \approx h_{ie}$$

Input Impedance of Circuit :-

The input Impedance of CE Circuit is [It is equivalent ~~Cir~~ Impedance at Circuit i/p teminal

$$Z_i = R_1 || R_2 || Z_b$$

We know that $Z_b = h_{ie}$

$$Z_i = R_1 || R_2 || h_{ie}$$

Output Impedance of Device :-

The output Impedance of transistor at output terminal is

$$Z_c = \frac{1}{h_{oe}}$$

Output Impedance of Circuit :-

The output Impedance of Circuit is equivalent Impedance at Circuit output terminal

output Impedance with R_L Connected.

$$Z_o = R_L \,||\, R_c \,||\, \left(\frac{1}{h_{oe}}\right) \leftarrow Z_e$$

output Impedance without R_L

$$Z_o = R_c \,||\, \frac{1}{h_{oe}}$$

Voltage Gain of CE Circuit :- A_v

The Circuit Gain [voltage Gain] is ratio of output voltage V_o to input voltage V_i of Circuit.

$$A_V = \frac{V_o}{V_i}$$

$$V_i = I_b\, h_{ie}$$

$$V_o = -I_c \left(R_c \| R_L \| \frac{1}{h_{oe}}\right)$$

Note
$I_c = h_{fe} I_b$

$$V_o = -h_{fe} I_b \left(R_c \| R_L \| \frac{1}{h_{oe}}\right)$$

$$A_V = \frac{-h_{fe} \cancel{I_b} \left(R_c \| R_L \| \frac{1}{h_{oe}}\right)}{\cancel{I_b}\, h_{ie}}$$

$$\boxed{A_V = \frac{-h_{fe} \left(R_c \| R_L \| \frac{1}{h_{oe}}\right)}{h_{ie}}}$$

if h_{oe} is very very small $\frac{1}{h_{oe}}$ is very very high

$\therefore R_c \| R_L \| \frac{1}{h_{oe}} \approx (R_c \| R_L)$

then

$$\boxed{A_V = \frac{-h_{fe} (R_c \| R_L)}{h_{ie}}}$$

The minus sign in A_V indicates that V_o is 180° out of phase with input V_i

Summary

Device input impedance

$$Z_b = hie$$

Circuit input impedance

$$Z_i = R_1 \| R_2 \| Z_b = R_1 \| R_2 \| hie$$

Device output impedance

$$Z_c = \frac{1}{hoe}$$

Circuit output impedance

$$Z_o = R_L \| R_c \| \frac{1}{hoe} \quad [\text{with } R_L]$$

$$Z_o = R_c \| \frac{1}{hoe} \quad [\text{without } R_L]$$

$$Z_o \approx R_c \quad [\text{if hoe is very very small}]$$

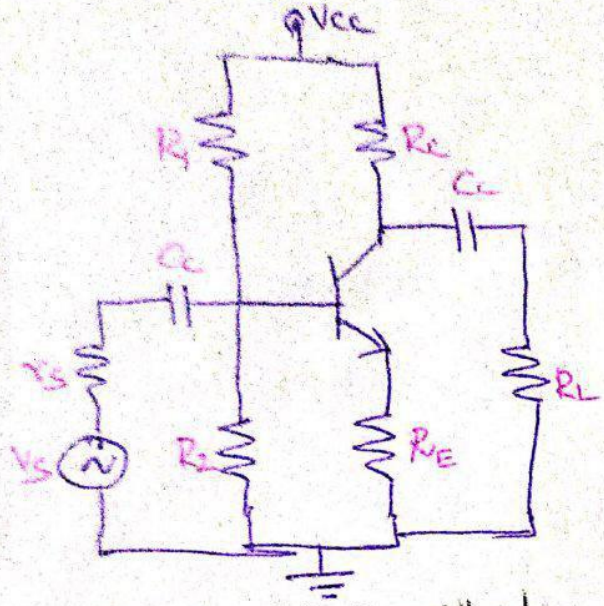
Circuit Voltage gain

$$A_V = \frac{-hfe\,(R_c \| R_L \| \frac{1}{hoe})}{hie}$$

$$A_V = \frac{-hfe\,(R_c \| R_L)}{hie} \quad [\text{if hoe is very very small}]$$

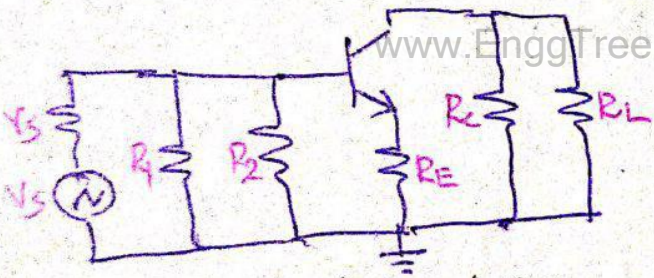
$$A_V = \frac{-(R_c \| R_L)}{hib} \quad [\text{if h-Parameter is Converted to CB h-Parameter}]$$

8. Obtain the Hybrid model of CE Amplifier and Explain AC Analysis of Common Emitter Amplifier without Bypass Capacitor ? [Unbypassed]



CE Amplified without Bypass Capacitor.

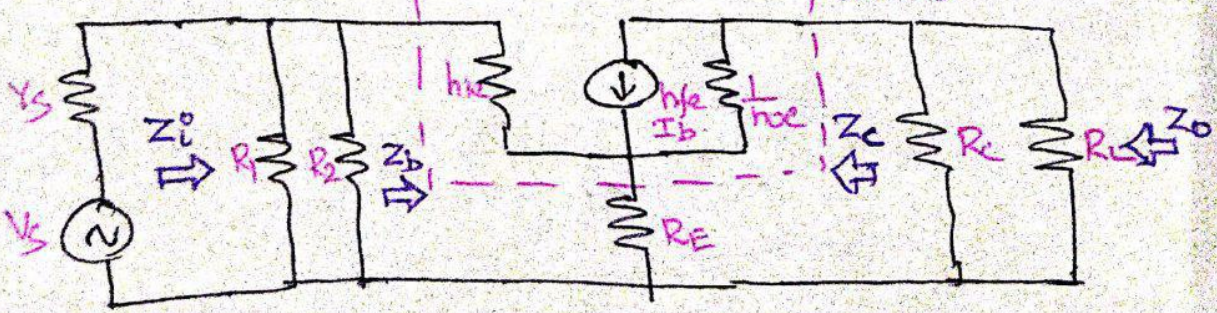
When CE amplifier is unbypassed the Emitter resistor R_E is present in a AC equivalent circuit as shown in figure.



Ac equivalent of CE Unbypased Circuit

As R_E is present in Ac equivalent circuit - in hybrid equivalent circuit also R_E will present as shown in h-model below.

h-model for CE [here VCE is omitted]



Input Impedance of Device :-

The input impedance of transistor at i/p of transistor terminal is

$$Z_b = \frac{V_i}{I_b}$$

$$V_i = I_b h_{ie} + I_e R_E$$

$$= I_b h_{ie} + (I_c + I_b) R_E$$

$$= I_b h_{ie} + (h_{fe} I_b + I_b) R_E$$

$$V_i = I_b [h_{ie} + (1 + h_{fe}) R_E]$$

$$Z_b = \frac{I_b [h_{ie} + (1+h_{fe}) R_E]}{I_b}$$

$$\boxed{Z_b = h_{ie} + (1+h_{fe}) R_E.}$$

Input Impedance of Circuit :-

The input impedance of Circuit at input terminal of Circuit is given by

$$Z_i = R_1 \| R_2 \| Z_b$$

$$\boxed{Z_i = R_1 \| R_2 \| [h_{ie} + (1+h_{fe}) R_E]}$$

Output Impedance of Device :-

The output Impedance of Device is given by

$$Z_c = \frac{1}{h_{oe}} + \left(1 + \frac{1}{h_{fe}}\right) R_E.$$

Output Impedance of Circuit :-

The output Impedance of Circuit at output terminal of Circuit is

$$Z_o = R_L \| R_c \| \frac{1}{h_{oe}}$$

h_{oe} is very small $\frac{1}{h_{oe}}$ is very high

$$Z_o = R_L \| R_c$$

without Load Resistance

$$Z_o \approx R_c$$

Voltage Gain A_V :-

$$A_V = \frac{V_o}{V_i}$$

$$V_i = I_b [h_{ie} + (1+h_{fe}) R_E]$$

$$V_o = -I_c (R_c \| R_L)$$

$$= -h_{fe} I_b (R_c \| R_L)$$

$$A_v = \frac{-h_{fe} I_b (R_c \| R_L)}{I_b [h_{ie} + (1+h_{fe}) R_E]}$$

$$\boxed{A_v = \frac{-h_{fe} (R_c \| R_L)}{h_{ie} + (1+h_{fe}) R_E}}$$

if $(1+h_{fe}) R_E >>> h_{ie}$

$$\boxed{A_v \approx \frac{-h_{fe} (R_c \| R_L)}{R_E}}$$

Note

$$\frac{h_{fe}}{1+h_{fe}} \approx 1$$

Summary :-

Device input impedance

$$Z_b = h_{ie} + (1+h_{fe}) R_E$$

$1+h_{fe} >>> h_{ie}$ & $h_{fe} \approx 1+h_{fe}$

$$Z_b \approx h_{fe} R_E$$

Circuit input impedance :-

$$Z_i = R_1 \| R_2 \| Z_b$$

$$\therefore Z_i = R_1 \| R_2 \| [h_{ie} + R_E(1+h_{fe})]$$

Circuit output impedance :-

$$Z_o = R_L \| R_C \| \frac{1}{h_{oe}}$$

$$Z_o = R_C \| \frac{1}{h_{oe}} \quad [\text{without } R_L]$$

$$Z_o \approx R_C \quad [\frac{1}{h_{oe}} \text{ is very very high}]$$

Circuit voltage gain :-

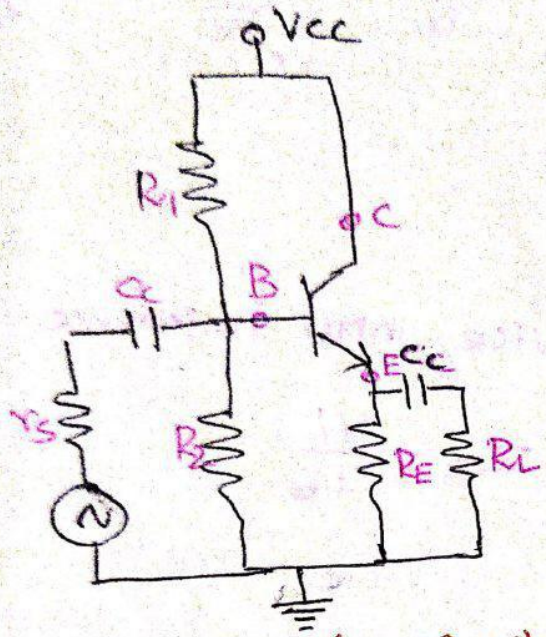
$$A_V = \frac{-h_{fe}(R_C \| R_L)}{h_{ie} + R_E(1+h_{fe})}$$

$1+h_{fe} >>> h_{ie}$ So h_{ie} is omitted & $1+h_{fe} \approx h_{fe}$

$$\therefore A_V \approx -\frac{(R_C \| R_L)}{R_E}$$

Advantage of CE amplifier with an Unbypassed emitter resistor is input impedance is much higher than for a CE circuit that has R_E bypassed.

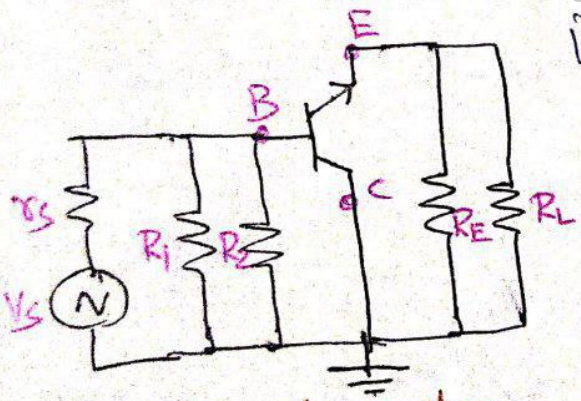
9. Explain the Small signal AC Analysis of Common Collector Amplifier (or) Emitter follower and find Z_i, Z_o and A_v?



CC Amplifier Circuit

The Common Collector Circuit shown in figure. The output is taken in Emitter so it is also called as Emitter. As output is taken across Emitter. So Emitter Resistor is not bypassed.

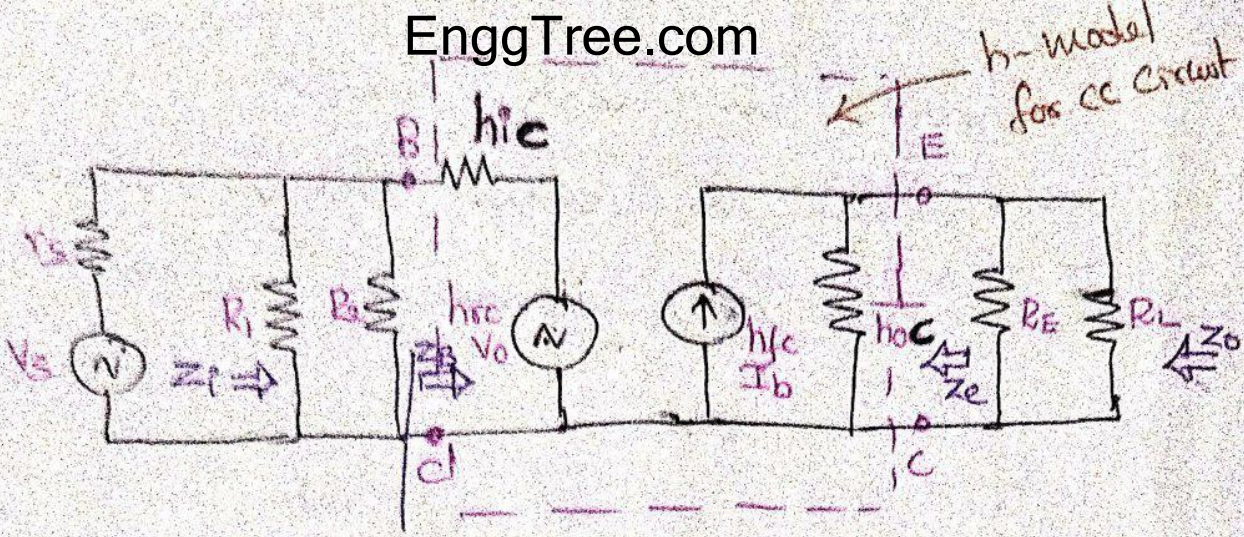
The collector is directly connected to Vcc so no R_C is used.



Ac Equivalent for CC Amplifier

To get ac Equivalent Circuit all capacitor are Short Circuited and dc Supply is also Short Circuited as shown in figure.

h-Parameter equivalent Circuit for CC Amplifier Circuit is shown below.



Where

$$h_{ic} = \frac{V_{BC}}{i_b}$$

$$h_{rc} = \frac{V_{BC}}{V_{CE}}$$

$$h_{fc} = \frac{I_e}{I_b}$$

$$h_{oe} = \frac{I_e}{V_{CE}}$$

Device input impedance

$$Z_B = \frac{V_i}{I_b}$$

$$V_i = I_b h_{ie} + h_{rc} V_o$$

$$= I_b h_{ic} + I_e (R_E \| R_L)$$

$$= I_b h_{ic} + h_{fc} I_b (R_E \| R_L)$$

$$V_i = I_b [h_{ic} + h_{fc} [R_E \| R_L]]$$

$$Z_B = \frac{I_b [h_{ic} + h_{fc} [R_E \| R_L]]}{I_b}$$

$$\boxed{Z_B = h_{ic} + h_{fc} (R_E \| R_L)}$$

Circuit input impedance :-

It is input impedance is impedance at input terminal.

$$Z_i = R_1 \| R_2 \| Z_b$$

$$\boxed{Z_i = R_1 \| R_2 \| [h_{ic} + h_{fc}(R_E \| R_L)]}$$

Device output Impedance :-

$$Z_e = \frac{V_o}{I_e}$$

from Circuit we know that.

$$I_b = \frac{V_o}{h_{ic} + (R_1 \| R_2 \| r_s)}$$

$$\alpha = h_{fc} = \frac{I_e}{I_b}$$

$$I_e = h_{fc} I_b$$

$$I_e = h_{fc} \frac{V_o}{[h_{ic} + (R_1 \| R_2 \| r_s)]}$$

$$Z_e = \frac{\cancel{V_o}}{\frac{h_{fc} \cancel{V_o}}{[h_{ic} + (R_1 \| R_2 \| r_s)]}}$$

$$\boxed{Z_e = \frac{h_{ic} + (R_1 \| R_2 \| r_s)}{h_{fc}}}$$

Output Impedance of Circuit :-

$$Z_o = Z_e \| R_E \| R_L$$

$$Z_o = Z_e \| R_E \quad [\text{If } R_L \text{ is not connected}]$$

Usually R_E is much larger than Z_e

$$\therefore Z_o \approx Z_e$$

$$Z_o \approx \left[\frac{h_{ic} + (R_1 \| R_2 \| r_s)}{h_{fc}}\right]$$

Voltage Grain A_V :-

$$A_V = \frac{V_o}{V_i}$$

$$V_o = I_e (R_E \| R_L)$$

$$V_i = I_b [h_{ic} + h_{fc} (R_E \| R_L)]$$

$$A_V = \frac{I_e (R_E \| R_L)}{I_b [h_{ic} + h_{fc} (R_E \| R_L)]}$$

$$= \frac{h_{fc} I_b (R_E \| R_L)}{I_b [h_{ic} + h_{fc} (R_E \| R_L)]}$$

$$A_V = \frac{h_{fc}(R_E \| R_L)}{h_{ic} + h_{fc}(R_E \| R_L)}$$

this is reduce to

$$A_V = \frac{(R_E \| R_L)}{h_{ib} + (R_E \| R_L)}$$

Summary $\frac{0}{0}$

Device input impedance $\frac{0}{0}$

$$Z_b = h_{ic} + h_{fc}(R_E \| R_L)$$

Circuit input impedance $\frac{0}{0}$

$$Z_i \approx R_1 \| R_2 \| Z_b$$

$$Z_i \approx R_1 \| R_2 \| [h_{ic} + h_{fc}(R_E \| R_L)$$

Device output impedance $\frac{0}{0}$

$$Z_e = \frac{h_{ic} + (R_1 \| R_2 \| r_s)}{h_{fc}}$$

Circuit output impedance $\frac{0}{0}$

$$Z_o = Z_e \| R_E \| R_L$$

$$Z_o = Z_e \| R_E \quad [\text{without } R_L]$$

$$Z_o \approx Z_e \quad [\text{If } R_E \text{ is very large}]$$

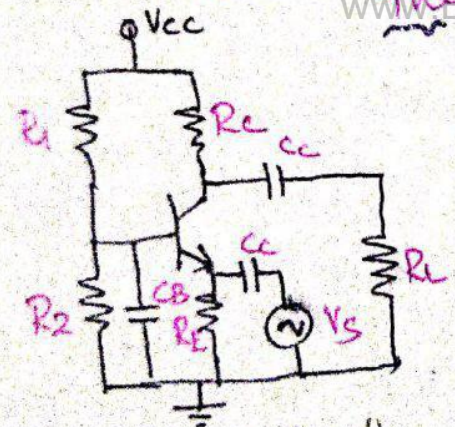
Circuit Voltage gain :-

$$A_V = \frac{h_{fc}(R_E \| R_L)}{h_{ic} + h_{fc}(R_E \| R_L)}$$

$$A_V = \frac{(R_E \| R_L)}{h_{ib} + (R_E \| R_L)} \approx 1$$

---

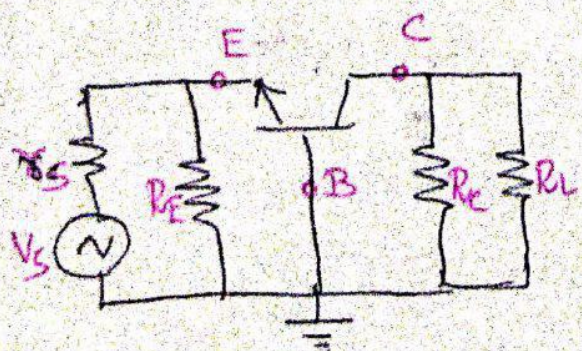
10. Do AC Analysis of the Common Base Amplifier with help of hybrid Parameter?



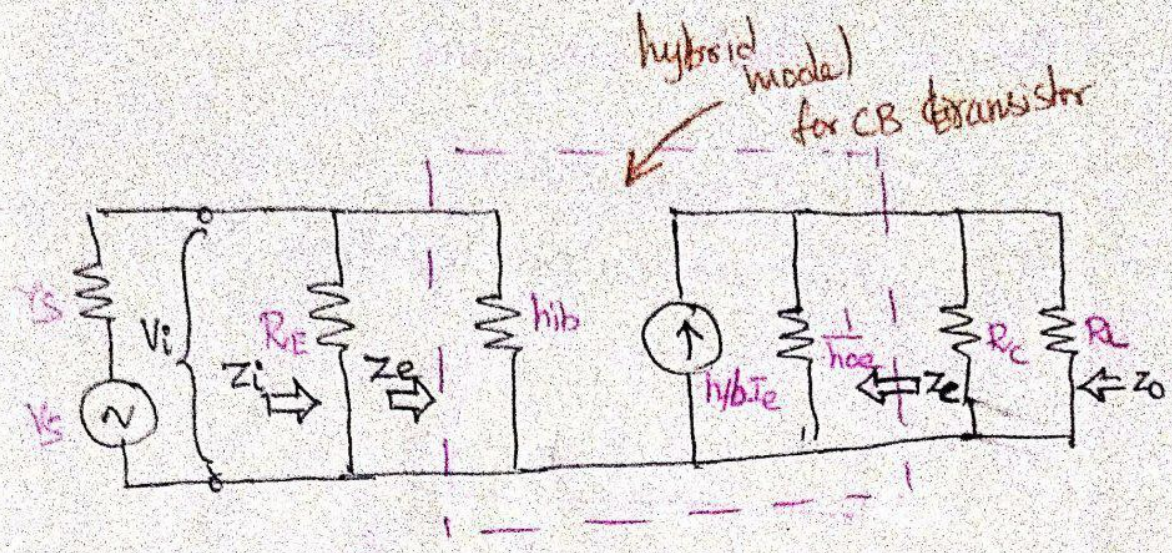
CB Amplifier Circuit.

The Common Base (CB) Circuit is shown in figure. is very Similar to a CE Circuit, except that the input Signal is applied to the transistor emitter instead of base and the Base terminal is Bypassed by C_B capacitor.

The ac equivalent Circuit also shown in figure.



AC equivalent of CB Amplifier Circuit.



Here $h_{rb} V_{BC}$ is omitted.

Where

$$h_{ib} = \frac{V_{BE}}{i_e}, \quad h_{rb} = \frac{V_{BE}}{V_{BC}}, \quad h_{fb} = \frac{I_c}{I_e}$$

and $$h_{oe} = \frac{I_e}{V_{BC}}$$

Device Input Impedance $\frac{0}{0}$

The input impedance of CB transistor is simply h_{ib}

$$\boxed{Z_e = h_{ib}}$$

Circuit Input Impedance $\frac{0}{0}$

$$\boxed{Z_i = Z_e \,||\, R_E}$$

$$\boxed{Z_i = Z_e}$$ (usually R_E is very very high).

Device output Impedance :-

The Device output Impedance is Impedance at output terminal of CB transistor

$$Z_c = \frac{1}{h_{ob}}$$

Circuit output Impedance :-

The Circuit output Impedance is given as

$$Z_o = Z_c \| R_c \| R_L$$

note.
if R_L not Connected.

$$Z_o = Z_c \| R_c$$

Usually Z_c is very very big

$$Z_o = R_c$$

Circuit Voltage Gain Av :-

The Voltage Gain is given by

$$A_V = \frac{V_o}{V_{in}}$$

$$V_o = I_c (R_c \| R_L)$$

$$V_o = h_{fb} I_e (R_c \| R_L)$$

$$V_{in} = I_e h_{ib}$$

$$A_v = \frac{h_{fb} I_e (R_c \| R_L)}{I_e h_{ib}}$$

$$\boxed{A_v = \frac{h_{fb} (R_c \| R_L)}{h_{ib}}}$$

Summary :-

Device input impedance :-

$$Z_e = h_{ib}$$

Circuit input impedance :-

$$Z_i = Z_e \| R_E$$

$$= h_{ib} \| R_E.$$

Device output impedance :-

$$Z_c = \frac{1}{h_{oe}}$$

Circuit output impedance :-

$$Z_o = Z_c \| R_c \| R_L$$

$$Z_o = Z_c \| R_c \quad [\text{without } R_L]$$

$Z_o = R_c$ [Z_c is very very large]

Circuit voltage gain :-

$$A_V = \frac{h_{fb}(R_c \| R_L)}{h_{ib}}$$

---

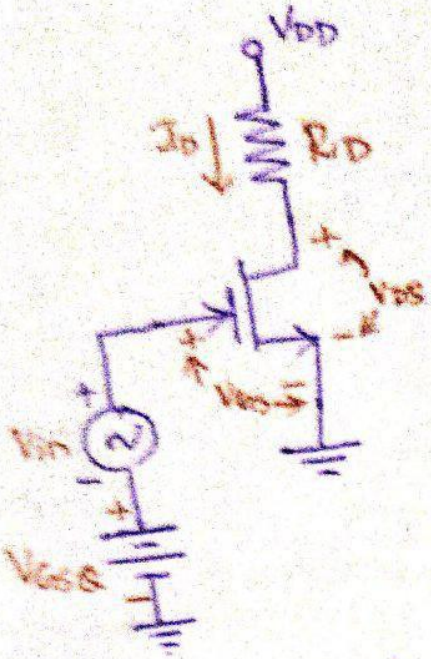
11. Give Conversion from CE h-Parameter to CB and CC h-Parameters. ?

CE to CB h-Parameter	CE to CC h-Parameter
$h_{ib} \approx \frac{h_{ie}}{1+h_{fe}}$	$h_{ic} = h_{ie}$
$h_{rb} \approx \frac{h_{ie}h_{oe}}{1+h_{fe}} - h_{re}$	$h_{rc} = 1 - h_{re}$
$h_{fb} \approx \frac{h_{fe}}{1+h_{fe}}$	$h_{fc} = 1 + h_{fe}$
$h_{ob} \approx \frac{h_{oe}}{1+h_{fe}}$	$h_{oc} = h_{oe}$

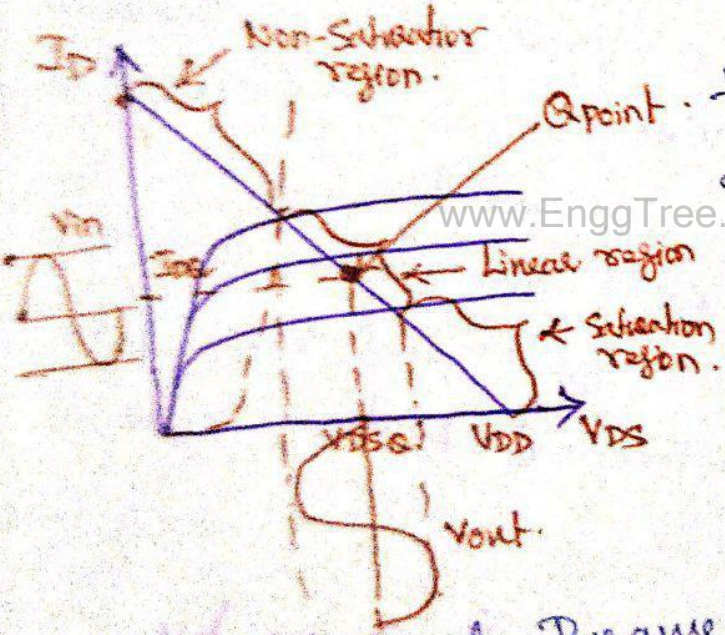
---

12. Explain the MOSFET CS, CD and obtain the hybrid model. Find Zi, Zo and Av

MOSFET Amplifiers :-



The figure shows n-channel enhancement mode MOSFET Common Source Circuit with a time-varying (a.c) voltage Source in series with the dc Source.



The figure shows the MOSFET characteristics dc load line, and Q-Point where the dc load line and Q-Point are function of VGS, VDD, RD and the MOSFET Parameters

Small Signal Parameters :-

The instantaneous gate to Source Voltage is given by

$$V_{GS} = V_{GSQ} + V_{in} = V_{GSQ} + V_{gs}$$

The instantaneous drain Current is

$$i_D = \beta_n (V_{GS} - V_T)^2$$

Sub V_{GS} in i_D

$$i_D = \beta_n [V_{GSQ} + v_{gs} - V_T]^2$$

$$= \beta_n [(V_{GSQ} - V_T) + v_{gs}]^2$$

$$i_D = \underbrace{\beta_n (V_{GSQ} - V_T)^2}_{\text{DC component}} + \underbrace{2\beta_n (V_{GSQ} - V_T) v_{gs}}_{\text{Time varying } I_D \text{ component}} + \underbrace{\beta_n v_{gs}^2}_{\text{harmonics.}}$$

The first term in equation represents the d.c (or) quiescent drain current I_{DQ}, the second term represents the time varying drain current component that is linearly related to the signal v_{gs}, and the third term is proportional to the square of the signal voltage.

The transconductance is given by

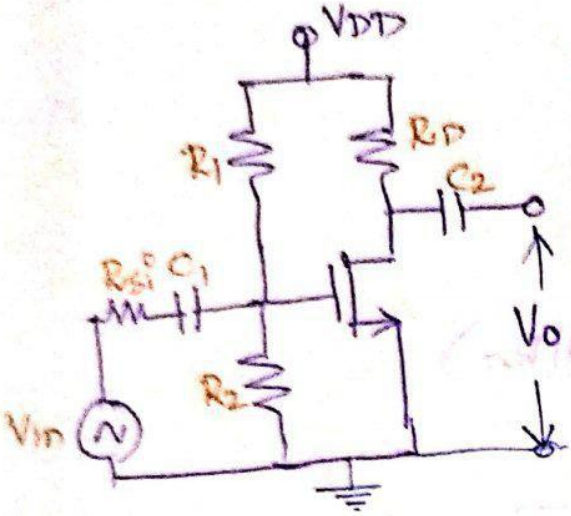
$$g_m = \frac{\partial i_D}{\partial v_{gs}} = 2\beta_n (V_{GSQ} - V_T)$$

$$g_m = 2\sqrt{\beta_n I_{DQ}}.$$

where

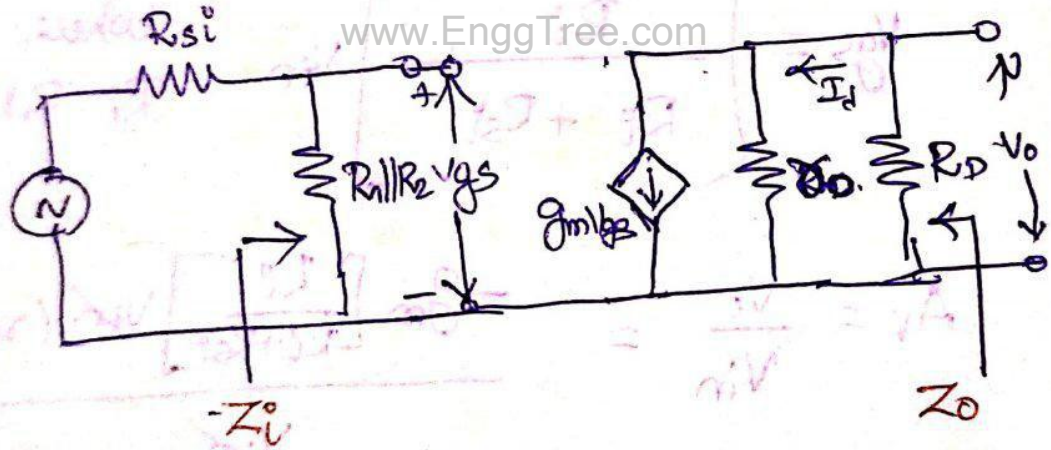
$$\beta_n = \frac{1}{2} \mu_n C_{ox} \left[\frac{W}{L}\right]$$

(i) Common Source Amplifier
[Voltage Divider Bias]



In Common Source Amplifier input is applied in gate and output is taken at Drain terminal. Here Source is Common. as shown in the figure

Low frequency equivalent circuit, CS amplifier with voltage divider bias is shown in figure



Input Impedance

$$Z_i = R_1 \| R_2$$

output Impedance

$$Z_o = R_D \| r_o$$

Voltage gain A_V =?

$$V_o = -I_d (r_o \| R_D)$$

$$I_d = g_m V_{gs}$$

$$V_o = -g_m V_{gs} (r_o \| R_D)$$

$$V_{gs} = \left[\frac{(R_1 \| R_2)}{(R_1 \| R_2) + R_{si}}\right] V_{in}.$$

$$V_{gs} = \left[\frac{R_i}{R_i + R_{si}}\right] V_{in} \quad \text{where } R_i = R_1 \| R_2$$

$$A_V = \frac{V_o}{V_{in}} = \frac{-g_m \left[\frac{R_i}{R_i + R_{si}}\right] V_{gs} (r_o \| R_D)}{V_{in}}$$

$$\boxed{A_V = -g_m \left[\frac{R_i}{R_i + R_{si}}\right] (r_o \| R_D)}$$

Summary :-

Input Impedance :-

$$Z_i = R_1 \| R_2$$

output Impedance :-

$$Z_o = r_o \| R_D$$

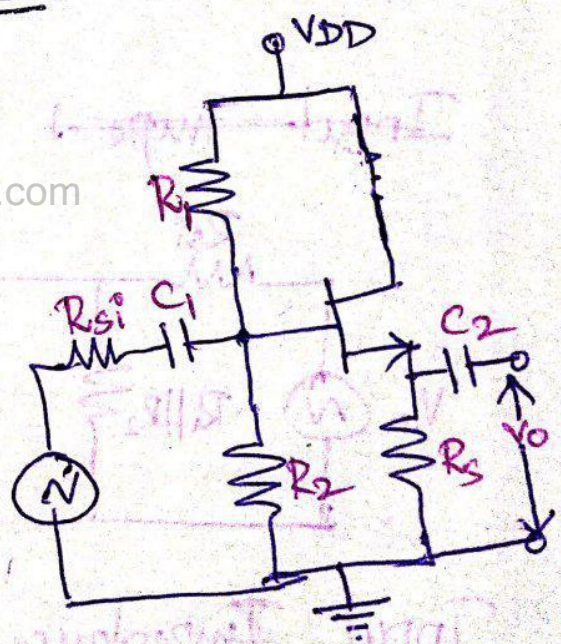
Voltage Gain :-

$$A_V = -g_m \left(\frac{R_i}{R_i + R_{si}} \right) (r_o \| R_D)$$

MOSFET Source Follower Amplifier, [Common Drain Amplifier]

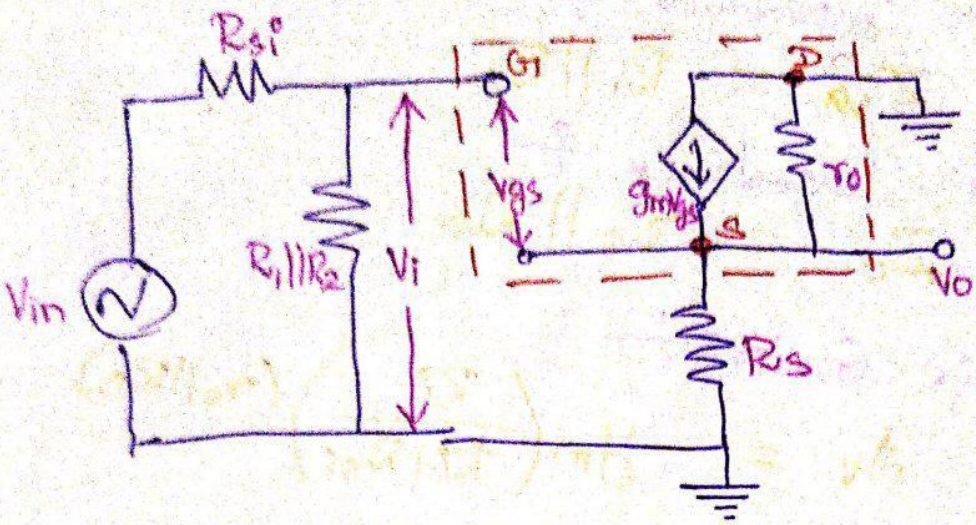
(i)

NMOS Source follower (common drain) amplifier is shown in figure. Here, the output is taken from the Source with respect to ground and drain is connected directly to V_{DD}



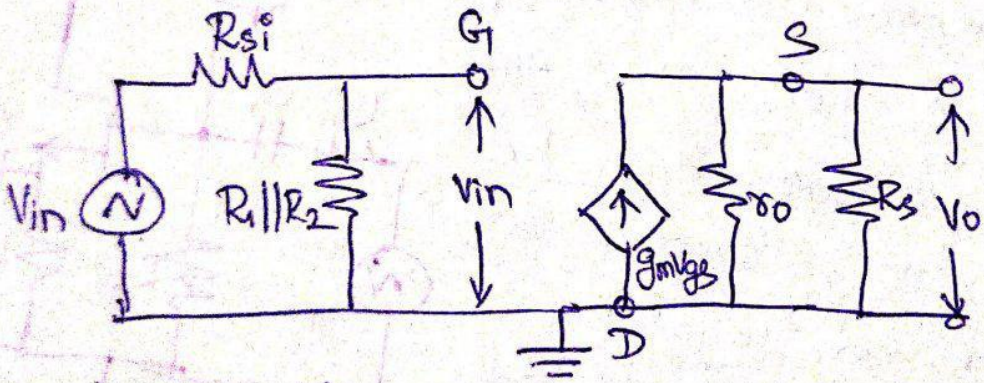
The Small Signal equivalent circuit. The circuit is drawn assuming the Coupling Capacitor acts as a short circuit.

It is shown in figure below.



The same equivalent Circuit, with all signal grounds at a Common Point.

~~Input impedance~~

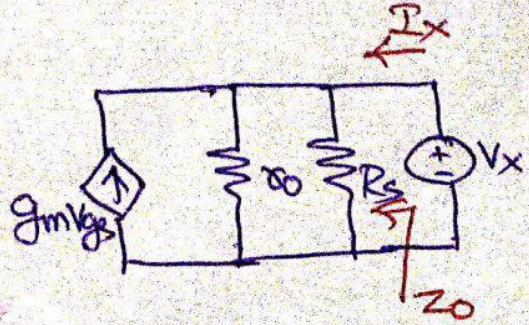


Input Impedance $\frac{0}{0}$

$$Z_i = R_1 || R_2$$

output Impedance $\frac{0}{0}$

$$I_x + g_m V_{gs} = \frac{V_x}{r_o} + \frac{V_x}{R_s}$$



Since input Current is Zero, we have

$$V_{gs} = -V_x$$

$$I_x - g_m V_x = \frac{V_x}{r_o} + \frac{V_x}{R_s}$$

$$I_x = V_x \left[g_m + \frac{1}{r_o} + \frac{1}{R_s} \right]$$

$$\frac{I_x}{V_x} = \frac{1}{Z_o} = g_m + \frac{1}{r_o} + \frac{1}{R_s}$$

$$Z_o = \frac{1}{g_m + \frac{1}{r_o} + \frac{1}{R_s}}$$

$$\boxed{Z_o = \frac{1}{g_m} \,||\, r_o \,||\, R_s}$$

Voltage gain $\frac{0}{0}$

$$V_o = I_d (r_o || R_s) = g_m V_{gs} (r_o || R_s)$$

$$V_{in} = V_{gs} + V_o$$

$$V_{in} = V_{gs} + g_m V_{gs} (r_o || R_s)$$

$$V_{gs} = \frac{V_{in}}{1 + g_m (r_o || R_s)}$$

$$V_{in} = \frac{R_i'}{R_i' + R_{si}'} V_i' \qquad \text{where } R_i' = R_1 || R_2$$

$$V_{gs} = \frac{1}{1 + g_m(r_o || R_s)} \cdot \frac{R_i'}{R_i' + R_{si}'} V_i'$$

$$V_o = \frac{g_m (r_o || R_s)}{1 + g_m (r_o || R_s)} \frac{R_i'}{R_i' + R_{si}'} V_i'$$

$$\boxed{A_V = \frac{V_o}{V_i'} = \frac{g_m(r_o || R_s)}{1 + g_m(r_o || R_s)} \cdot \frac{R_i'}{R_i' + R_{si}'}}$$

$$A_V = \frac{g_m(r_o || R_s)}{1 + g_m(r_o || R_s)} \cdot \frac{R_i'}{R_i' + R_{si}'}$$

Summary :-

Input Impedance :-

$$Z_i' = R_1 || R_2$$

Output Impedance :-

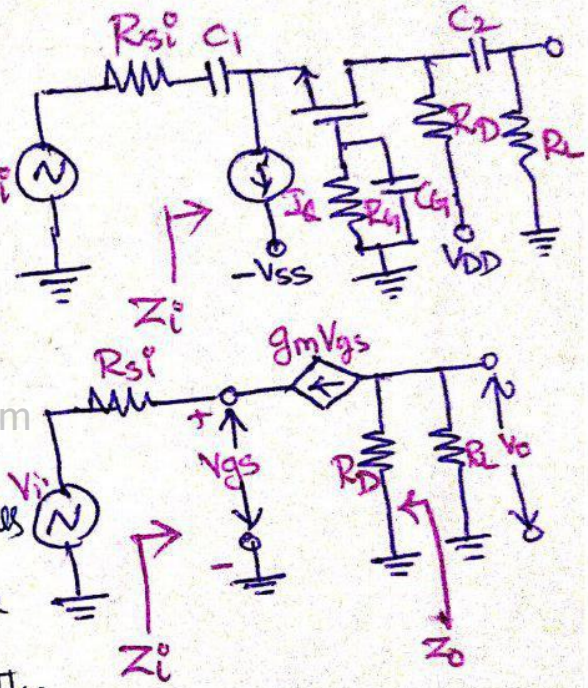
$$Z_o = \frac{1}{g_m} || r_o || R_s$$

Voltage Gain A_v :-

$$A_v = \frac{g_m(r_o \| R_s)}{1 + g_m(r_o \| R_s)} \cdot \frac{R_i}{R_i + R_{si}}$$

MOSFET Common Gate Amplifier :-

The NMOS common gate amplifier circuit is shown in figure. Here, the constant current source I_a is used to bais the MOSFET. Resistor R_G at the gate Prevents the build up of Static Charge on the gate teminal and the bypass Capacitor C_G ensures that the gate is at Signal ground. The Coupling Capacitor C_1 couples the Signal to the Source teminal and coupling Capacitor C_2 couples the output Voltage to the load resistor R_L



Input Impedance :-

$$Z_i = \frac{V_i}{I_i} = \frac{-V_{gs}}{I_i}$$

$$I_i = -g_m V_{gs}$$

$$Z_i = \frac{+V_{gs}}{+g_m V_{gs}} = \frac{1}{g_m}$$

$$Z_i = \frac{1}{g_m}$$

Output Impedance $\frac{0}{0}$

$$Z_o = R_D$$

Voltage gain A_V $\frac{0}{0}$

$$V_o = -g_m V_{gs} (R_D \| R_L)$$

$$V_i = I_i R_{si} - V_{gs}$$

$$V_i = (-g_m V_{gs}) R_{si} - V_{gs}$$

$$V_{gs} = \frac{-V_i}{1 + g_m R_{si}}$$

$$V_o = (-g_m) \frac{-V_i}{1 + g_m R_{si}} (R_D \| R_L)$$

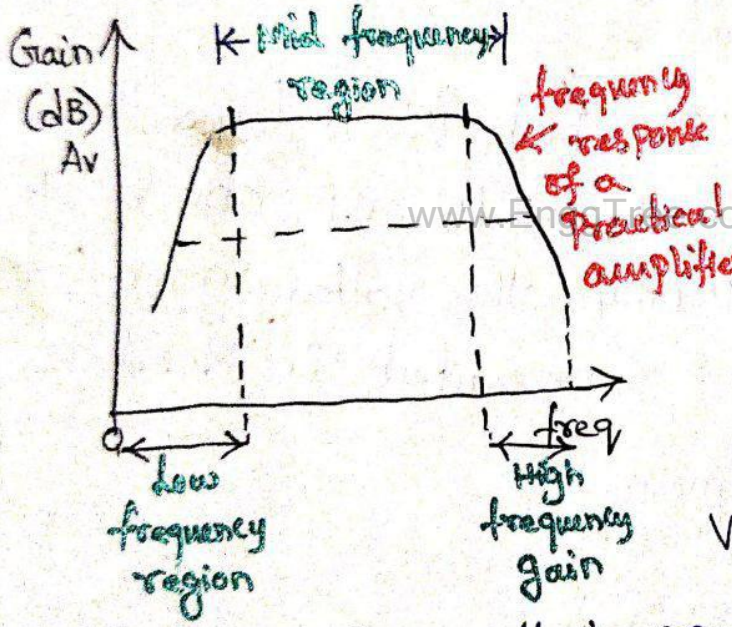
$$A_V = \frac{V_o}{V_i} = \frac{g_m}{1 + g_m R_{si}} (R_D \| R_L)$$

$$A_V = \frac{g_m}{1 + g_m R_{si}} (R_D \| R_L)$$

13. Explain the frequency response of Amplifier?

Ans:- General shape of frequency Response of Amplifiers :-

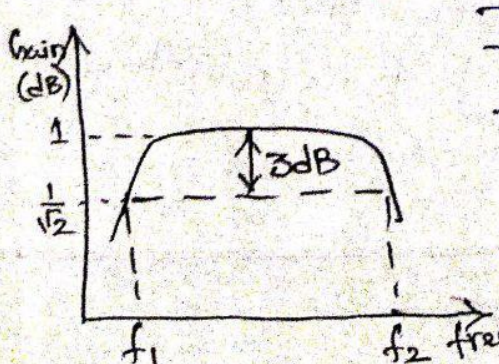
An amplifier should ideally provide the same amplification for all frequencies. But Practically frequency response of the amplifier is shown below.



The curve is a plot of the voltage gain of an amplifier verses frequency of input signal.

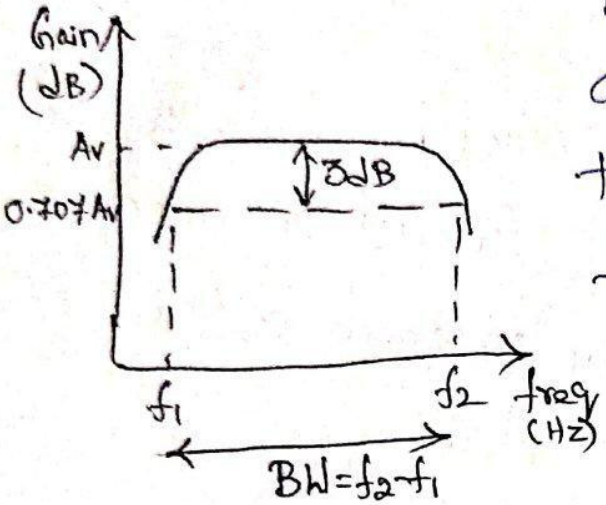
The decrease in voltage gain with frequency is called roll-off.

Cut off frequencies :-



It is frequency at which the gain fall to half its maximum power (or) fall to $\frac{1}{\sqrt{2}}$ times (0.707) of its maximum values as it shown in figure f1 & f2.

Bandwidth :-



Bandwidth of the amplifier is defined as the difference between f_2 and f_1.

$$BW = f_2 - f_1$$

The Decibel unit :-

The Decibel is a logarithmic measurement of the ratio of one voltage to another. Usually, the voltage gain of the amplifier is represented in decibels (dB). It is given by

$$\text{Voltage gain in dB} = 20 \log \left[\frac{V_{out}}{V_{in}}\right]$$

Note :- $20 \log \frac{1}{\sqrt{2}} = -3\,dB$ thats why. $-3\,dB$ is taken to find Bandwidth.

Then A_{is}, at low frequency $= \frac{I_L}{I_s} = \frac{-g_m r_\pi R_s}{R_s + r_b + r_\pi}$

$$A_{is(low)} = \frac{-h_{fe} R_s}{R_s + r_b + r_\pi} \quad \because h_{fe} = g_m r_\pi$$

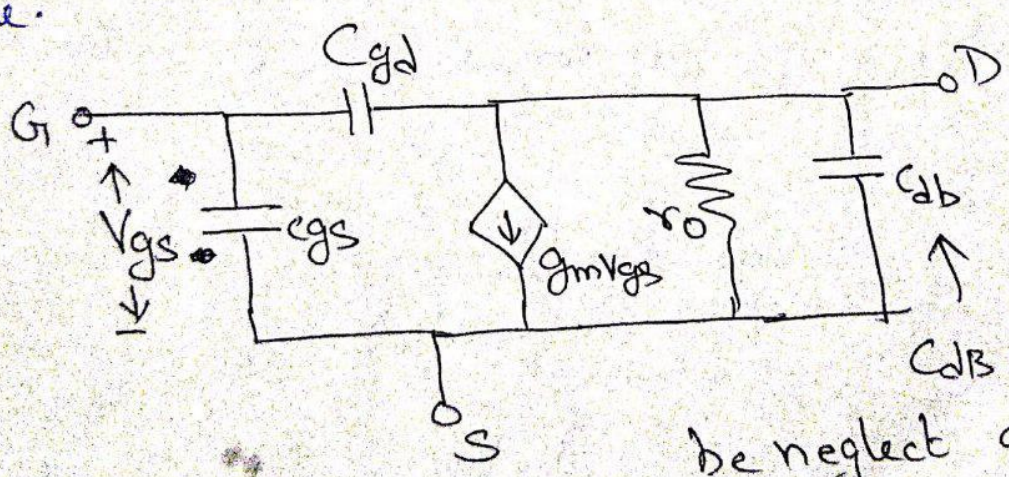
$$A_{is(low)} = \frac{-h_{fe} R_s}{R_s + h_{ie}} \quad \because h_{ie} = r_b + r_\pi.$$

14. Explain with a neat diagram high frequency analysis of MOSFET?

MOSFET Analysis

High frequency MOSFET Model

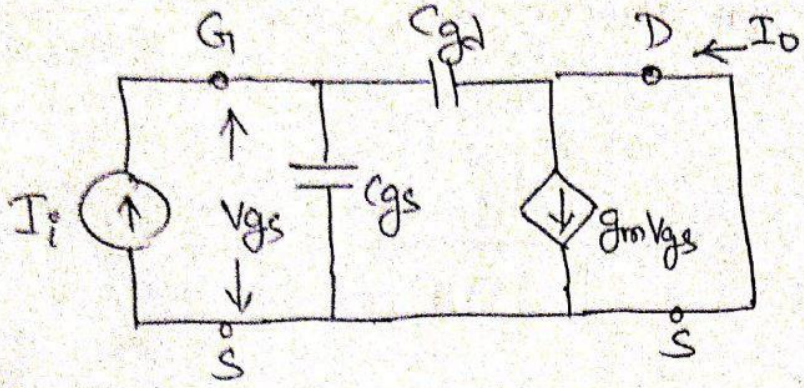
The high frequency equivalent circuit model for MOSFET is shown in figure.



C_{DB} can be neglect as it is very small.

Unit-Gain frequency (f_T) :-

The f_T is the frequency at which the short-circuit current gain of the CS MOSFET amplifier became unity.



The Short Circuit Current I_o is given by

$$I_o = g_m V_{gs} - S C_{gd} V_{gs}.$$

$S C_{gd} V_{gs}$ is very small and can be neglected.

$$I_o \simeq g_m V_{gs}$$

The V_{gs} in terms of I_i can be given by

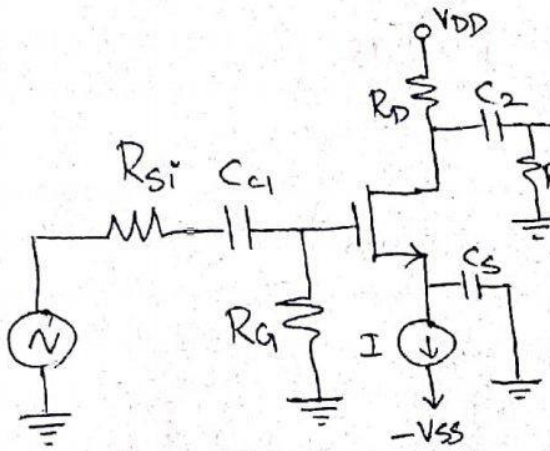
$$V_{gs} = \frac{I_i}{S(C_{gs}+C_{gd})}$$

$$\frac{I_o}{I_i} = \frac{g_m V_{gs}}{V_{gs}\, S(C_{gs}+C_{gd})} = \frac{g_m}{S(C_{gs}+C_{gd})}$$

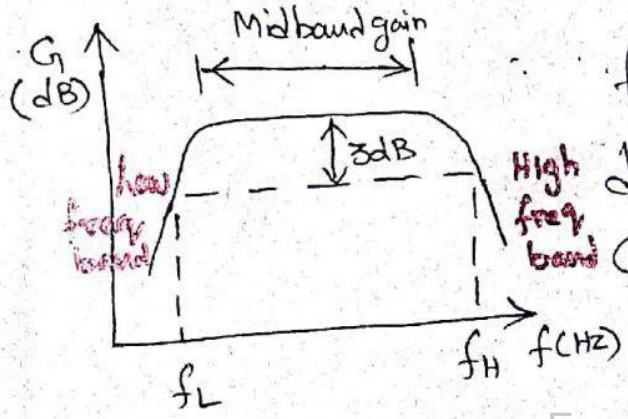
$$\omega_T = \frac{g_m}{C_{gs}+C_{gd}}$$

$$f_T = \frac{g_m}{2\pi (C_{gs}+C_{gd})}$$

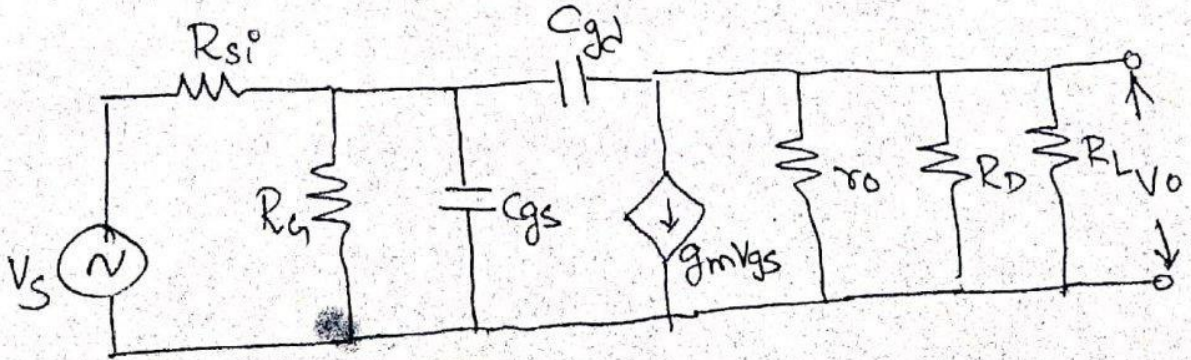
Frequency Response of CS Amplifier :-



CS MOSFET amplifier show in figure. Its gain falls at low frequency due to the effect of C_{c1}, C_s and C_{c2}. Its gain falls at high frequency due to the effect of C_{gs} and C_{gd}.

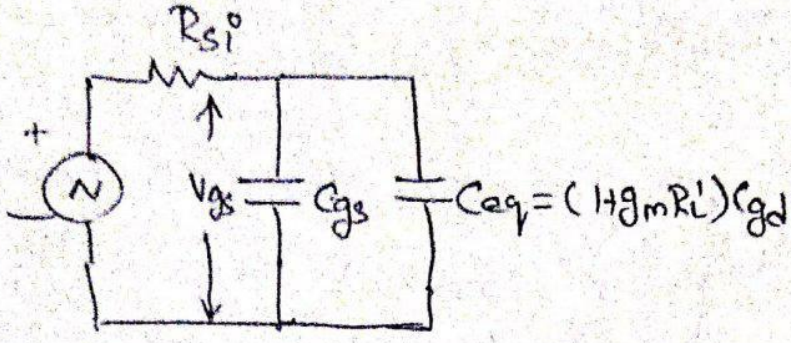


The high frequency equivalent Circuit for CS MOSFET amplifier.



$$V_o = -I_L R_L' = -g_m V_{gs} R_L'$$

where $R_L' = r_o \| R_D \| R_L$



By Millers theorem, equivalent Capacitance is given by

$$C_{eq} = (1+A_V)\,C = (1+A_V)\,C_{gd}$$

$$A_V = \frac{V_o}{V_{in}} = \frac{-g_m V_{gs} R_L'}{V_{gs}} = -g_m R_L'$$

$$C_{eq} = (1+g_m R_L')\,C_{gd}$$

Total input Capacitance C_{in} can be given by

$$C_{in} = C_{gs} + C_{eq} = C_{gs} + (1+g_m R_L')\,C_{gd}.$$

The total resistance is given by

$$R_{si}' = R_{si} \| R_G$$

Time Constant is

$$\tau = RC = R_{si}' C_{in}.$$

$$\omega_0 = \frac{1}{\tau} = \frac{1}{R_{si}' C_{in}} \qquad f_H = \frac{1}{2\pi R_{si}' C_{in}}$$

EC 3353 - Electronic Devices and Circuits.

Unit - III Multistage Amplifiers and Differential Amplifiers

Cascode amplifier, Differential amplifier - Common mode and Difference mode analysis MOSFET input stages - tuned amplifiers - Gain and frequency response - Neutralization methods.

Unit III: Multistage Amplifiers and Differential Amplifier

1. Define multistage amplifier.

Multistage amplifier is defined as an amplifier in which more than one amplifying stage is used to achieve greater voltage and power gain.

2. Mention the types of multistage amplifiers.

i. Cascade Amplifier

ii. Cascode Amplifier

3. What do you mean by Cascade amplifier?

The output of one stage is fed as the input of the next stage. Two or more CE amplifier are connected together to form cascade amplifier.

4. What is Cascode amplifier?

It is the combination of CE and CB amplifiers. The output of CE amplifier is connected as the input of CB amplifier.

5. Define voltage gain of a multistage amplifier.

The voltage gain is defined as the product of the gain of the individual stages of the multistage amplifier.

$A_V = A_{V1} A_{V2} \ldots A_{Vn}$

6. What are the basic requirements of multistage amplifier?

i. Impedance matching

ii. High gain

iii. Large bandwidth

7. What is BIMOS amplifier?

The common Base (CB) BJT (Bipolar) amplifier stage is connected in cascade with a common Gate (CG) MOSFET amplifier to form a BIMOS amplifier.

8. Define differential amplifier.

The differential amplifier is defined as the amplifier which amplifies the difference between two input signals.

$V_O = V_1 - V_2$

9. What do you mean by common mode signal?

The signal which is common to both input terminals is called common mode signal.

10. What do you mean by differential mode signal?

When the two applied signals are different, the output is the difference between two input signals. The output difference signal is called differential mode signal.

11. Define differential gain.

Differential gain is defined as the gain with which the differential amplifier amplifies the differential signal.

12. Define common mode gain.

Common mode gain is defined as the gain with which a practical differential amplifier amplifies the common mode signal.

13. Define CMRR.

Common Mode Rejection Ratio (CMRR) is defined as the ability of a differential amplifier to reject the common mode signal. It is the figure of merit of a differential amplifier.

$$\text{CMRR}\,(d\text{B}) = 20 \log_{10} \left| \frac{A_d}{A_c} \right|$$

14. Write the features of differential amplifier.

i. High differential gain

ii. Low common mode gain

iii. High CMRR

iv. High input impedance and low output impedance

v. High gain

vi. Large Bandwidth

15. How can CMRR be improved?

i. Increase differential gain Ad

ii. Decrease common mode gain Ac

16. Write the features of FET differential amplifier.

i. Very high input impedance

ii. Low differential gain

iii. Low input bias and offset current

iv. More noise

17. Define tuned amplifier?

An amplifier which amplifies specific frequency is called tuned amplifier.

18. Define selectivity.

Selectivity is defined as the ratio of the bandwidth of the circuit to its resonant frequency.

Selectivity = Bandwidth/Resonant frequency

19. What is meant by double tuned amplifier?

If the amplifier has two inductively coupled tuned circuits which are tuned to same frequency, then the amplifier is called double tuned amplifier.

20. What is meant by Stagger tuning?

In this amplifier, number of single tuned amplifiers are connected in cascade and tuned to slightly different frequencies.

21. Why do we need neutralization?

To prevent oscillations in tuned amplifiers, the neutralization technique is used.

22. What are the types of neutralization.

i. Hazeltine neutralization

ii. Neutrodyne neutralization

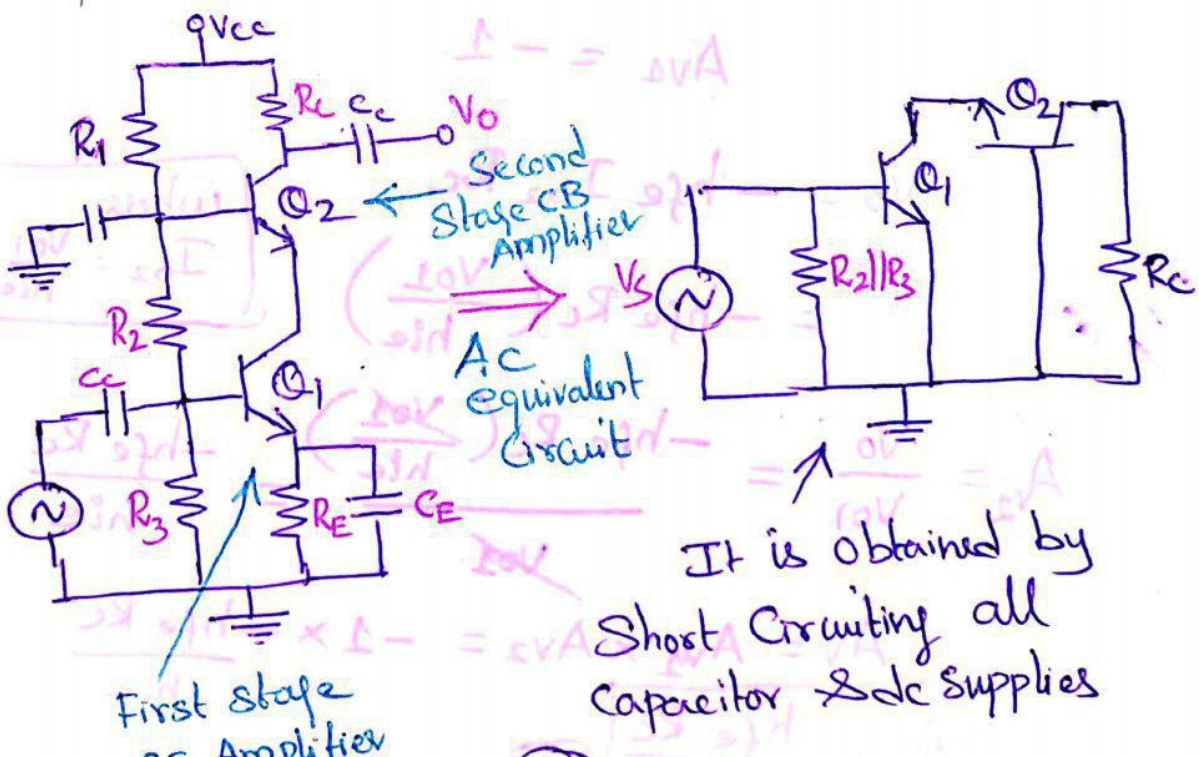
iii. Neutralization using coil

Cascode Amplifier :-

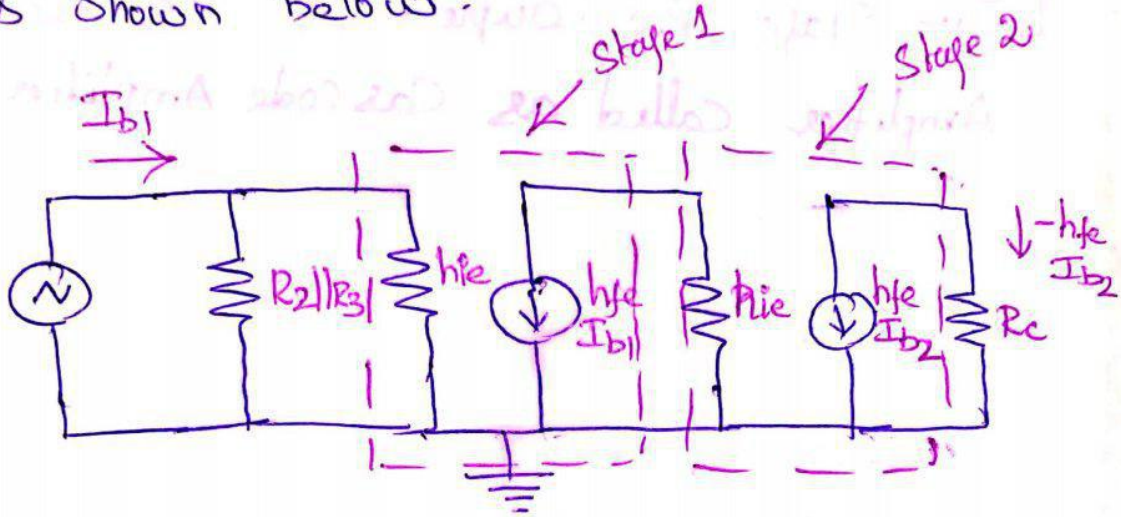
[Two Stage Rc Coupled CE – CB Cascade Amplifier called as Cascode Amplifier]

In Cascade Amplifier gain increases bayt Bandwidth reduced So overcome this limitation Cascode amplifier is used.

It Consist of a CE Stage (1st stage) followed by a CB Stage (2nd stage) directly coupled to each other and Combines some of the features of the both amplifiers. it is shown in figure.



Approximate h-parameter model for Cascode is shown below.



$$V_i = I_{b1} h_{ie}$$

$$V_{o1} = -I_{b2} h_{ie}$$

$$A_{v1} = \frac{V_{o1}}{V_i} = \frac{-I_{b2} h_{ie}}{I_{b1} h_{ie}} = \frac{-I_{b2}}{I_{b1}}$$

if $I_{b1} = I_{b2}$

$$A_{v1} = -1.$$

$$V_o = -h_{fe} I_{b2} R_c$$

$$= -h_{fe} R_c \left(\frac{V_{o1}}{h_{ie}}\right)$$

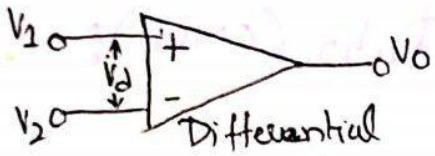
where $I_{b2} = \frac{V_{o1}}{h_{ie}}$

$$A_{v2} = \frac{V_o}{V_{o1}} = \frac{-h_{fe} R_c \left(\frac{V_{o1}}{h_{ie}}\right)}{V_{o1}} = \frac{-h_{fe} R_c}{h_{ie}}$$

$$A_v = A_{v1} \times A_{v2} = -1 \times \frac{-h_{fe} R_c}{h_{ie}}$$

$$\boxed{A_v = \frac{h_{fe} R_c}{h_{ie}}} \quad (50)$$

Differential Amplifier :-



V_1 & V_2 are two different inputs.

The function of differential amplifier is to amplify the difference between two Signal It is shown in figure.

Two Mode of operation.

* Differential Mode
* Common mode.

Differential mode is when two different input is applied V_1 & V_2. $\boxed{V_1 \neq V_2}$

The gain of Differential mode is

$$A_d = \frac{V_o}{V_1 - V_2} = \frac{V_o}{V_{in}} = \frac{V_o}{V_d}$$

Common mode is when both input are Same $\boxed{V_1 = V_2}$

The gain of Common mode is

$$A_c = \frac{V_o}{V_c} = \frac{V_o}{\frac{V_1+V_2}{2}} = \frac{V_o}{\frac{V_1+V_1}{2}} = \frac{V_o}{V_1}$$

The total output of differential Amplifier

$$V_{out} = A_d V_d + A_c V_c.$$

Common Mode Rejection Ratio (CMRR) :-

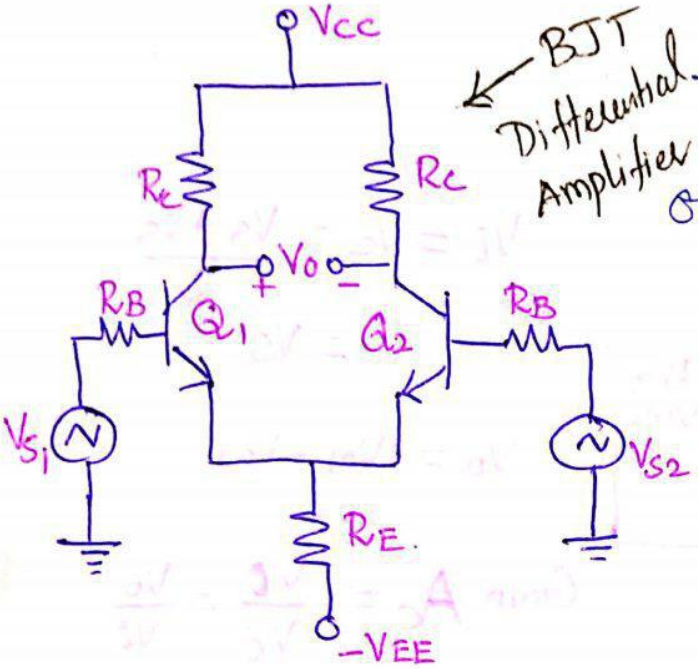
The ability of a differential amplifier to reject a common mode signal is defined by a ration called Common Mode Rejection Ratio. and is defined as ratio of the differential voltage gain A_d to Common mode gain A_c

$$CMRR = \frac{|A_d|}{|A_c|}$$

$$CMRR\,(dB) = 20 \log \frac{|A_d|}{|A_c|}$$

Differential Amplifier using BJT :-

The basic BJT Differential Amplifier with Dual input, balance output is shown in figure.



BJT Differential Amplifier

There are two mode of operation

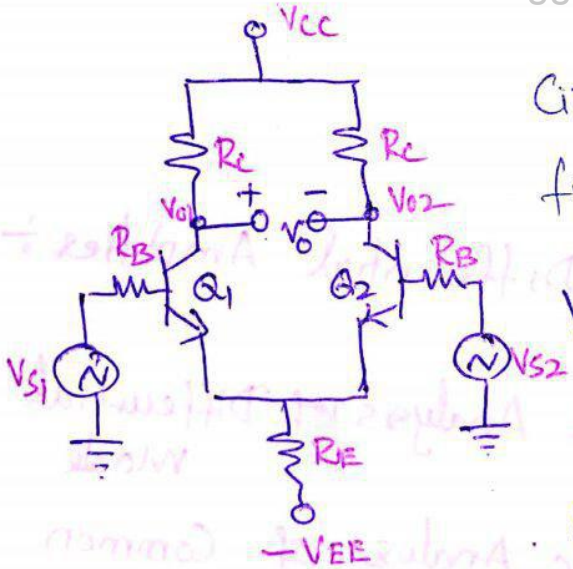
i) Differential mode

ii) Common mode

Differential mode :-

The two input signals are different from each other $V_{s1} \neq V_{s2}$

The Differential mode Circuit is shown in figure.



$V_d = V_i = V_{s1} - V_{s2}$

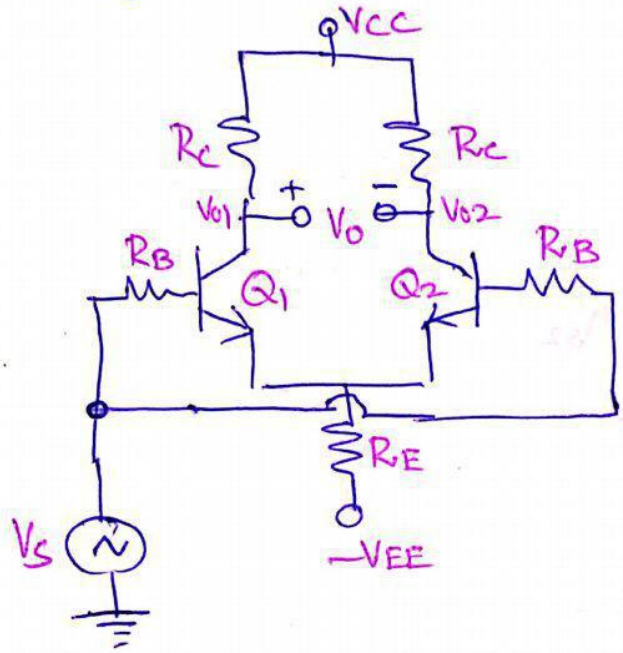
$V_o = V_{o1} - V_{o2}$

Gain $A_d = \frac{V_o}{V_i} = \frac{V_o}{V_d}$

Common Mode :-

The two input signal are same $V_{s1} = V_{s2}$ (ie., both input are connected

together) as shown in figure.



$$V_i = V_c = \frac{V_s + V_s}{2}$$

$$= V_s$$

$$V_o = V_{o1} - V_{o2}$$

$$\text{Gain } A_c = \frac{V_0}{V_c} = \frac{V_o}{V_i}$$

$$A_c = \frac{V_{o1} - V_{o2}}{V_s}$$

Common mode Rejection Ratio :-

$$CMRR = \frac{|A_d|}{|A_c|}$$

$$CMRR(dB) = 20 \log \frac{|A_d|}{|A_c|}$$

Ac Analysis of Differential Amplifier :-

- Ac Analysis of Differential mode
- Ac Analysis of Common mode.

Ac Analysis of Differential mode :-

For differential mode the input are different to easy analysis

We assume

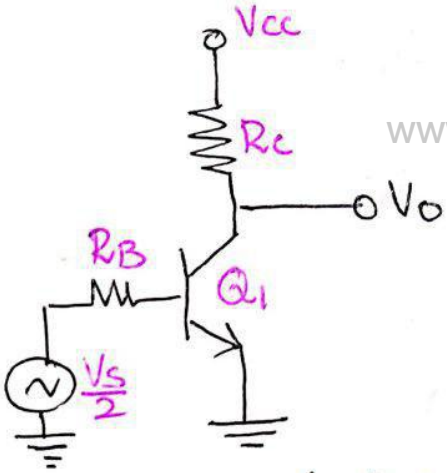
$$V_{S1} = -V_{S2} = \frac{V_S}{2}$$

that is equal in magnitude but having 180° phase shift.

$$V_{in} = V_d = \frac{\frac{V_S}{2} - \left(-\frac{V_S}{2}\right)}{2} = \frac{\frac{V_S}{2} + \frac{V_S}{2}}{2}$$

$$V_d = V_S$$

For easy analysis only one side of differential Amplifier is take for Ac equivalent circuit as shown in figure.



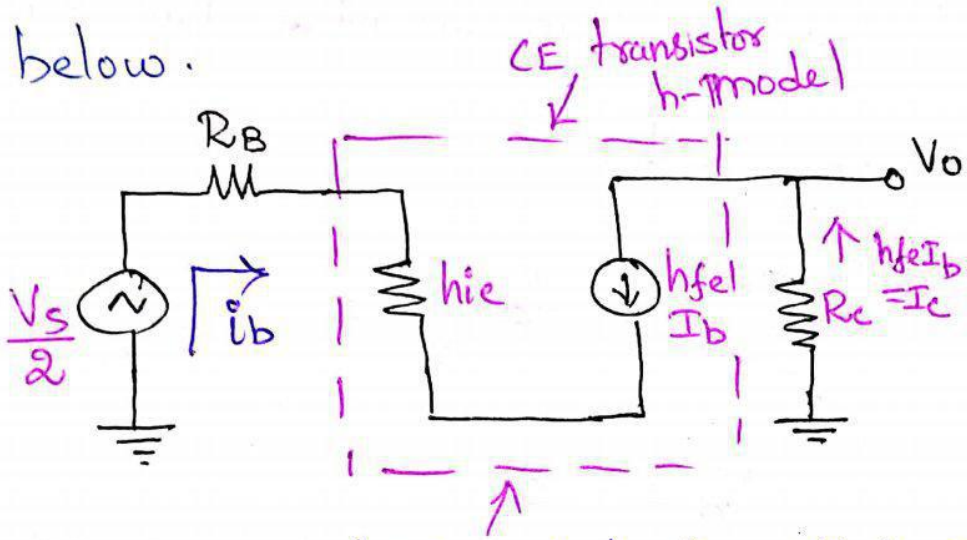
Ac equivalent Circuit for Differential mode

In ac equivalent Circuit of Differential mode R_E and V_{EE} is removed because $i_{e1} = -i_{e2}$ as we apply $\frac{V_S}{2}$ and $-\frac{V_S}{2}$ as input. So total current in emitter resistor $i_e = i_{e1} + i_{e2}$

$$i_e = 0$$

note
$i_{e1} = -i_{e2}$

The approximate hybrid parameter model for Differential mode is shown below.



$h_{re}V_{CE}$ and $\frac{1}{h_{oe}}$ is omitted as it is very small.

Apply KVL to the input loop.

$$\frac{V_s}{2} = i_b R_B + i_b h_{ie}$$

$$i_b = \frac{V_s}{2(R_B + h_{ie})}$$

Apply KVL to the output loop.

$$V_o = -h_{fe} I_b R_c$$

$$V_o = -h_{fe} R_c \left[\frac{V_s}{2(R_s + h_{ie})}\right]$$

Note

$V_d = \frac{V_s}{2} - \left(-\frac{V_s}{2}\right)$

$= V_s$

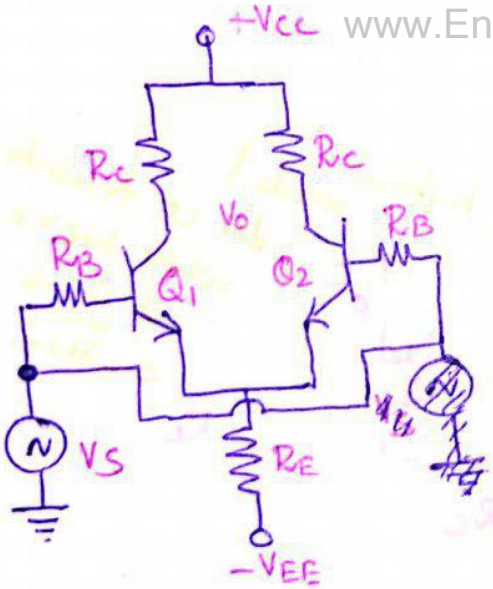
$$\frac{V_o}{V_s} = \frac{-h_{fe} R_c}{2(R_s + h_{ie})} = \frac{V_o}{V_d}$$

To get balance output across the two collector of Q_1 and Q_2 2 is multiplied in gain

$$\therefore A_d = \frac{V_o}{V_s} = \cancel{2} \times \frac{-h_{fe} R_c}{\cancel{2}(R_B + h_{ie})}$$

$$|A_d| = \frac{h_{fe} R_c}{R_B + h_{ie}}$$

Common mode :-



when the inputs V_1 and V_2 are equal $V_1 = V_2$

∴ both input signals be Vs and are inphase with each other.

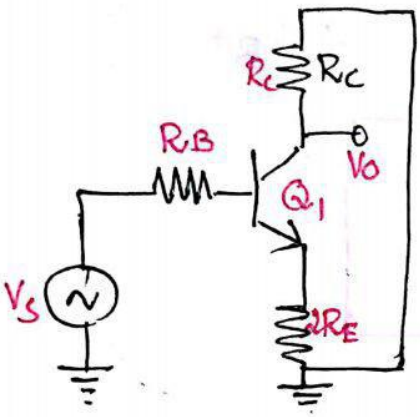
The Common mode input

$$V_c = \frac{V_1 + V_2}{2} = \frac{V_s + V_s}{2} = V_s$$

Common mode gain

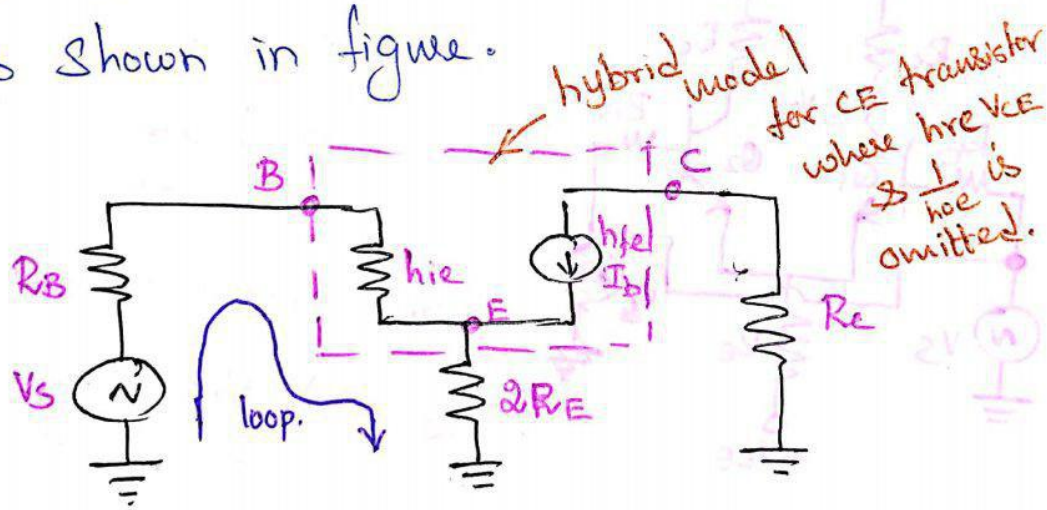
$$A_c = \frac{V_o}{V_{in}} = \frac{V_o}{V_c} = \frac{V_o}{V_s}$$

As both inputs are equal, the emitter current $I_{e1} = I_{e2} = I_e$, flows through R_E in the same direction. Hence the total current following through R_E is $2I_e$.



Ac equivalent circuit for common mode differential Amplifier is shown in figure. By short circuit all dc supplies & capacitors

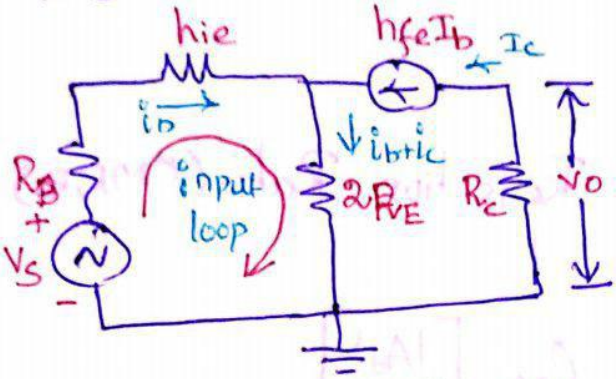
An Approximate hybrid model for Common mode differential amplifier is shown in figure.



Note :-

Here $2R_E$ is present because emitter current $2I_e$ flows in R_E resistor

Apply KVL at the input loop, we get.



$$V_S = I_b R_B + I_b hie + I_e 2R_E$$

$$V_S = I_b R_B + I_b hie + (I_b + I_c) 2R_E$$

$$= I_b R_B + I_b hie + (I_b + h_{fe} I_b) 2R_E$$

$$V_S = I_b [R_B + hie + 2(1+h_{fe}) R_E]$$

Apply KVL at the output loop we get

$$V_o = -i_o R_c$$

$$V_o = -h_{fe} I_b R_c$$

Common mode Gain $\frac{0}{0}$

$$A_c = \frac{V_o}{V_c} = \frac{V_o}{V_S}$$

$$= \frac{-h_{fe} I_b R_c}{I_b [R_B + hie + 2(1+h_{fe}) R_E]}$$

$$A_c = \frac{-h_{fe} R_c}{[R_B + hie + 2(1+h_{fe}) R_E]}$$

A_c is same for both balanced and unbalance output.

$$|A_c| = \frac{h_{fe} R_c}{R_B + h_{ie} + 2R_E(1+h_{fe})}$$

Common mode Rejection Ratio (CMRR)

$$CMRR = 20 \log \left[\frac{|A_d|}{|A_c|}\right]$$

$$CMRR = 20 \log \left[\frac{\frac{h_{fe} R_c}{R_B + h_{ie}}}{\frac{h_{fe} R_c}{R_B + h_{ie} + 2R_E(1+h_{fe})}}\right]$$

$$\boxed{CMRR = 20 \log \left[\frac{R_B + h_{ie} + 2R_E(1+h_{fe})}{R_B + h_{ie}}\right]}$$

Input Impedance of differential Amplifier:-

$$Z_i = \frac{V_s}{I_b}$$

we know

$$I_b = \frac{V_s}{2(R_B + h_{ie})}$$

$$\boxed{Z_i = 2(R_B + h_{ie})}$$

output impedance of differential Amplifier:-

$$\boxed{Z_o \approx R_c}$$

3. Draw the circuit of differential amplifier with constant current source and explain its operation and explain how CMRR is improved.

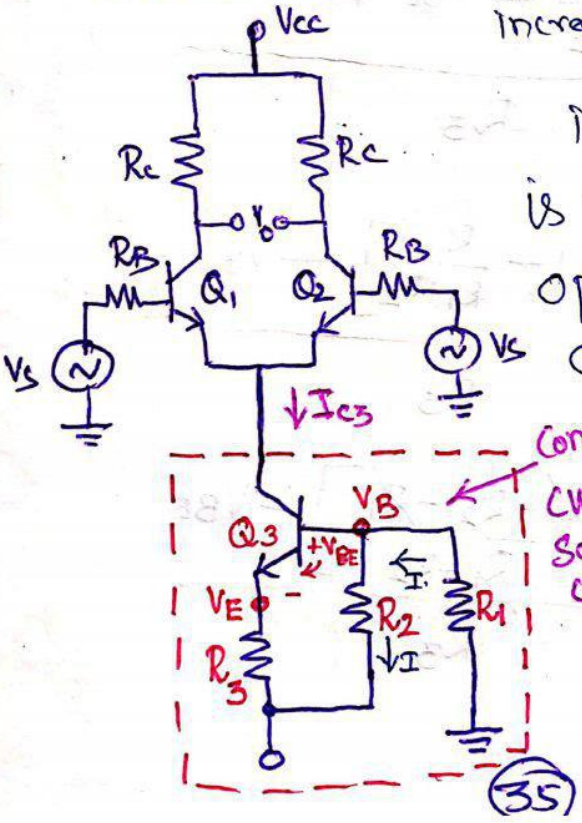
Methods For Improving CMRR :-

Higher the value of CMRR, better the performance of differential amplifier. CMRR can be increase by increasing R_E.

Hence, Practically instead of increasing R_E various other methods are used which provide effect of increased R_E without any limitations.

* Constant Current Circuit method
* Use of Current Mirror Circuit.

Differential Amplifier with Constant Current Circuit.



To increase CMRR, R_E should increase without physically increasing R_E, the R_E is replaced by a transistor operated at a constant current.

The transistor used is Q_3 and the value of R_1, R_2 and R_3 are selected so as to act as Constant Current Source

Apply KvL in Constant Current Source

$-IR_1 - IR_2 = -V_{EE}$ [minus indicate current direction]

$IR_1 + IR_2 = V_{EE}$

$$I = \frac{V_{EE}}{R_1+R_2}$$

$$\therefore V_B = -IR_1$$

$$V_B = \frac{-V_{EE}}{R_1+R_2} \times R_1$$

Now,

$$V_E = V_B - V_{BE} = \frac{-V_{EE}R_1}{R_1+R_2} - V_{BE}.$$

$$I_{E3} = \frac{V_E - (-V_{EE})}{R_3}$$

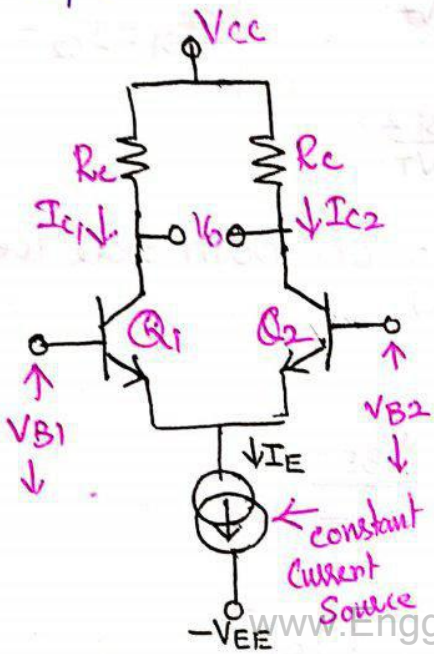
$$I_{E3} = \frac{\frac{-V_{EE}R_1}{R_1+R_2} - V_{BE} + V_{EE}}{R_3}$$

$$I_{E3} = \frac{V_{EE}\left[1 - \frac{R_1}{R_1+R_2}\right] - V_{BE}}{R_3}$$

$$= \frac{V_{EE}\left[\frac{R_1+R_2-R_1}{R_1+R_2}\right] - V_{BE}}{R_3}$$

$$I_{E3} = \frac{V_{EE}\left[\frac{R_2}{R_1+R_2}\right] - V_{BE}}{R_3}$$

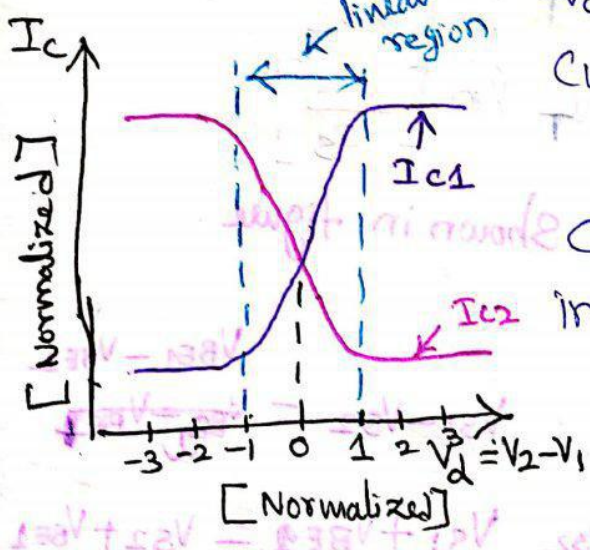
Transfer Characteristics of a Differential Amplifier :-



The dc transfer characteristic is very useful in understanding the large signal behaviour of the differential Amplifier.

It is characteristic is graph drawn between $V_d (V_2 - V_1)$ and output current I_{C1} and I_{C2}

The Transfer characteristics is shown in figure.



Derivation :-

The expression for the Collector Current of Transistor

$$I_C = I_S e^{\frac{V_{BE}}{V_T}}$$

I_S = Reverse Saturation Current.

V_T = Voltage equivalent of temperature.

$$I_{C1} = I_S e^{\frac{V_{BE1}}{V_T}}$$

$$I_{C2} = I_S e^{\frac{V_{BE2}}{V_T}}$$

Note

$I_{S1} = I_{S2} = I_S$

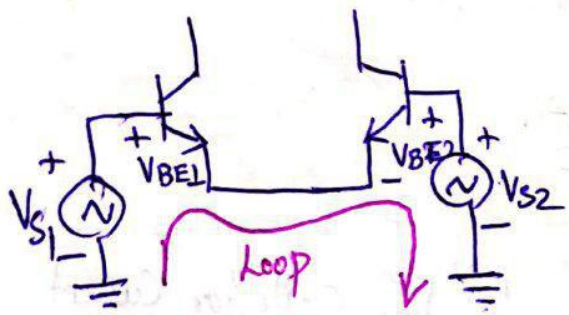
Taking the natural log on both side we get

$$\ln \frac{I_{C1}}{I_S} = \frac{V_{BE1}}{V_T}$$

$$V_{B1} = V_T \ln\left[\frac{I_{C1}}{I_S}\right]$$

$$V_{B2} = V_T \ln\left[\frac{I_{C2}}{I_S}\right]$$

Apply KVL as shown in figure.



$$V_{S1} - V_{S2} = V_{BE1} - V_{BE2}$$

$$V_{S1} + V_{BE2} = V_{S2} + V_{BE1}$$

$$V_{S1} + V_T \ln\left[\frac{I_{C2}}{I_S}\right] = V_{S2} + V_T \ln\left[\frac{I_{C1}}{I_S}\right]$$

$$V_{S1} - V_{S2} = V_T \left[\ln \left(\frac{I_{C1}}{I_S} \right) - \ln \left[\frac{I_{C2}}{I_S} \right] \right]$$

$$V_{S1} - V_{S2} = V_T \left[\ln \frac{\left[\frac{I_{C1}}{I_S} \right]}{\left[\frac{I_{C2}}{I_S} \right]} \right]$$

$$V_{S1} - V_{S2} = V_T \left[\ln \left[\frac{I_{C1}}{I_{C2}} \right] \right]$$

$$\ln \left[\frac{I_{C1}}{I_{C2}} \right] = \frac{V_{S1} - V_{S2}}{V_T} = \frac{V_d}{V_T}$$

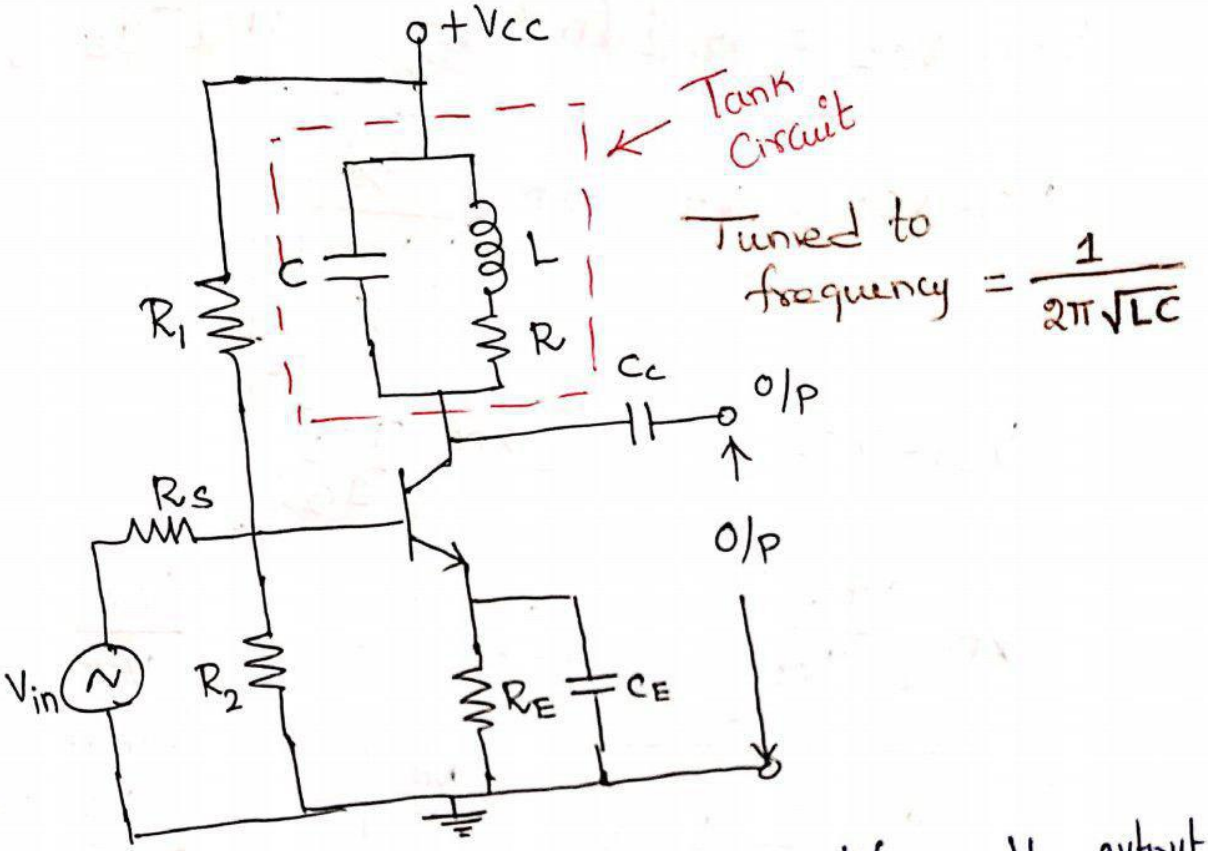
$$\therefore \frac{I_{C1}}{I_{C2}} = e^{\frac{V_d}{V_T}}$$

where $V_{S1} - V_{S2} = V_d$

(4) Draw the Circuit diagram of a Single tuned amplifier and Discuss the frequency response of Single tuned amplifier.

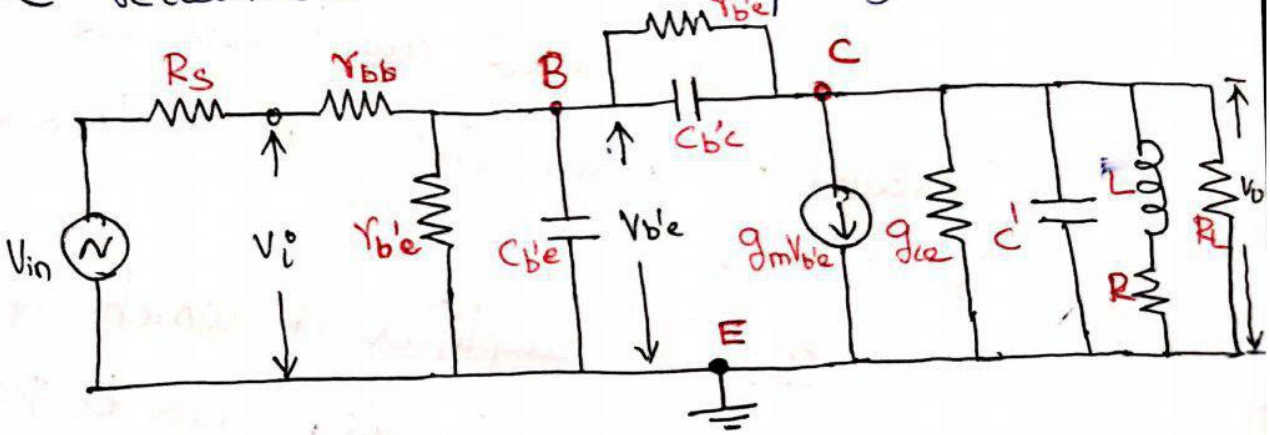
Single tuned amplifiers use one Parallel resonant Circuit as the load impedance in output.

It is amplifier in which the load Circuit is tank Circuit, tuned to pass (or) amplify Selection of a desired frequency.



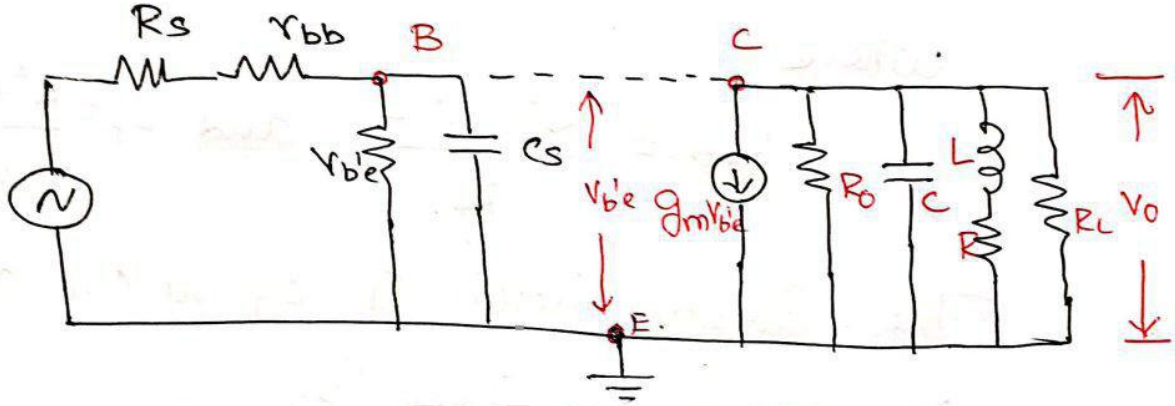
In the single tuned amplifier, the output across the tuned circuit is coupled to the next stage through the coupling capacitor C_c as shown in figure.

The tuned circuit formed by L and C resonates at the frequency of operation.



The modified and Simplified equivalent Circuit obtained by miller's theorem.

The reactance of the bypass Capacitor C_E and the Coupling Capacitor C_c are negligible



where

$$C_S = C_{b'e} + C_1 + C_{b'c}(1-A)$$

$$C = C_{b'c}\left(\frac{A-1}{A}\right) + C_2 + C'$$

and

$$g_{ce} = \frac{1}{r_{ce}} = h_{oe} - g_m h_r \approx h_{oe} = \frac{1}{R_o}$$

The admittance of the inductor along with resistor R is given by

$$Y = \frac{1}{R + j\omega L} = \frac{R - j\omega L}{(R+j\omega L)(R-j\omega L)}$$

$$Y = \frac{R - j\omega L}{R^2 + \omega^2 L^2}$$

$$Y = \frac{R}{R^2+\omega^2L^2} - j\frac{\omega L}{R^2+\omega^2L^2}$$

$$Y = \frac{1}{R_P} + \frac{1}{j\omega L_P}$$

where

$$R_P = \frac{R^2+\omega^2L^2}{R} \quad \text{and} \quad L_P = \frac{R^2+\omega^2L^2}{\omega^2 L}$$

The Quality factor Q of the coil at resonance is given by

$$Q_0 = \frac{\omega_0 L}{R}$$

$\omega_0 = \frac{1}{\sqrt{LC}}$ is the frequency of resonance of the circuit.

Q_0 of the coil is usually large so that $\omega L >>> R$

$$\therefore \frac{R}{\omega^2 L^2} <<< 1$$

$$R_p = \frac{R^2+\omega^2L^2}{R} = \frac{R\left(R+\frac{\omega^2L^2}{R}\right)}{R}$$

$\frac{\omega^2L^2}{R} >>>> R$ [R is neglected]

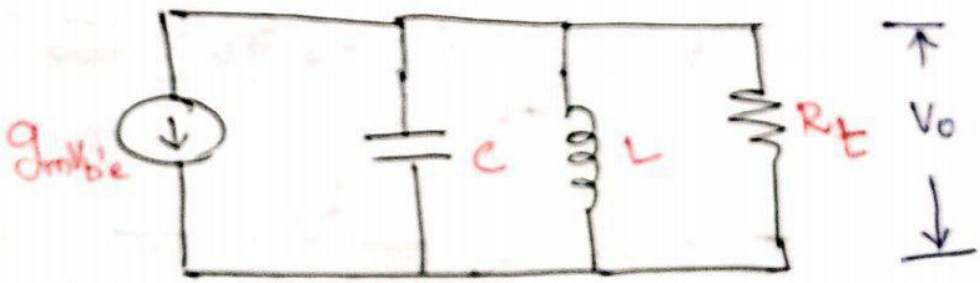
$$\boxed{R_p = \frac{\omega^2L^2}{R}}$$

Illy $L_p = \frac{R^2+\omega^2L^2}{\omega^2L} = \frac{\omega^2L\left[\frac{R^2}{\omega^2L}+L\right]}{\omega^2L}$

$\frac{R^2}{\omega^2L} << 1$ [$L\frac{R^2}{\omega^2L}$ is neglected]

$\boxed{L_p \approx L}$ $\boxed{\text{ie, } L_p \simeq L}$.

The output Circuit of the amplifier can be modified and simplied as.



$$\frac{1}{R_t} = \frac{1}{R_0} + \frac{1}{R_p} + \frac{1}{R}$$

$$V_0 = -g_m V_{b'e} \cdot Z$$

where $Z = \frac{1}{Y}$ and $Y = \frac{1}{R_t} + \frac{1}{j\omega L} + j\omega C$

$$Y = \frac{1}{R_t}\left[1 + \frac{R_t}{j\omega L} + j\omega C R_t\right]$$

multiplying numerator and denominator by ω_0

$$Y = \frac{1}{R_t}\left[1 + \frac{R_t \omega_0}{j\omega L \omega_0} + \frac{j\omega\omega_0 C R_t}{\omega_0}\right]$$

Substituting $\frac{R_t}{\omega_0 L} = \omega_0 C R_t = Q_0$

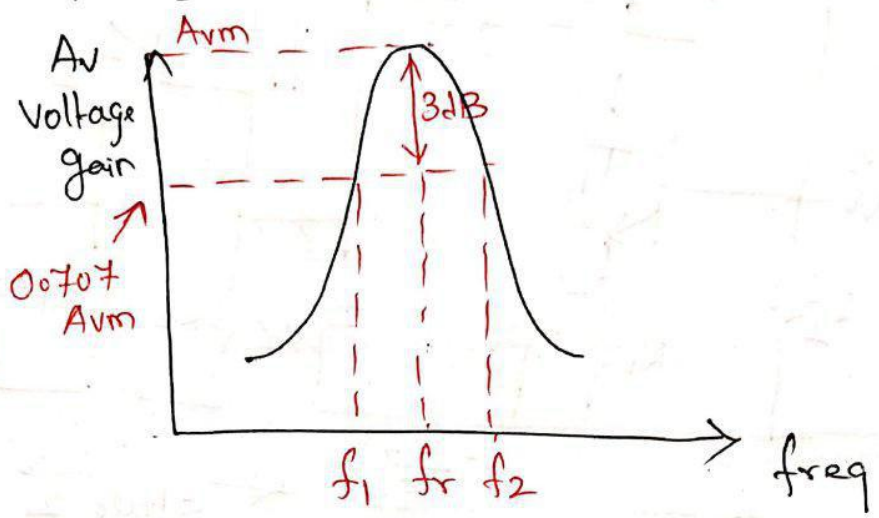
$$Y = \frac{1}{R_t}\left[1 + \left[\frac{\omega_0}{j\omega} + \frac{j\omega}{\omega_0}\right] Q_0\right]$$

$$Y = \frac{1}{R_t}\left[1 + j Q_0\left[\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right]\right]$$

$$Z = \frac{1}{Y} = \frac{R_t}{1 + jQ\left[\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right]}$$

$$V_o = -g_m V_{b'e} \cdot \left[\frac{R_t}{1 + jQ\left[\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right]} \right]$$

frequency response of tuned amplifier



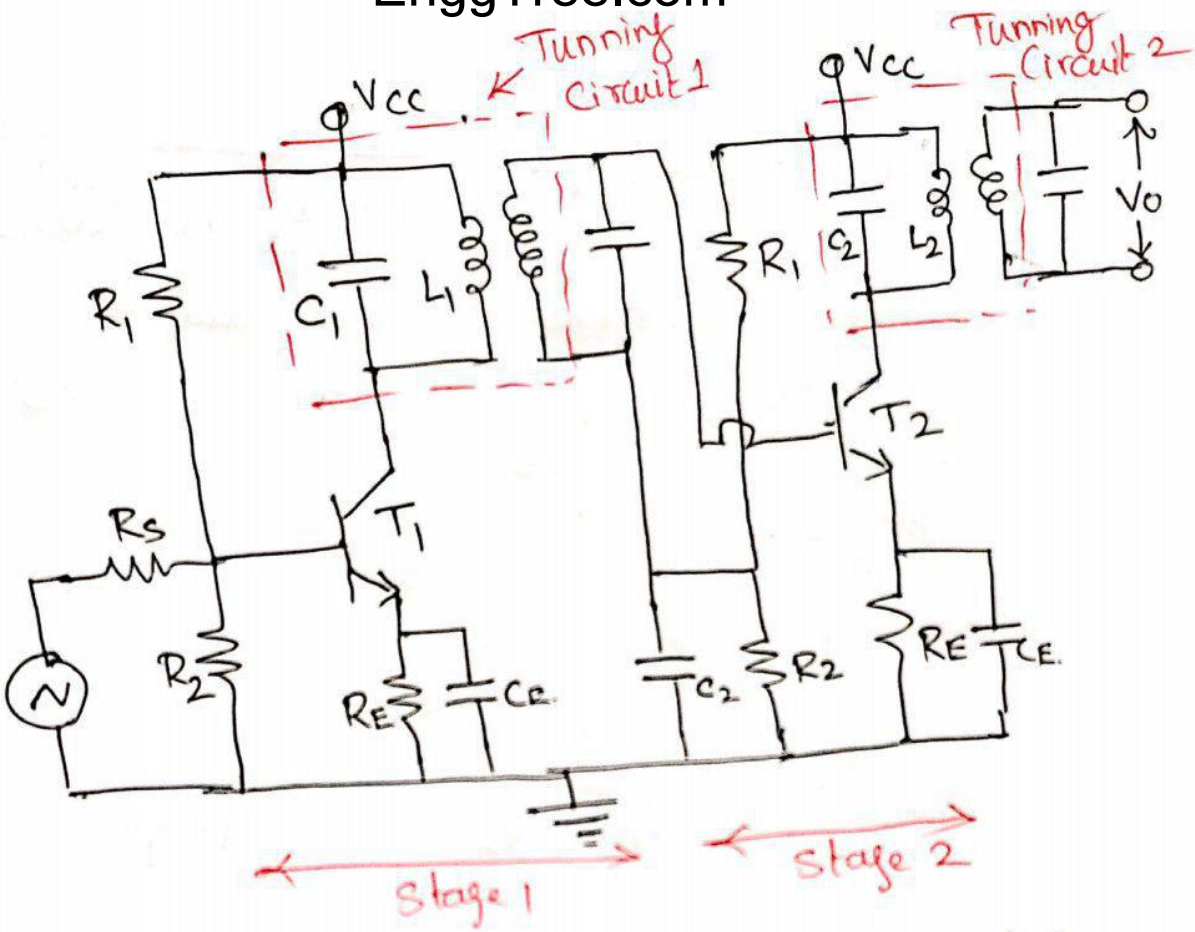
$$f_r = \frac{1}{2\pi\sqrt{LC}} \qquad B.W = f_2 - f_1$$

$$\Delta f = \frac{1}{2\pi R_t C}$$

---

(5) Draw the Circuit diagram of a double tuned amplifier and explain its frequency response.

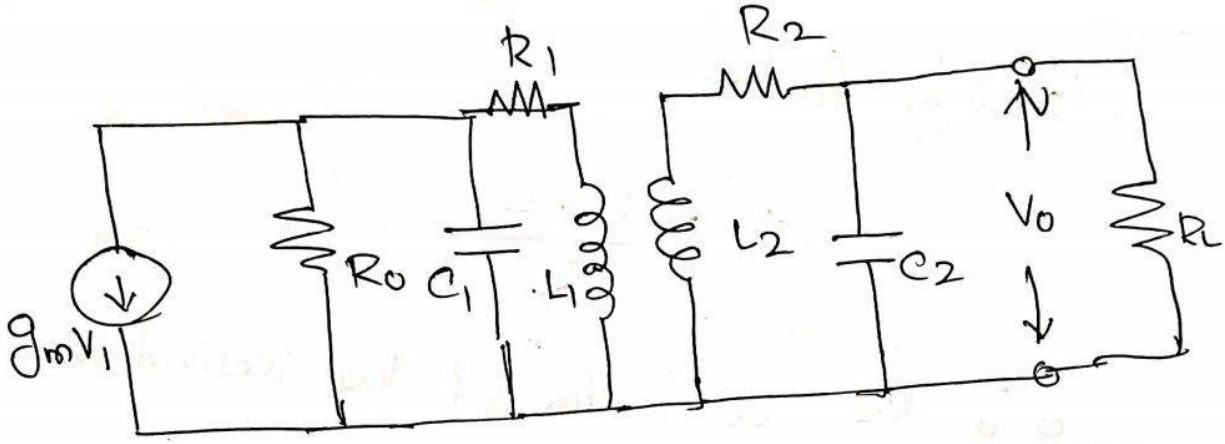
The double-tuned amplifier has two tuned circuits which are coupled inductively.



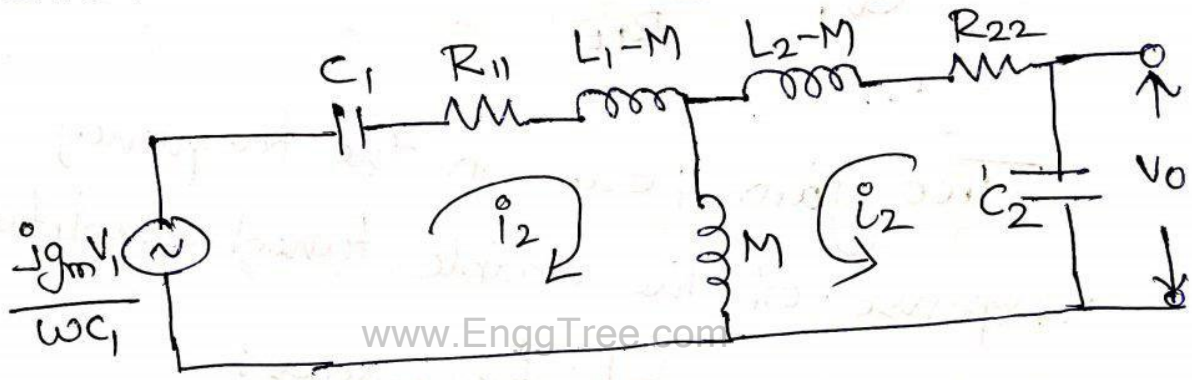
both tuned circuits are tuned to the same frequency.

The double tuned circuit can Provide a bandwidth of Seaval Percent of the resonant frequency and gives Steep Sides to the response Curve.

The equivalent Arcuit for double tuned amplifier is Shown in figure below.



Using mutal Impedance M the above Circuit is Simplified as



In above Circuit Current Source is Converted in Voltage Source..

In Simplified equivalent Circuit the Series and Parallel resistances are Combined into Series elements

$$R_P = \frac{\omega^2 L^2}{R}$$

∴ we Can write $R_{11} = \frac{\omega_0^2 L_1^2}{R_0} + R_1$

$$R_{22} = \frac{\omega_0^2 L_2^2}{R_L} + R_2.$$

Quality factor

$$Q = \frac{\omega_r L}{R}$$

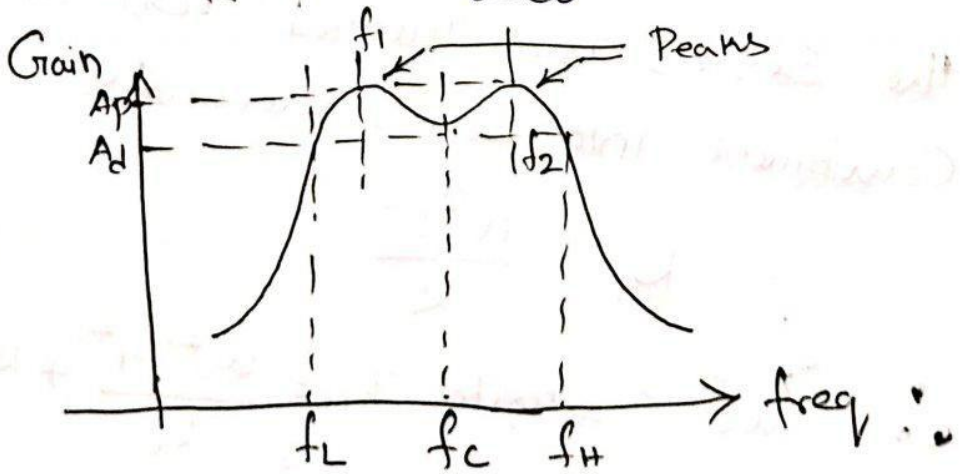
∴ The Q factor of the individual tank circuits are

$$Q_1 = \frac{\omega_r L_1}{R_{11}} \quad \text{and} \quad Q_2 = \frac{\omega_r L_2}{R_{22}}.$$

Two gain peaks in the frequency response of the double tuned amplifier can be given at frequencies:

$$f_1 = f_r \left[1 - \frac{1}{2Q}\sqrt{K^2Q^2 - 1}\right] \text{ and}$$

$$f_2 = f_r \left[1 + \frac{1}{2Q}\sqrt{K^2Q^2 - 1}\right]$$



~~We know that~~

Advantage of double tuned Amplifier

* Greater Bandwidth

$$B.W = \frac{3.1\, f_r}{Q}$$

which is substantially greater than 3 dB bandwidth of single tuned amplifier.

* Possesses a flatter response having steeper sides

* Providing large gain bandwidth Product.

(8) Explain the techniques used for neutralization with neat diagram?

At higher frequency, the inter junction Capacitance between base and Collector, C_{bc} of the transistor became dominant.

This ~~feedback~~ Capacitor C_{bc} act as Positive feedback and Causes oscillation and Can stop working as an amplifier. and tuned amplifier losses its Stability.

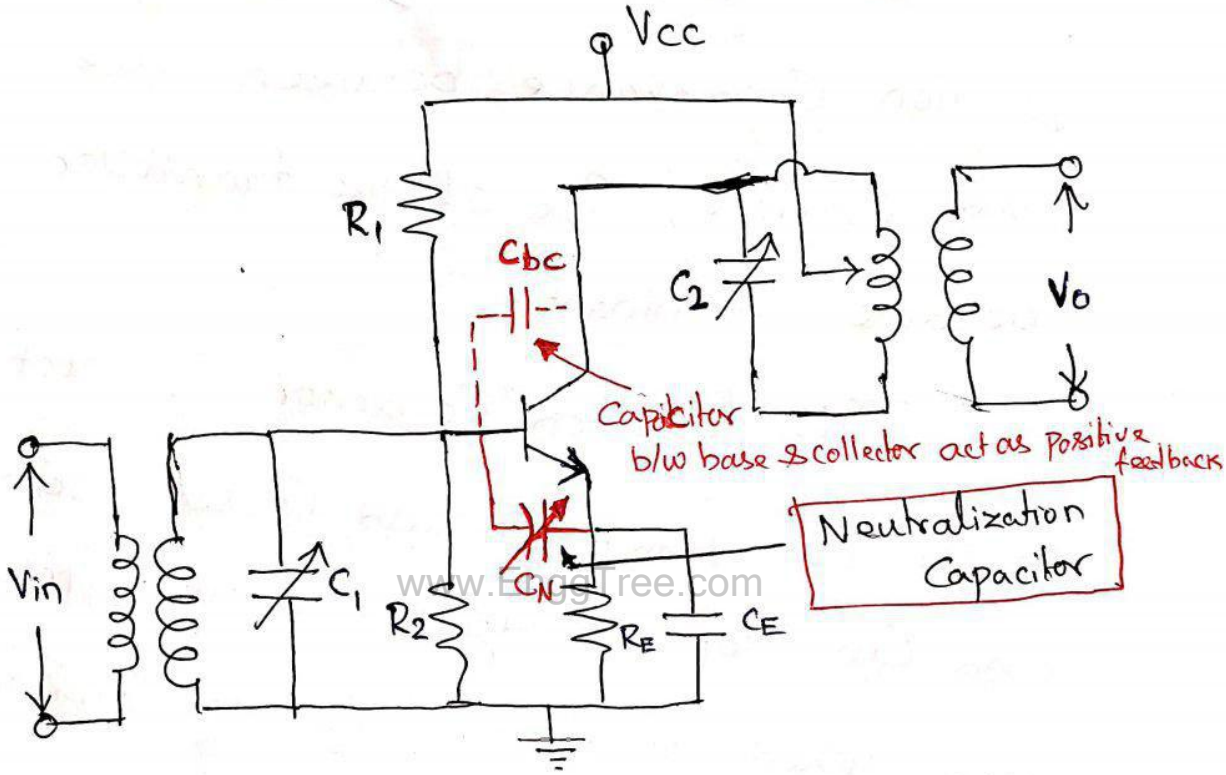
To Prevent oscillations in tuned amplifier and to ensure the Circuit Stability we use Neutralization technique.

Types of Neutralization Circuits.

* Hazeltine Neutralization.
* Modified Hazeltine (Neutrodyne) Neutralization
* Neutralization using Coil.

Hazeltine Neutralization :-

The Hazeltine Neutralization Circuit is shown in figure below.



When the tuned amplifier working in higher frequency. The depletion region between Collector to base act as transistion (reverse bias) Capacitance C_{bc} as shown in figure with doted lines.

This Capacitance C_{bc} is Connected between output (collector) and to input (base) act as positive feedback

which make to amplifier working as Oscillator. and reduce the stability of tuned amplifier.

To Compansate this C_{be} Capacitor and neutralization Capacitor C_N is Conneted between the base and emitted to nullify the effect

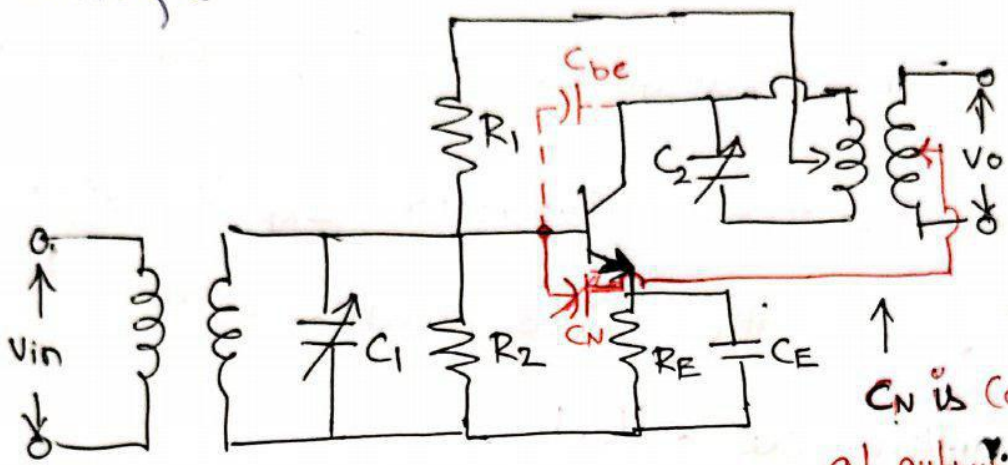
This Capacitor C_N Provides Signals of opposite polarity to Compansate the effect of collector to base Capacitor signal.

Modified Hazeltine Neutralization:-

Modified Version of hazeltine neutralization called Neutrodyne neutralization technique.

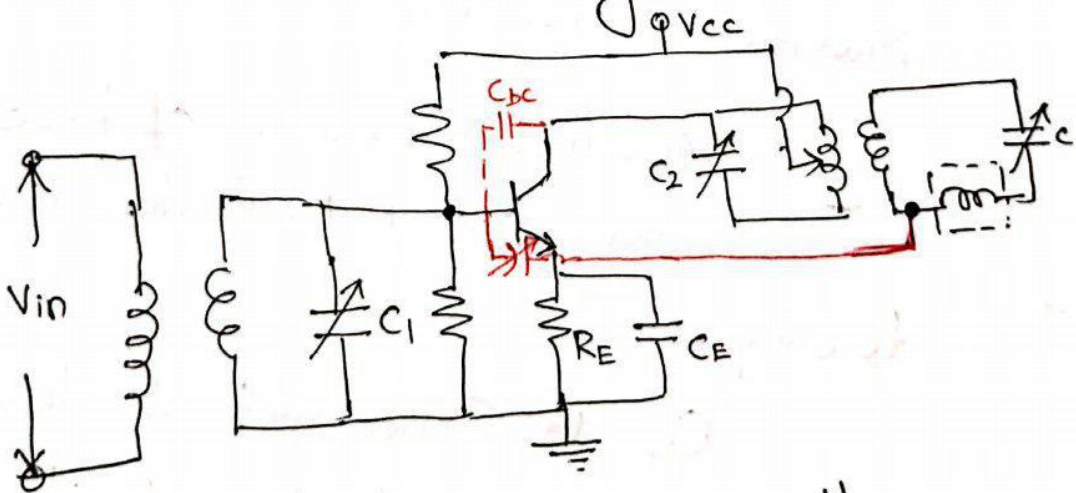
C_N is Connected to the lower end of Secondary Coil of next Stage

Hence it is connected with Vcc, it is insesitive to any vaeiation in Supply voltage



It Provides higher Stabilization for the tuned amplifier.

~~Net~~ Neutralization using Coil:-



Neutralization using Coil.

The figure shows the tuned circuit at the base of the next stage is oriented for minimum coupling to the other windings.

It is mounted at right angles to the coupled windings.

If the windings are properly polarized, the voltage across L due to the circulating current in the base circuit.

Advantages :-

* Amplify defined frequencies.
* Good signal to noise at o/p.
* Suitable for radio transmitter & receiver.

Disadvantages :-

* bulky circuit
* Costly
* not suitable for audio frequency.

UNIT -4

FEEDBACK AMPLIFIRS AND OSCILLATORS

Advantages of negative feedback - Voltage/ Current, Series, Shunt feedback amplifiers, - Positive feedback - Condition for oscillation, Phase Shift - wien bridge, Hartley, Colpitts and Crystal oscillators.

Unit IV: Feedback Amplifiers and Oscillators

PART - A

1. Differentiate voltage and current feedback in amplifiers.

In voltage feedback, feedback voltage V_f is proportional to output voltage V_o and in current feedback, feedback voltage V_f proportional to the output current I_o.

2. Define positive and negative feedback?

Positive Feedback: If the feedback voltage (or current) is so applied as to increase the input voltage (i.e., it is in phase with it), then it is called positive feedback.

Negative Feedback: If the feedback voltage (or current) is so applied as to reduce the input voltage (i.e., it is 180° out of phase with it), then it is called negative feedback.

3. What are the advantages of negative feedback (or) Why do you prefer negative feedback in amplifier?

Advantages of Negative Feedback

1. Negative feedback stabilizes the gain of the amplifier.
2. There is a significant increase in the bandwidth of the amplifier.
3. Distortions in the amplifier output are reduced.
4. Input resistance increases for certain feedback configurations.
5. Output resistance decreases for certain feedback configurations.
6. Operating point is stabilized.

4. List out four different ways of connecting the feedback amplifier.

Different ways of connecting the feedback amplifier are

1. Voltage series feedback
2. Voltage shunt feedback
3. Current series feedback
4. Current shunt feedback

5. What is Barkhausen Criterion?

For getting sustained oscillations we should satisfy the following two conditions.

(i) The loop gain should be unity

(ii) The loop phase shift should be 0° or 360°. ie., $\beta_v A_v = 1$. This criterion is known as Barkausen's criterion for oscillation.

6. What are the factors needed to choose type of oscillators?

The factors needed to choose type of oscillators are

i. The nature of generated wave form.
ii. The frequency of generated signals
iii. The type of associated circuit of components.
iv. The fundamental mechanism involved.

7. What is resonant circuit oscillator?

The oscillator using resonant LC tank circuits are more often used for sources of radio frequency energy are called as resonant circuit oscillator.

8. What is the difference between amplifier and oscillator?

In an amplifier circuit, the frequency waveform and magnitude of ac power generated is controlled by ac signal voltage applied at the input of the amplifier in the other hand in an oscillator the frequency, waveform and magnitude of ac power generated is controlled by the circuit itself i.e. no external controlling voltage is required. Thus an oscillator may be considered as an amplifier which provides its own input signal.

9. Why RC phase shift oscillators are needed?

For the generation of low frequency signal as the LC circuits become impracticable and the RC phase shift oscillators are more suitable with the advantage of IC technology RC network is the only feasible solution. It is very difficult to make an inductance that too of very high value in an IC. Therefore RC oscillators are increasingly popular.

10. Which oscillators use both positive and negative feedback? Why?

Wien bridge oscillator uses both positive and negative feedback. The positive feedback ensures sustained oscillation, the negative feedback ensures constant output ie., any increase or decrease in the oscillator output is taken care of by this negative feedback.

11. What are the advantages of crystal oscillator?

i. Simple circuit since no tuned circuit is needed other than the crystal itself hotel is used.

ii. Different frequencies of oscillations can be obtained by simply replacing one crystal another. Hence it makes it easy for a radio transistor to work at different frequencies.

iii. Since the frequency of oscillation is set by the crystal, changes in the supply VS and transistor parameters does not affect the frequency of oscillation.

12. Name two low frequency oscillators.

i. RC phase shift oscillator
ii. Wien bridge oscillator

13. Name two high frequency oscillators.

i. Hartley Oscillator
ii. Colpitt's Oscillator

14. Why crystal oscillators are superior than other oscillators?

Crystal oscillators are superior than other oscillators because of their great mechanical strength, simplicity of manufacture and it obeys the Piezoelectric effect accurately.

15. Write the expression for frequency of oscillation in RC-phase shift oscillator.

$$f_o = \frac{1}{2\pi RC\sqrt{6+4K}} \quad \text{where } K = \frac{RC}{R}$$

Feedback Amplifiers and Oscillators

1. Write Short notes on

   i) Voltage Series feedback
   ii) Voltage Shunt feedback
   iii) Current Series feedback
   iv) Current Shunt feedback.

Feedback is process of part of output is sampled and feedback to the input.

Feedback is defined as the process in which a part of output signal (voltage or current) is returned back to the input.

The amplifier that operates on the Principle of feedback is known as feedback amplifier.

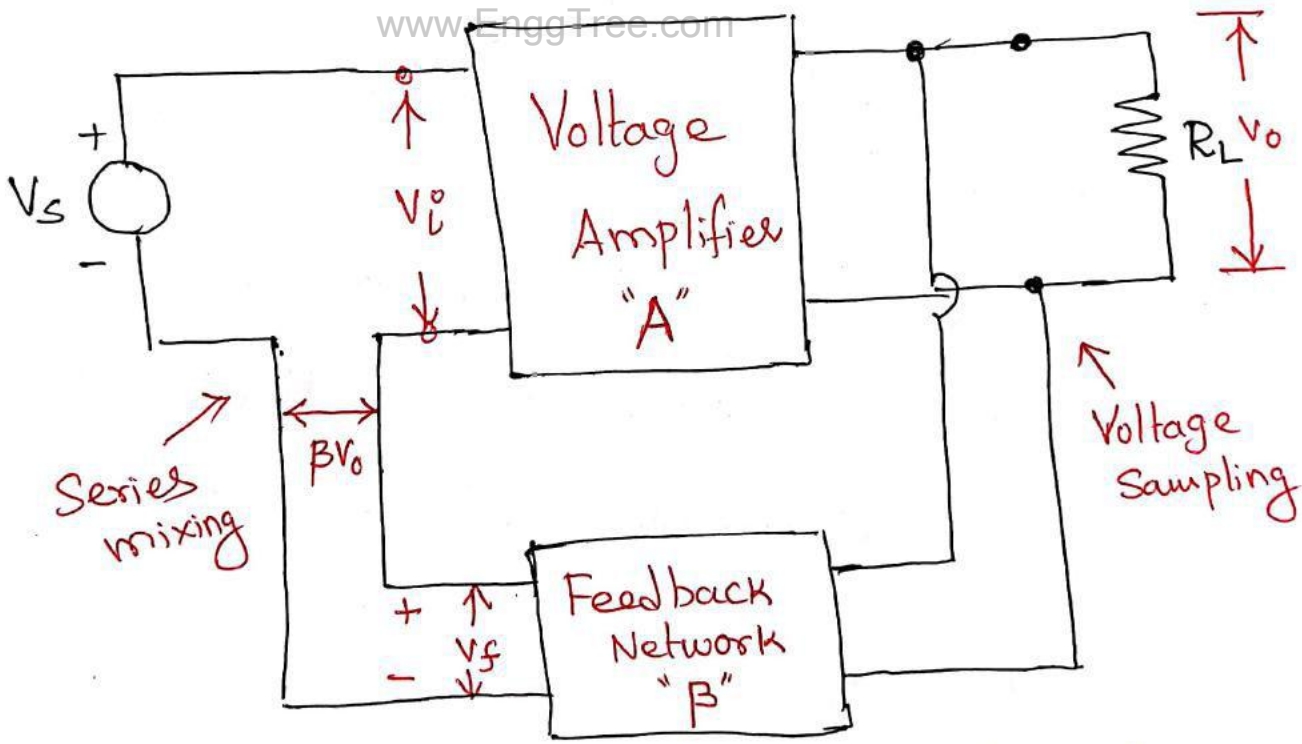
Types of feedbacks.

1. Positive feedback
2. Negative feedback.

Types of feedback based on Sampling and Mixing Network

* Voltage Series Feedback
* Current Series Feedback
* Current Shunt Feedback
* Voltage Shunt Feedback.

* Voltage Series Feedback.



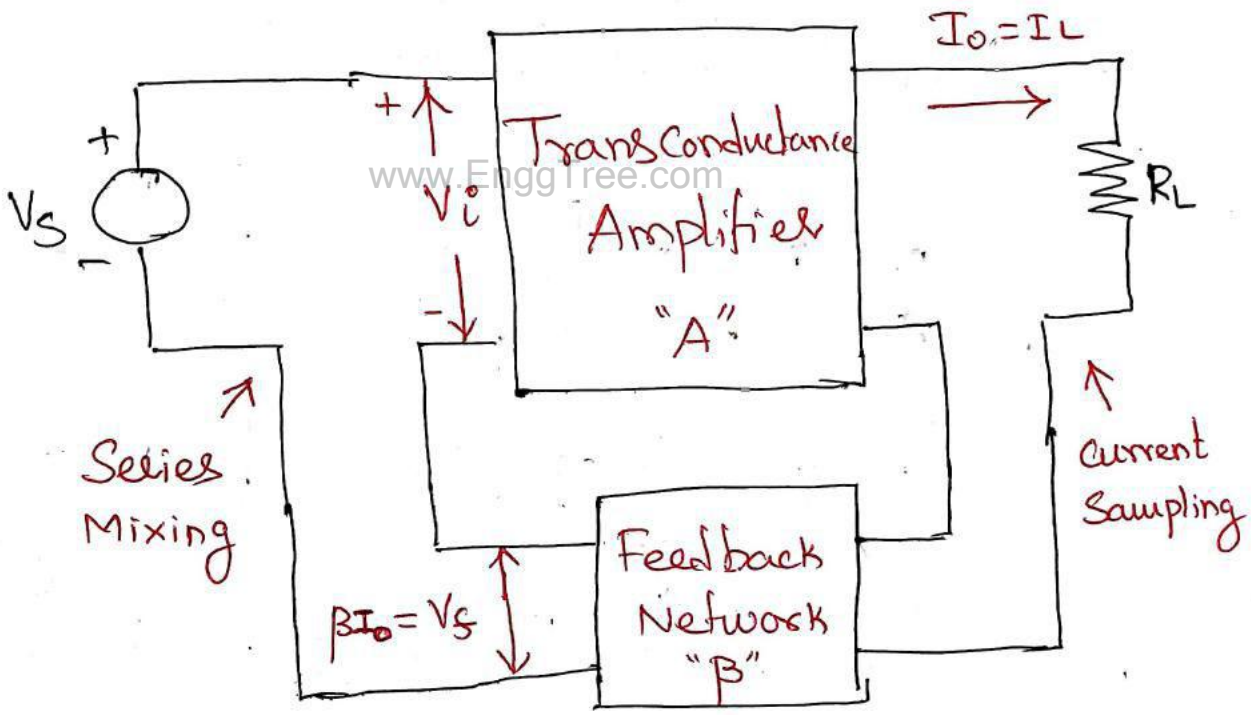
Voltage is Sampled at output and mixed in Series in input with feedback Network "β".

It is also called as series-shunt amplifier.

$$\text{where} \quad A = \frac{V_o}{V_i} \Rightarrow V_o = A \cdot V_i$$

This is also called as voltage Amplifier.

* Current - Series Feedback :-



Here the sampling parameter is current and mixing is series, as shown in figure.

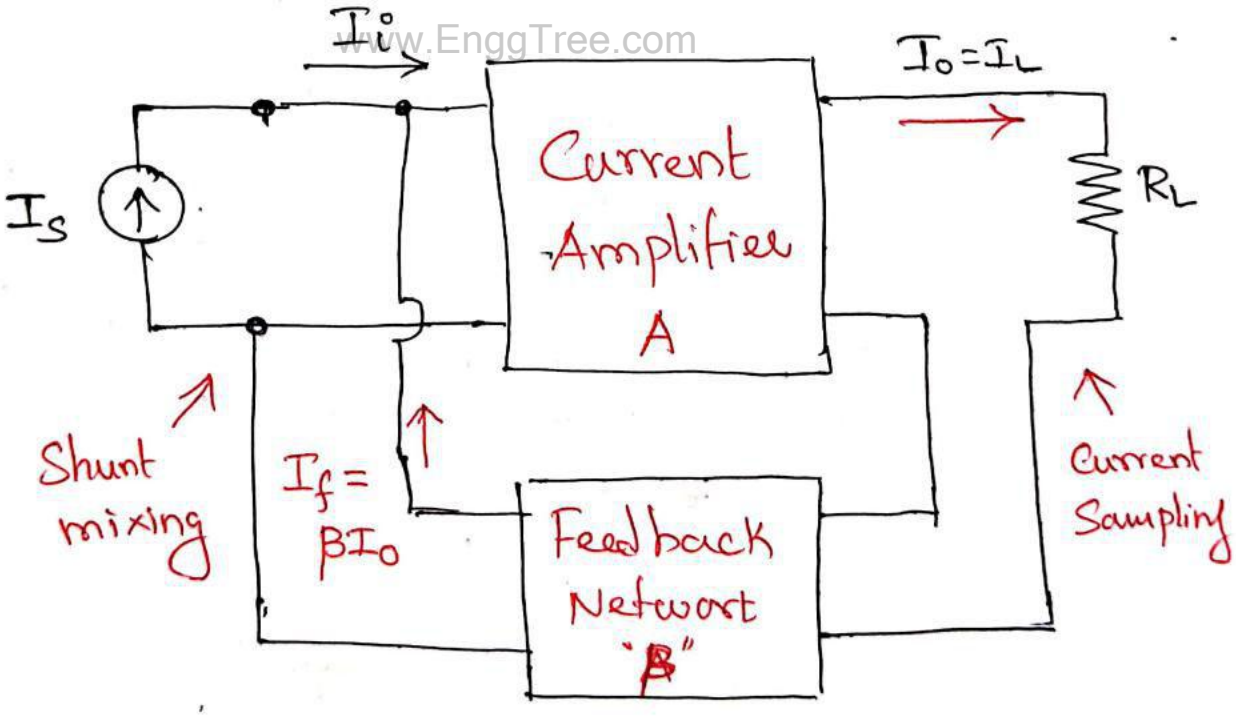
It is also called as series-series feedback amplifier.

$$A = \frac{I_o}{V_i} \quad (or) \quad I_o = A V_i$$

In this case the output Current is directly Proportional to input voltage

This is also called as transconductance Amplifier.

* Current-Shunt feedback :-



Here, the Sampling is Current at output and mixing is Shunt, as shown in figure.

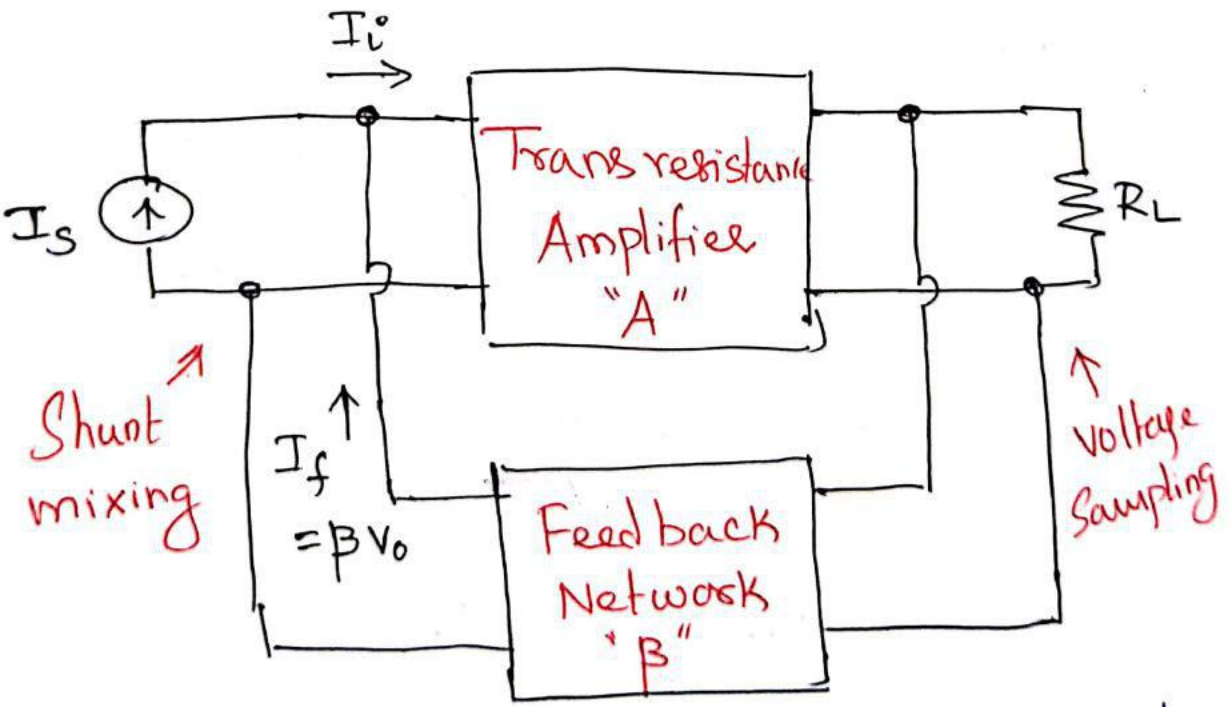
It is also called Shunt - Series feedback amplifier.

In this case, the output current is directly proportional to the input current.

$$A = \frac{I_o}{I_i^\circ} \quad (or) \quad I_o = A \cdot I_i^\circ$$

So it is called Current Amplifier.

* Voltage - Shunt Feedback :-



The Sampling parament is voltage and mixing is Shunt, as shown in figure.

It is also called as Shunt-Shunt feedback.

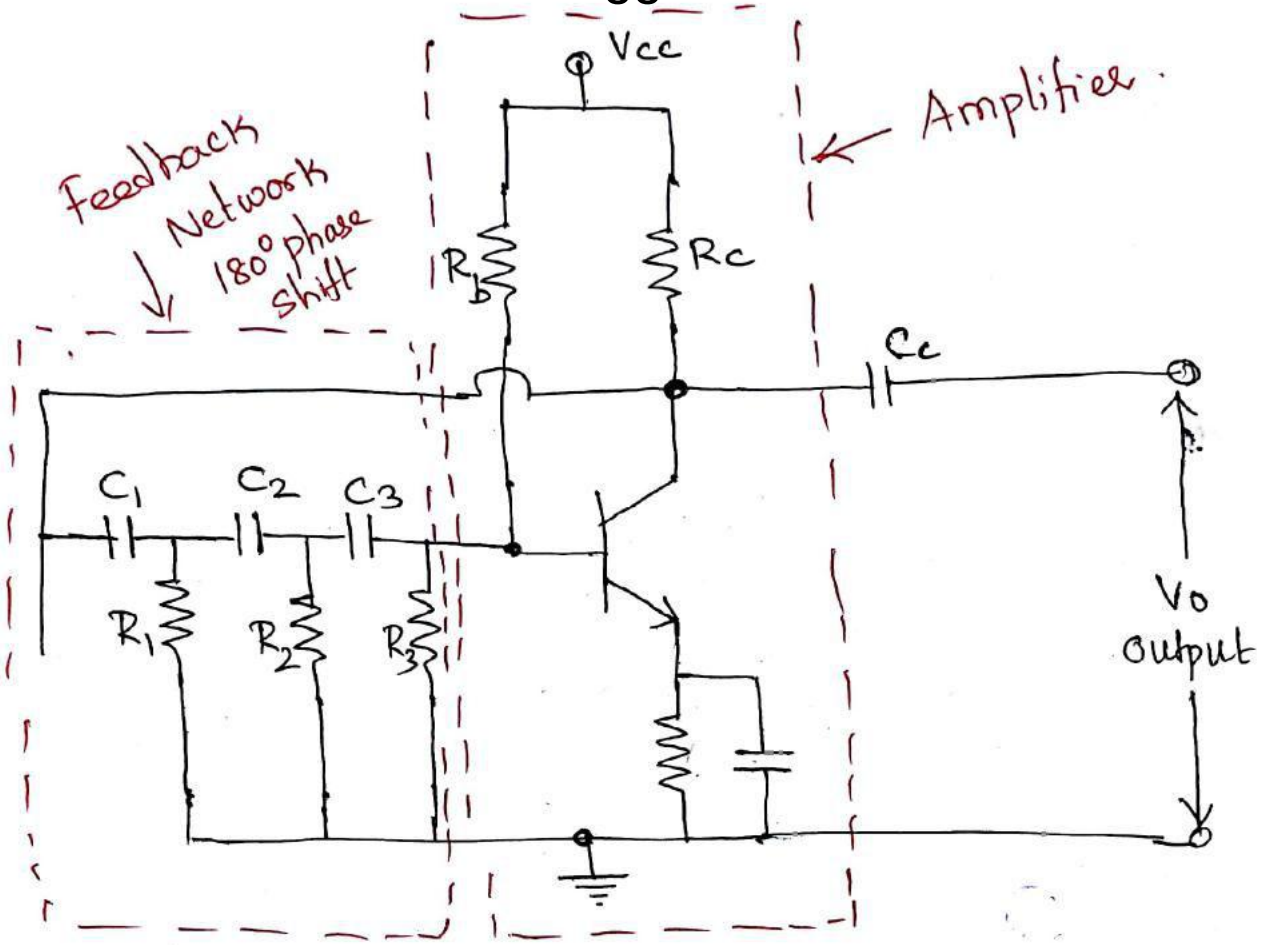
$$A = \frac{V_o}{I_i} \quad \text{(or)} \quad V_o = A \cdot I_i$$

It is also called as Transresistance amplifier.

---

2. With a neat diagram, explain the Construction of BJT RC phase Shift oscillator.

RC phase shift oscillator basically consists of an amplifier and a feedback network consisting of resistor and capacitors arranged in ladde fashion. Hence such an oscillator is also called ladder type RC phase shift oscillator.



The phase shift in each Rc section is 60°. with three Rc section total phase shift is 180° and amplifier (transistor) Produce phase shift of 180°

∴ Total phase shift is 360°.

= Transistor Amplifier phase shift 180° + Feedback Network 3-Rc section 180°

= 360° ← Positive feedback

The frequency of oscillations is given by

$$f_o = \frac{1}{2\pi RC\sqrt{4K+6}}$$

where

$$R = R_1 = R_2 = R_3$$

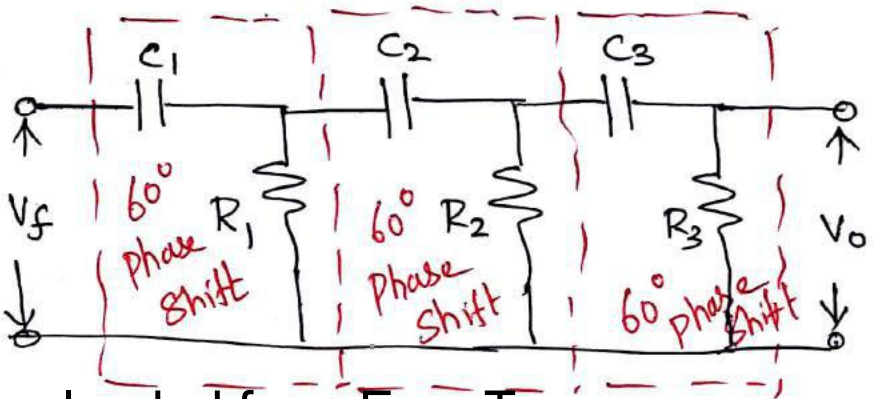
$$C = C_1 = C_2 = C_3$$

$$K = \frac{R_c}{R}$$

Condition for oscillation

$$\angle A\beta = 0^\circ \quad \& \quad |A\beta| = 1$$

$$\phi = \tan^{-1}\left[\frac{1}{2\pi f R_1 C_1}\right] + \tan^{-1}\left[\frac{1}{2\pi f R_2 C_2}\right] + \tan^{-1}\left[\frac{1}{2\pi f R_3 C_3}\right]$$



It is used as Audio frequency oscillator.

Advantage :-

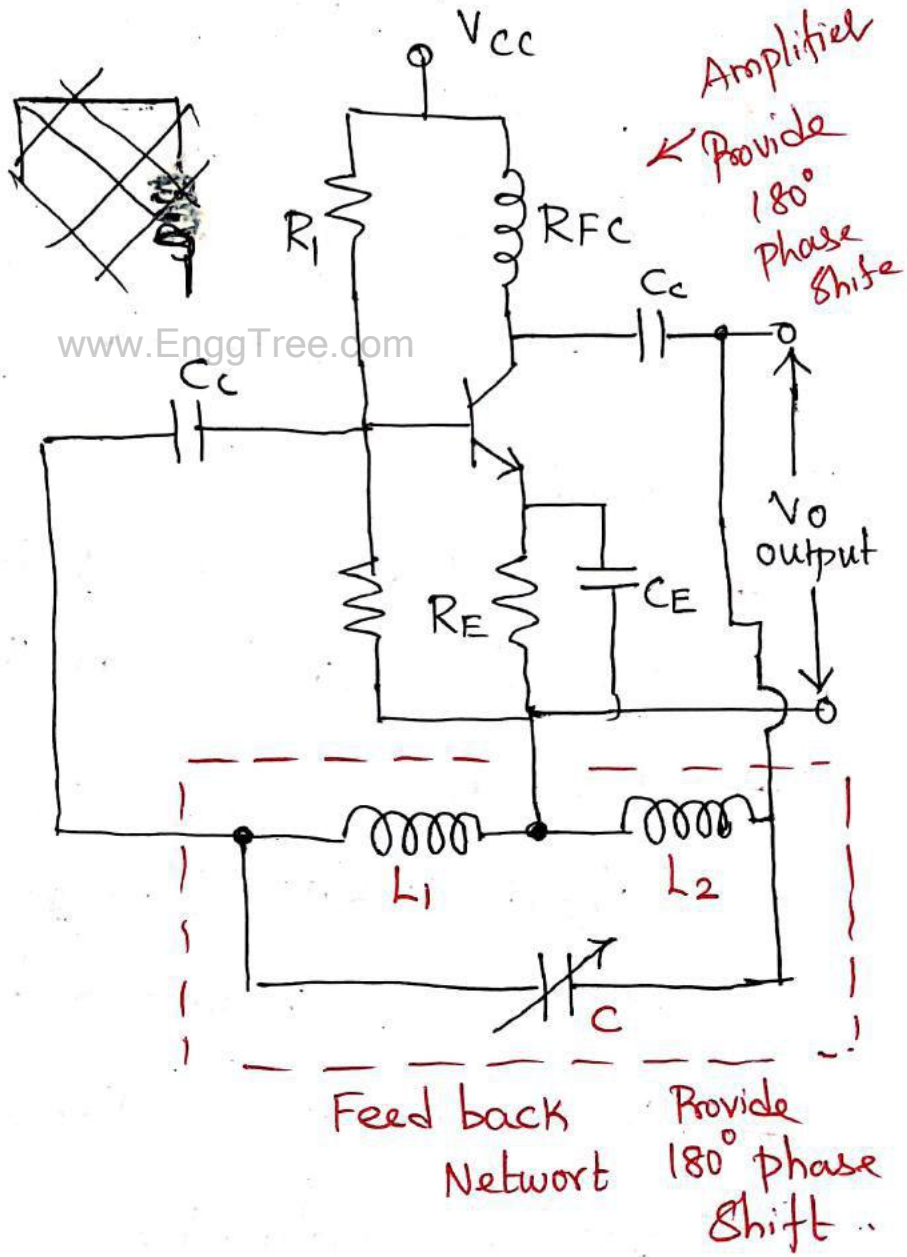
* The Rc phase Shift oscillator is useful over a wide frequency range from a few Hz to Several hundred KHz
* Large Size inductors (or) transformers are not required.
* In the low frequency range, large inductor are required for Lc oscillators which is impractical.

Disadvantages :-

* Gain of transistor must be high to overcome losses in Rc network.
* The upper frequency is limited upto about 10 KHz, because the impedance of the Rc network becomes so small.
* Frequency of oscillation cannot be varied easily, because it is difficult to vary three capacitor simultaneously.

3. Draw the Circuit of a Hartley oscillator and drive the condition for the frequency of oscillation.

Hartley oscillator is shown in figure below.



In Hartley oscillator, L_1 and L_2 are the inductors and C is a Capacitor used in feed back network which Produce the phase shift of 180°.

Resistor R_1, R_2, R_E and RFC with CE are act as Voltage divider bias Provides the necessary d.c. bias to the transistor.

The feedback network Consisting of inductors L_1 and L_2 and Capacitor C determines the frequency of the oscillator.

In the CE Configuration, the transistor Provides the phase difference of 180° between the input and output. and feedback network Provides 180° phase shift.

∴ the total phase shift of 360°.

(Positive feedback)

and loop gain $|A\beta| = 1$, the circuit acts as an oscillator.

To determine the frequency of oscillation

$$X_L = X_C$$

$$\omega_r(L_1 + L_2) = \frac{1}{\omega_r C}$$

$$\omega_r^2 = \frac{1}{(L_1+L_2)C}$$

$$(2\pi f_r)^2 = \frac{1}{(L_1+L_2)C}$$

$$f_r^2 = \frac{1}{(2\pi)^2(L_1+L_2)C}$$

$$f_r = \frac{1}{2\pi\sqrt{(L_1+L_2)C}}$$

$$f_r = \frac{1}{2\pi\sqrt{L_{eq}C}}$$

$$L_{eq} = L_1 + L_2$$

The frequency of oscillation may be varied by varying the capacitor "C".

Condition for oscillation :

$$|A\beta| = 1 \quad \text{and} \quad \angle A\beta = 360^\circ = 0^\circ$$

for that

$$-\omega^2 L_1 L_2 - \omega^2 L_1 L_2 h_{fe} + \frac{L_1}{C} = 0$$

$$\omega^2 (L_1 L_2)[1 + h_{fe}] - \frac{L_1}{C} = 0$$

$$\frac{L_1}{C} = \omega^2 L_1 L_2 (1 + h_{fe})$$

we know that $\omega^2 = \frac{1}{(L_1 + L_2)C}$

Substituting in above equation.

$$\frac{L_1}{C} = \frac{1}{(L_1 + L_2)C} L_1 L_2 (1 + h_{fe})$$

$$\frac{K_1}{\cancel{C}} = \frac{K_1 L_2}{(L_1 + L_2)\cancel{C}} [1 + h_{fe}]$$

$$\frac{L_1 + L_2}{L_2} = 1 + h_{fe}$$

$$\frac{L_1}{L_2} + \cancel{1} = \cancel{1} + h_{fe}$$

$$\boxed{h_{fe} = \beta = \frac{L_1}{L_2}}$$

Applications :-

Hartley oscillator is commonly used as a local oscillator in radio receivers.

Advantage :-

It is adaptability to a wide range of frequency

Easy to tune with the help of variable Capacitor.

Note :-

$$f_r = \frac{1}{2\pi\sqrt{C(L_1+L_2+2M)}}$$

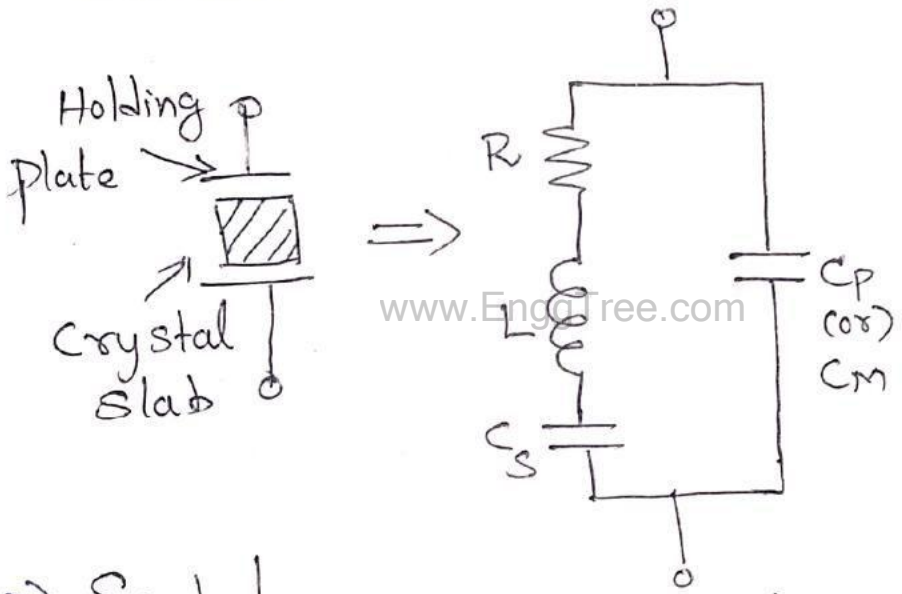
if mutual inductance is consider and it is M

Disadvantage :-

Bulk size due to Inductors.

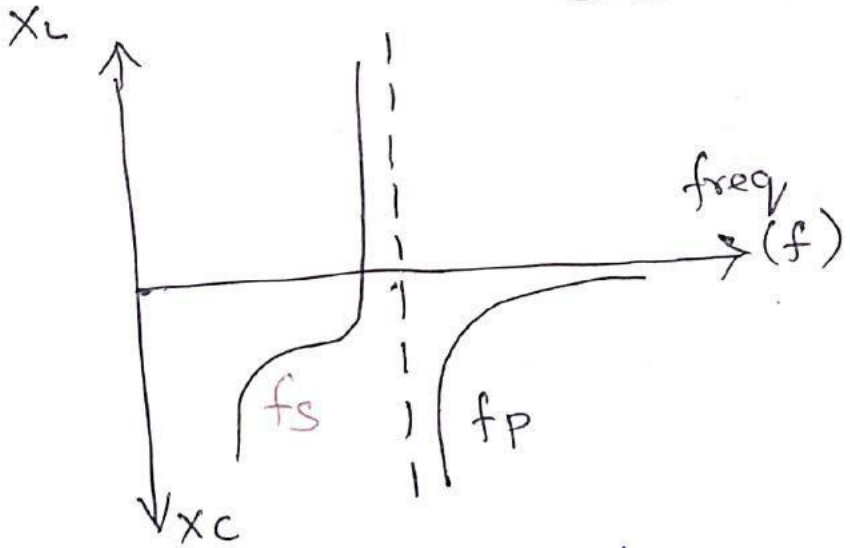
(5) Draw the Circuit of Crystal oscillator and explain its working.

The Crystal is a thin Slice of Piezo-electric material, Such as quartz, tourmaline and rochelle salt, which exhibit a Property called Piezo-electric effect.



(a) Symbol

(b) Equivalent Circuit



(c) Reactance Vs frequency.

frequency of oscillation is given by the relation

$$f_s = \frac{1}{2\pi\sqrt{L \cdot C_s}}$$

The Parallel resonant frequency (f_p) is given by

$$f_p = \frac{1}{2\pi\sqrt{L \cdot C_{eq}}}$$

where

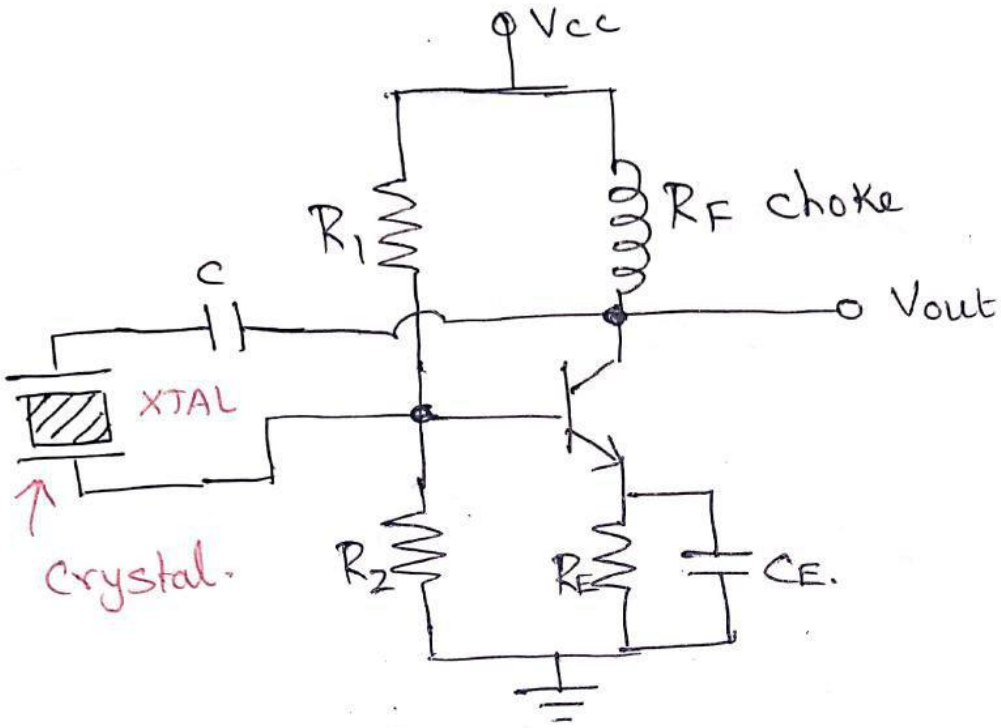
$$C_{eq} = \frac{C_s \cdot C_p}{C_s + C_p}$$

The Quality factor of a Crystal is given by

$$Q = \frac{\omega L}{R}$$

The Q-factor of a Crystal is 20,000 as compared to a maximum of about 100 for quality Lc tank Circuit.

Crystal oscillator Circuit :-



Here the Crystal is Connected as a Series element in the feedback Path from the Collector to the base.

The resistor R_1, R_2 and R_E Provide the necessary Voltage divider bias to the transistor and C_E is an emitter bypass Capacitor.

The radio frequency (RF) Choke Coil Provides d.c bias while decoupling

any a.c signal on the Power lines from affecting the output signal.

This also called Series resonant-Crystal oscillator. In this mode of Operation, the Crystal impedance is the Smallest and the amount of Positive feedback is the largest.

Crystal Provide 180° phase shift and transistor in CE mode Provide 180° phase shift. Totally 360° phase shift Positive feedback is Provide

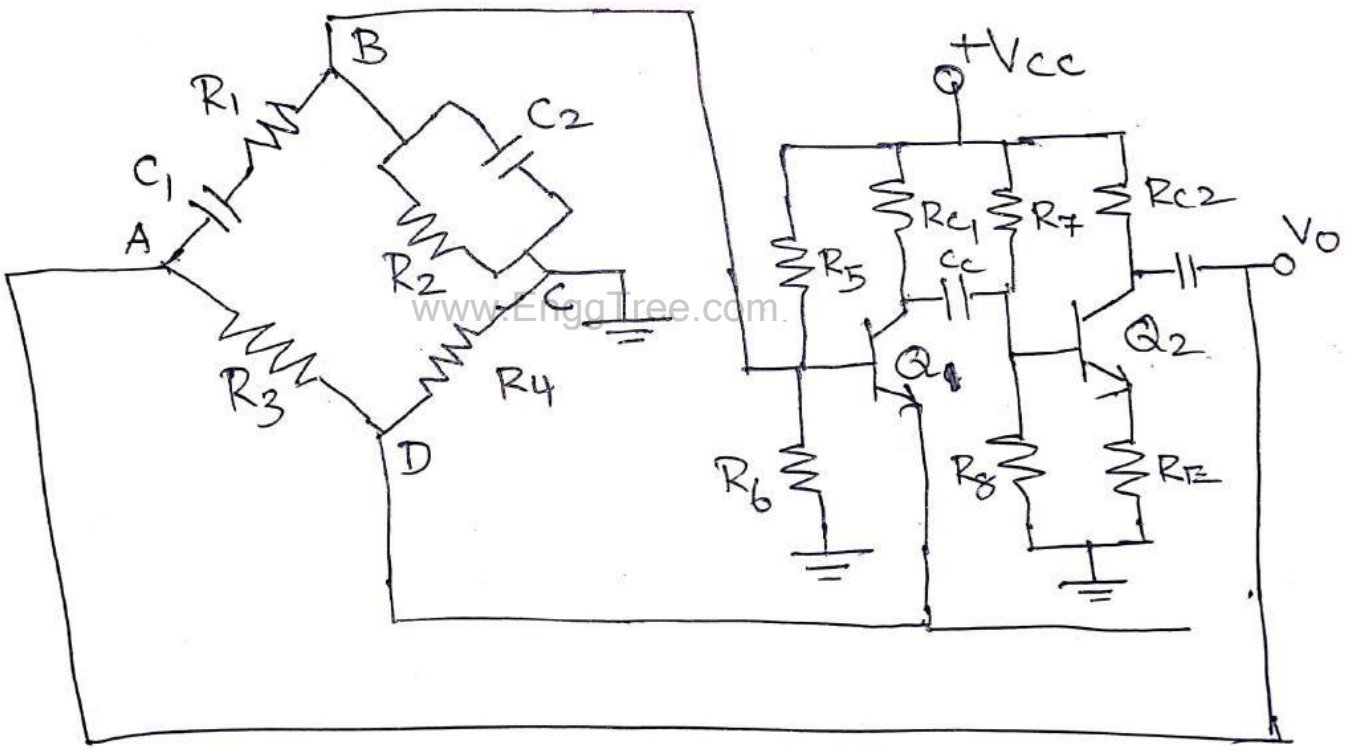
The frequency of oscillation is given by

$$f_r = \frac{1}{2\pi\sqrt{LC_s}}$$

The main advantage of the Crystal Oscillator is its Simplicity.

6. Draw the Circuit diagram of a Wien bridge oscillator and briefly explain its operation.

Wien-Bridge oscillator Circuit is shown in figure



In this Circuit, two stage common emitter transistor amplifier is used. Each stage Contributes 180° phase shift hence the total phase shift due to the amplifies stage becomes 360° (or) 0°

A balanced bridge is used as the feedback network which has no need to provide any additional phase shift.

The two arms of the bridge, namely R_1, C_1 in series and R_2, C_2 in parallel are called frequency sensitive arms.

The condition for oscillation

$$\frac{R_3}{R_4} = \frac{R_1}{R_2} + \frac{C_2}{C_1}$$

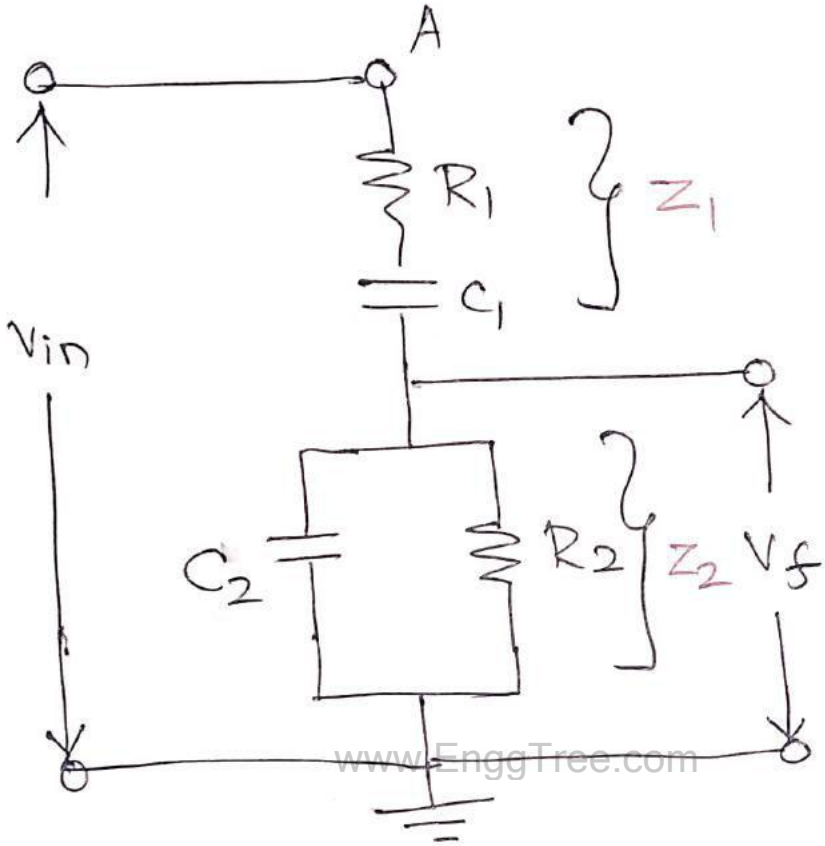
If $R_1 = R_2 = R$ and $C_1 = C_2 = C$, then

$$\frac{R_4}{R_3} = 2 \quad (ie) \quad R_3 = 2R_4$$

This ratio of R_3 to R_4 being greater than 2 will provide a sufficient, gain for the circuit to oscillate at the desired frequency

$$f = \frac{1}{2\pi RC}$$

Derivation for the frequency of oscillations



To have 360° (or) 0° phase shift of the feedback network

$$C_1 R_2 \omega (1 - \omega^2 R_1 R_2 C_1 C_2) = 0$$

$$1 - \omega^2 R_1 R_2 C_1 C_2 = 0$$

$$\omega^2 R_1 R_2 C_1 C_2 = 1$$

$$\omega^2 = \frac{1}{R_1 R_2 C_1 C_2}$$

$$\omega = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

$$f = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

if $R_1 = R_2 = R$ and $C_1 = C_2 = C$ then

$$f_r = \frac{1}{2\pi\sqrt{R^2 C^2}}$$

$$\boxed{f_r = \frac{1}{2\pi RC}}$$

and $$\beta = \frac{\omega^2 RC(3RC) + j\omega RC(1-\omega^2 R^2 C^2)}{(1-\omega^2 R^2 C^2) + \omega^2 (3RC)^2}$$

Substituting $\omega = \frac{1}{RC}$

$$\beta = \frac{3}{0 + \frac{1}{R^2 C^2} \times (3RC)^2}$$

$$\beta = \frac{3}{9}$$

$$\boxed{\beta = 1/3}$$

We know that

$$|A\beta| \geq 1$$

$$\therefore \boxed{|A| \geq 3}$$

Advantages :-

1. Good frequency stability
2. Output is Pure Sine wave
3. Highly stabilized amplitude and voltage amplification.

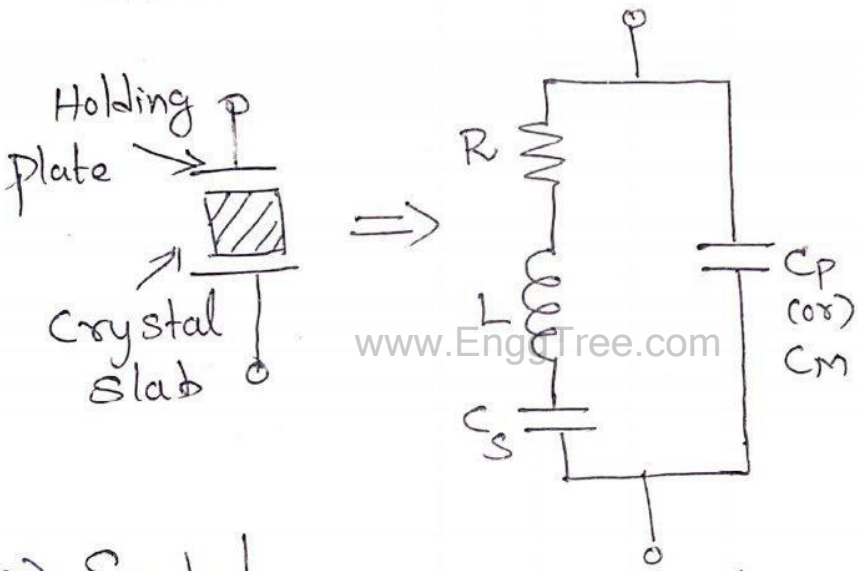
Disadvantage :-

1. Output frequency fo depends on discrete Components.

——— x ———

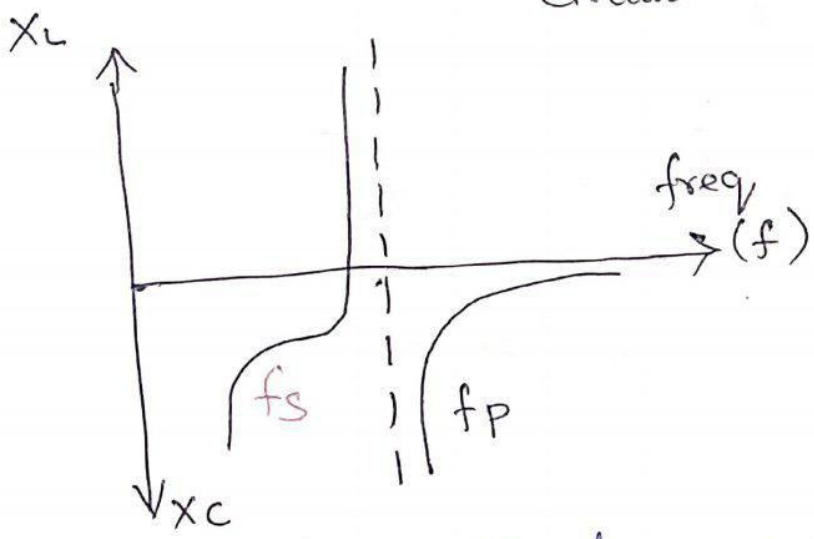
⑤ Draw the Circuit of Crystal oscillator and explain its working.

The Crystal is a thin Slice of Piezo-electric material, Such as quartz, tourmaline and rochelle salt, which exhibit a Property called Piezo-electric effect.



(a) Symbol

(b) Equivalent Circuit



(c) Reactance Vs frequency.

frequency of oscillation is given by the relation

$$f_s = \frac{1}{2\pi\sqrt{L \cdot C_s}}$$

The Parallel resonant frequency (f_p) is given by

$$f_p = \frac{1}{2\pi\sqrt{L \cdot C_{eq}}}$$

where

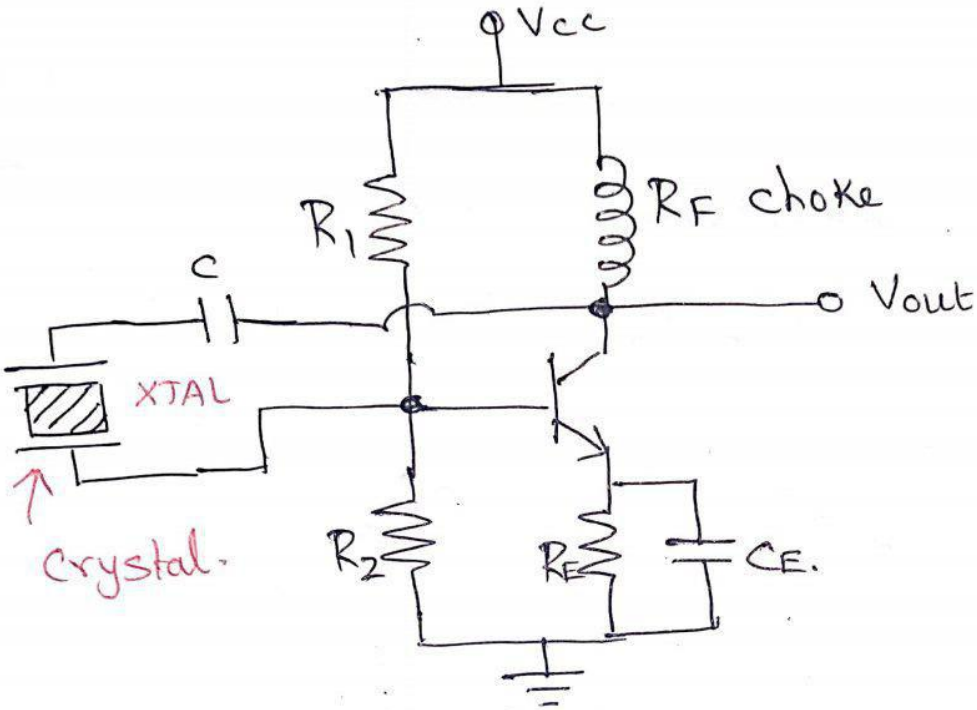
$$C_{eq} = \frac{C_s \cdot C_p}{C_s + C_p}$$

The Quality factor of a Crystal is given by

$$Q = \frac{\omega L}{R}$$

The Q-factor of a Crystal is 20,000 as compared to a maximum of about 100 for quality Lc tank Circuit.

Crystal oscillator Circuit :-



Here the Crystal is Connected as a Series element in the feedback Path from the Collector to the base.

The resistor R_1, R_2 and R_E Provide the necessary Voltage divider bias to the transistor and C_E is an emitter bypass Capacitor.

The radio frequency (RF) choke Coil Provides d.c bias while decoupling

any a.c signal on the Power lines from affecting the output signal.

This also called Series resonant-Crystal oscillator. In this mode of Operation, the Crystal impedance is the Smallest and the amount of Positive feedback is the largest.

Crystal Provide 180° phase shift and transistor in CE mode Provide 180° phase shift. Totally 360° phase Shift Positive feedback is Provide

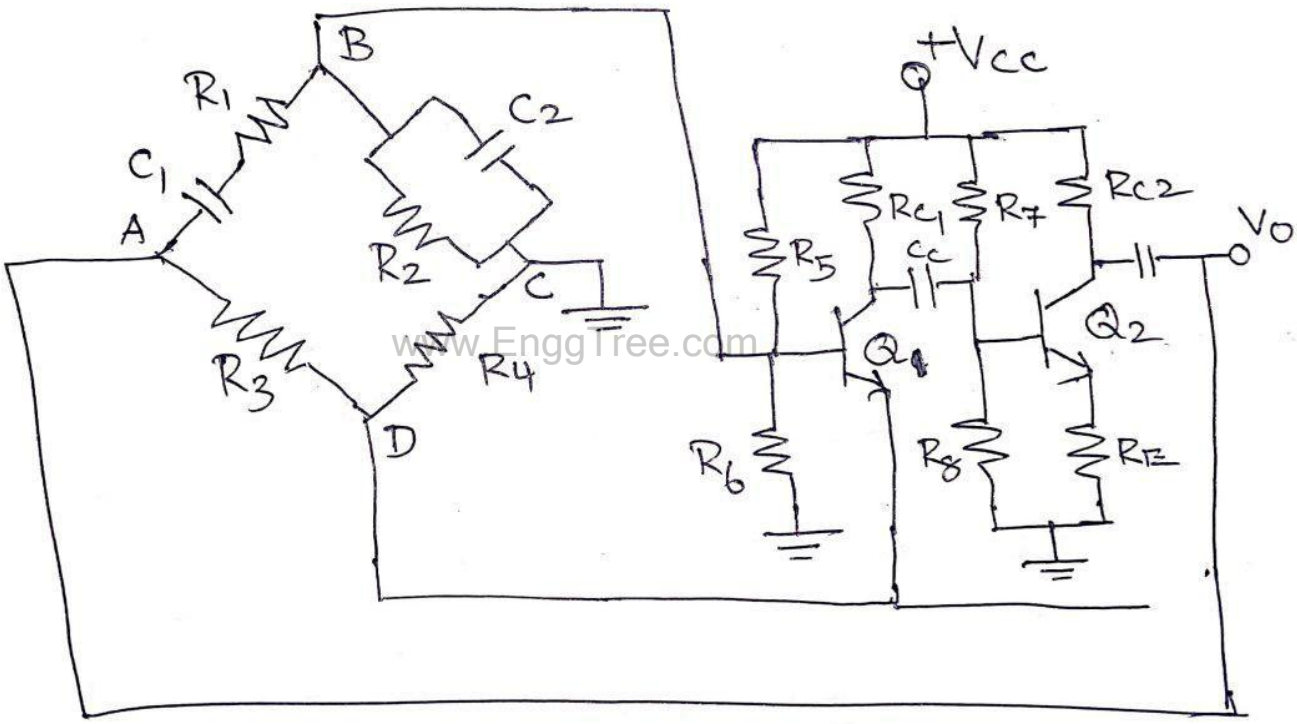
The frequency of oscillation is given by

$$f_r = \frac{1}{2\pi\sqrt{LC_s}}$$

The main advantage of the Crystal Oscillator is its Simplicity.

6. Draw the Circuit diagram of a Wien bridge oscillator and briefly explain its operation.

Wien-Bridge oscillator Circuit is shown in figure



In this Circuit, two stage common emitter transistor amplifier is used. Each stage Contributes 180° phase shift hence the total phase shift due to the amplifier stage becomes 360° (or) 0°

A balanced bridge is used as the feedback network which has no need to provide any additional phase shift.

The two arms of the bridge, namely R_1, C_1 in series and R_2, C_2 in parallel are called frequency sensitive arms.

The condition for oscillation

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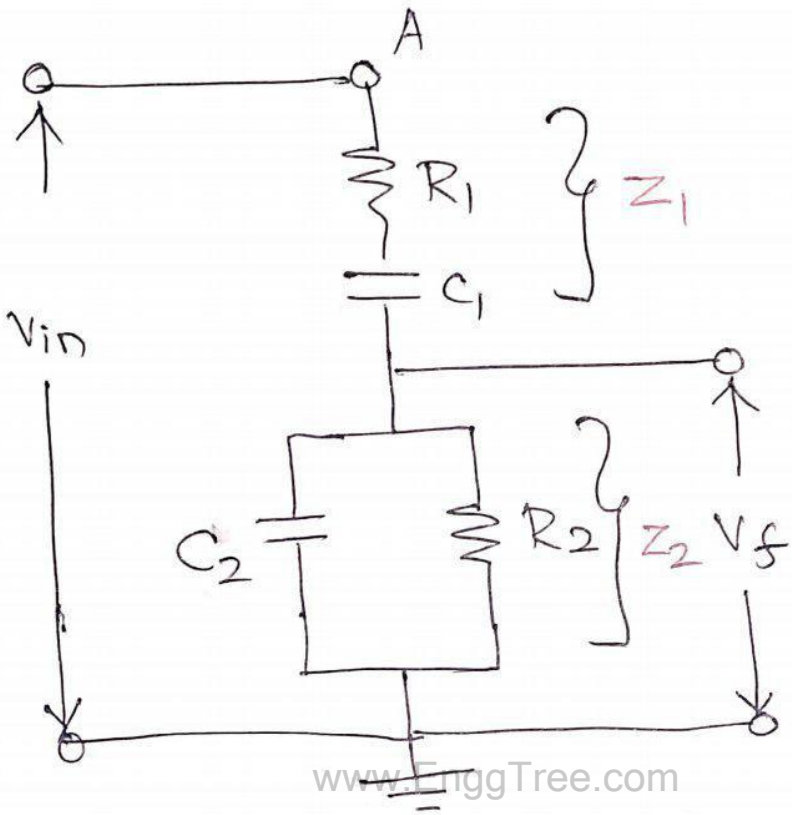
$$f = \frac{1}{2\pi RC}$$

Derivation for the frequency of oscillations



To have 360° (or) 0° phase shift of the feedback network

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$$1 - \omega^2 R_1 R_2 C_1 C_2 = 0$$

$$\omega^2 R_1 R_2 C_1 C_2 = 1$$

$$\omega^2 = \frac{1}{R_1 R_2 C_1 C_2}$$

$$\omega = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

$$f = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

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Substituting $\omega = \frac{1}{RC}$

$$\beta = \frac{3}{0 + \frac{1}{R^2 C^2} \times (3RC)^2}$$

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1. Good frequency stability
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Disadvantage :-

1. Output frequency fo depends on discrete Components.

——— x ———

unit - 5

POWER AMPLIFIERS

AND

DC-DC CONVERTERS

Power amplifiers – Class A, Class B, Class C – Power MOSFET, Temperture Effect – Class AB Power amplifier using MOSFET – DC/DC Convertors – Buck, Boost, Buck-Boost & analysis and Design.

Unit V: Power Amplifier and DC-DC Converter

PART – A

1. What is power amplifier?

Power amplifier amplifies a weak signal until sufficient power to operate output device such as loudspeaker.

2. Compare small signal and large signal amplifier?

S.No	Small Signal Amp	Large Signal Amp
1.	Also known as Voltage Amplifiers	Also known as Power Amplifiers
2.	They convert a small input voltage into a larger output voltage	They amplifies the power of input signal and deliver power to the load.
3.	They amplify very small signal voltage levels of only a few μV from sensors or audio signals	They amplify large input voltage signals or switch heavy load currents.

3. What are the features of power amplifier?

i. Impedance matching to deliver maximum power to the load.

ii. Need power transistors to withstand large voltages and current.

iii. Power amplifiers are bulk.

iv. Harmonic distortions occur due to non-linear character of transistors.

4. What is class A power amplifier?

A power amplifier is known as class A amplifier if the transistor used in the circuit conducts for full cycle of the input signal. The operating point is selected approx. at the center so that the output current follows the input signal.

5. Write the merits and demerits of class A power amplifier.

Advantages

i. Simple construction

ii. Distortionless output voltage

Disadvantages

i. Very low efficiency (25%)

ii. Large power dissipation in the transistors

iii. High output impedance

6. What is meant by cross over distortion?

In Push Pull operation of Class B amplifiers, the output waveform is not a perfect sinusoidal waveform. The output waveform will be as shown in Figure.

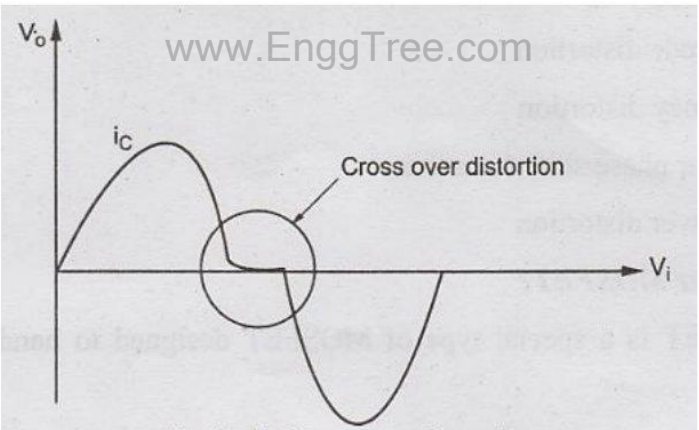


Fig. 5.44. Cross over distortion

The drive signal applied to class B transistor must reach a certain minimum level before its collector current is properly in active region

7. What is power MOSFET?

Power MOSFET is a special type of MOSFET designed to handle high power levels.

Power MOSFET are commonly used power devices due to the following advantages.

i. Low gate drive power

ii. Fast switching speed

iii. Parallel operation

8. Compare Class A, Class B, Class AB power amplifiers.

Class / Parameters	A	B	C	AB
Conduction angle	360°	180°	less than 180°	180° to 360°
Q-point	Centre of load line	Exactly on the X-axis	Below the X-axis	In between X-axis and centre load line
Overall efficiency	Poor 25 to 30%	Better 70-80%	Higher > 80%	50 to 70%
Signal Efficiency	None if correctly biased	At the X-axis cross-over distortion	Distortion occurs	less amount of distortion

9. Compare power MOSFET and power BJT.

i. MOSFET provides a very good isolation between the gate and other two terminals compared to BJT

ii. MOSFET can handle more power compared to BJT

iii. MOSFET has very low power less and a high speed

iv. Voltage signals can easily operate a MOSFET, hence it is used in many digital circuits for switching applications ex: motor control circuits.

v. Power MOSFET do not suffer from second breakdown compared to BJT.

vi. Power MOSFET do not require large dc large- drive current as that in power BJTs.

vii. Higher speed of operation than power BJT,

10. What is DC to DC converter.

The DC to DC converters convert one level of DC voltage to another level. It is also known as DC chopper.

11. Define Buck converter?

Buck converter is also known as step down converter and produces a lower output voltage than input voltage. The average output voltage is less than the input voltage.

12. Write the applications of Buck converter.

i. Used to drive high current loads, used in PCs, mother boards

ii. Battery chargers

iii. Solar chargers

13. Define Boost converter.

The boost regulator produces an output voltage greater than input voltage.

14. What is Buck-Boost Converter?

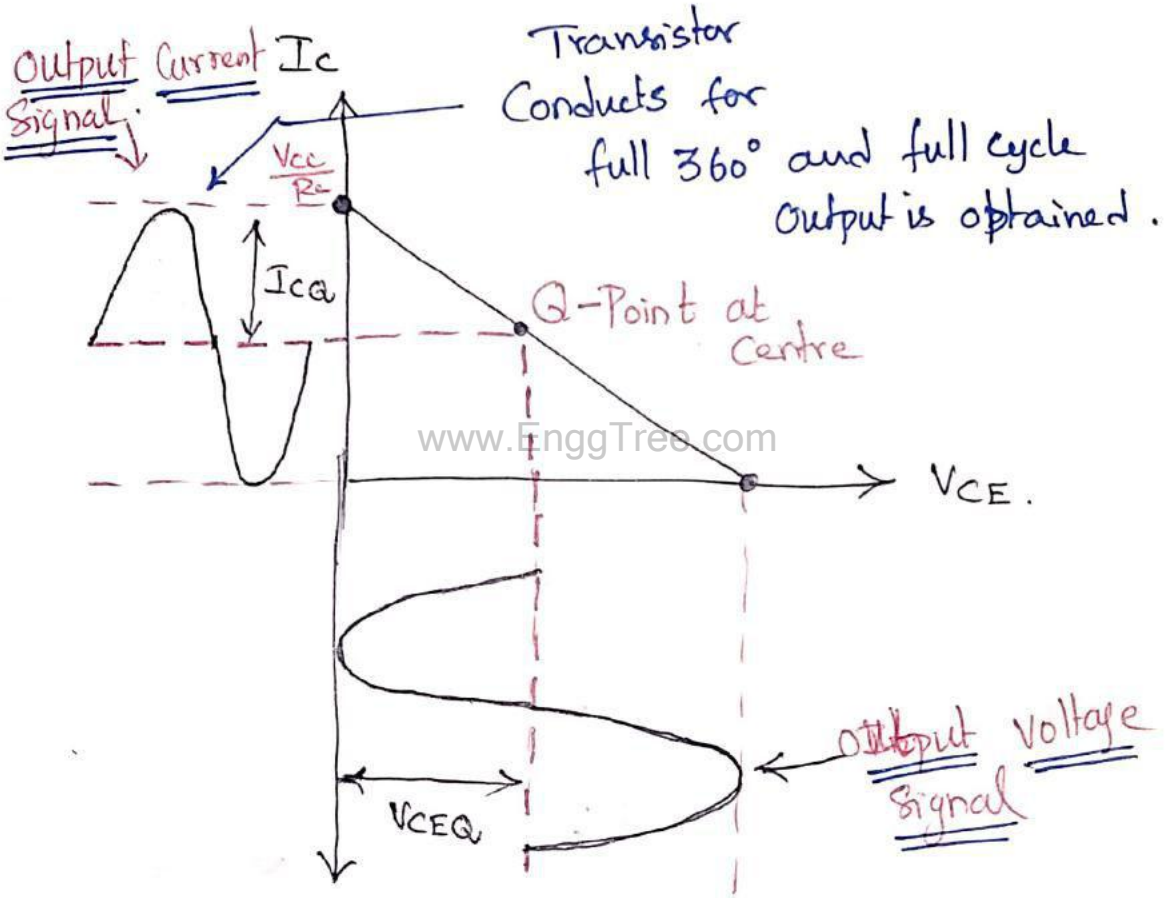
A Buck-Boost Regulator produces an output voltage which may be less than noitsioat boog or greater than the input voltage.

The polarity of output voltage is opposite that of input voltage. So, this regulator is also known as inverting or flyback regulator.

15. Differentiate Buck and Boost Converter.

	Buck Converter	Boost Converter
1.	Buck converter steps down the input voltage	Boost converter steps up the input voltage
2.	It is used to change the battery	It is used to match the load voltage from the low voltage input

Therefore, the Ac input signal is perfectly centered between the amplifiers upper and lower signal limits. The transistor conducts for entire 360° [full cycle]. As shown in the figure below.



In biasing, Q-Point is fixed by Vcc & R_B

$$I_c = \beta I_B = \beta \frac{(V_{cc} - V_{BE})}{R_B}$$

and

$$V_{CE} = V_{cc} - I_c R_c$$

The point is set halfway between 0 and $\frac{V_{cc}}{R_c}$ and ~~the~~ The input power is given by

$$P_{in(dc)} = V_{cc} I_{CQ}.$$

$$i_{CQ} = \left[\frac{\frac{V_{cc}}{R_c}}{2}\right] = \frac{V_{cc}}{2R_c}$$

$$V_{CEQ} = \frac{V_{cc}}{2}$$

} Middle of DC load line.

Power delivered to the load by the transister is

$$P_{o(ac)} = I_{c(rms)} \cdot V_{CE(rms)}$$

$$= \frac{I_{CQ}}{\sqrt{2}} \cdot \frac{V_{CEQ}}{\sqrt{2}}$$

$$= \frac{\left[\frac{V_{cc}}{2R_c}\right]}{\sqrt{2}} \cdot \frac{\left[\frac{V_{cc}}{2}\right]}{\sqrt{2}}$$

$$= \frac{\frac{V_{cc}^2}{4R_c}}{2}$$

$$\boxed{P_{o(ac)} = \frac{V_{cc}^2}{8R_c}}$$

Maximum efficiency $\eta_{(max)}$

$$\eta_{(max)} = \frac{P_{o(ac)}}{P_{in(dc)}} = \frac{\frac{V_{cc}^2}{8R_c}}{\frac{V_{cc}^2}{2R_c}} \times 100\%$$

$$\eta_{(max)} = \frac{1}{4} \times 100\%$$

$$\boxed{\eta_{(max)} = 25\%}$$

Since the transistor is operated in active region middle, the collector current and voltage are high which produce large power which is dissipated as heat. Hence, the efficiency of class A power amplifier is low (25%)

Advantages :-

* Simple Construction.
* Distortionless output voltage

* Cheaper and less bulky

Disadvantages :-

* Very low efficiency (25%)
* Lower Power dissipation in the transistors
* It required large heat sink.
* High output impedance.

Applications :-

* High-fidelity Audio Systems.
* Instrumentation amplifier.
* Radio frequency transmitters.

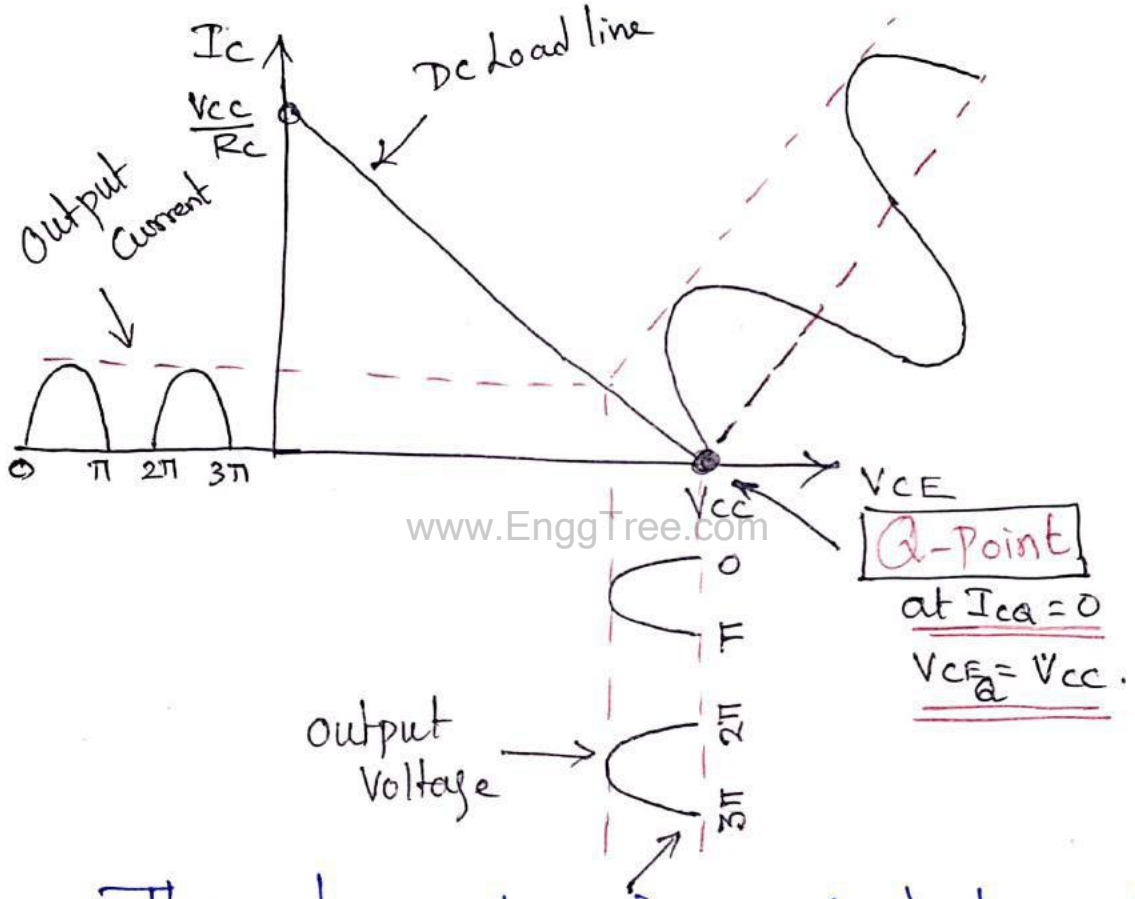
---

2. Draw the Circuit of Push pull class B Amplifier and Explain its opeeation.

The main drawback of class A amplifier is that all of the supply Power is dissipated in the transistor

The output Power is obtained for one half cycle of input only [180°].

The Collector Current flow for 180° only. The Q-Point is fixed in cut off region at $I_B = 0$, $V_{CE} = V_{cc}$. as shown in figure.

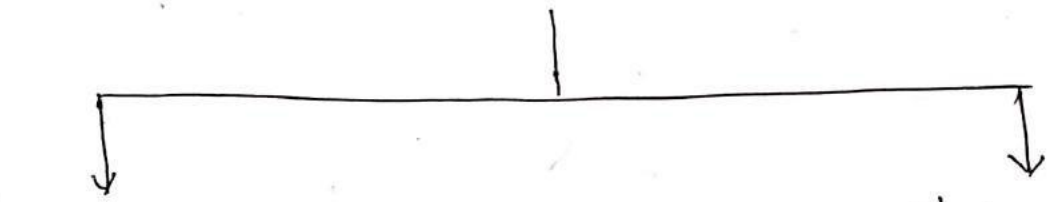


The transistor is in Conduction State during Positive half cycle of the Signal and in Cut off State during negative half of the Signal. Therefore, the output is obtain only for 180°

Since the transistor Conducts for only half cycle of the input, the Power dissipation

in Class B amplifier is very less. Hence efficiency is increased.

Types of Class B Amplifier.



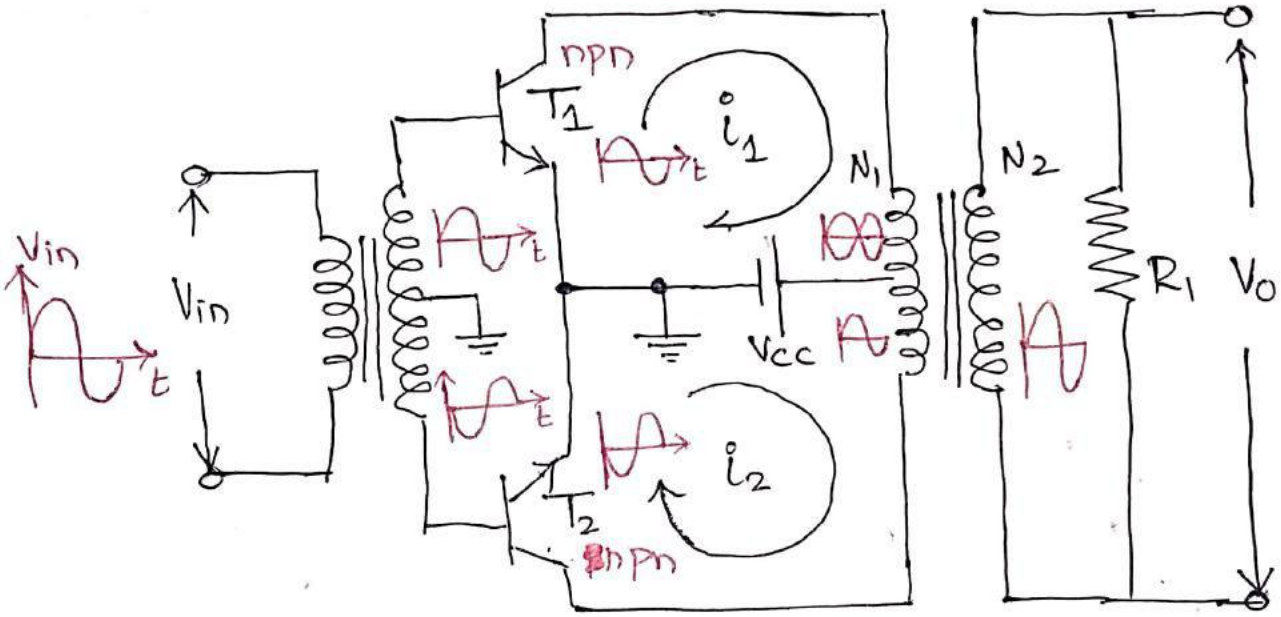
Class B Push Pull Amplifier [both transistor are same type]

Class B Complementary Symmetry Amplifier. [one of the transistor is npn and another is pnp transistor]

Class B Push-Pull Amplifier :-

The push-pull amplifier uses two centre tapped transformers. For getting full input signal we use push pull circuit.

In push-pull amplifiers, two transformers are used, one at the input and the other at the load side. Both are centre tapped transformers.



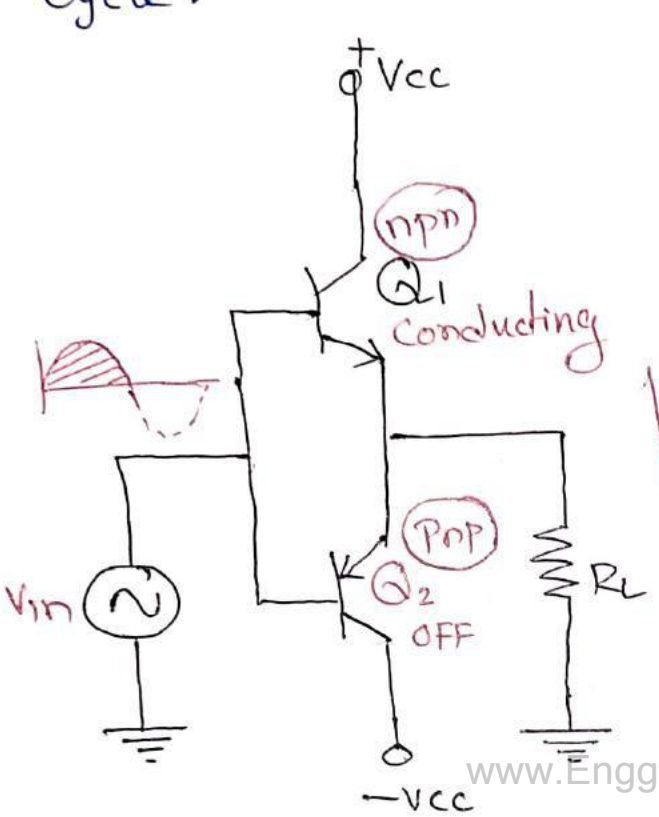
The input transformer converts the input signal to two out-of-phase signals for the two npn transistors.

The output transformer combines the signals by permitting current in both directions, even though one transistor is always cut off.

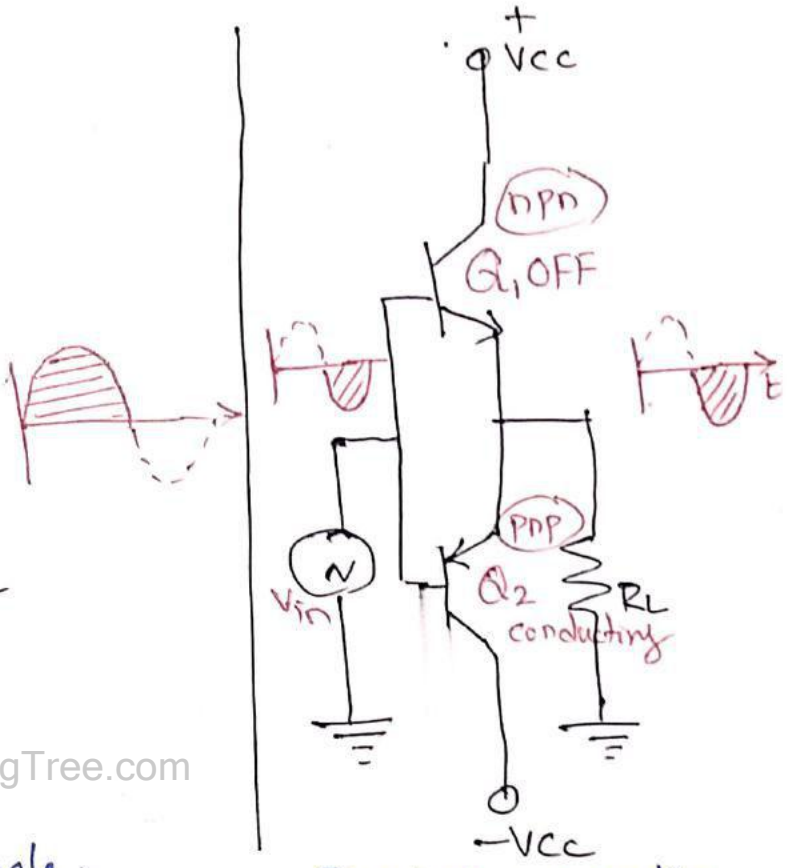
Complementary Symmetry Push Pull Class-B amplifier.

It is most popular types of Push-pull Class B amplifiers using two emitter followers and This is a Complementary amplifier because one emitter-follower uses an

npn transistor and the other a pnp, which Conduct on opposite alternations of the input cycle.



During a positive cycle.



During a negative half cycle.

When $V_{in} = 0$, both transistors Q_1 and Q_2 are OFF,

For Positive half input cycle Q_1 goes ON and Conduct

For negative half input cycle Q_2 goes ON and Conduct

Output power (Maximum) :-

$$P_{out} = I_{CQ(rms)} V_{CEQ(rms)}$$

$$= \frac{I_{CQ}}{\sqrt{2}} \times \frac{V_{CEQ}}{\sqrt{2}}$$

$$= \frac{I_{CQ} V_{CEQ}}{2}$$

$$I_{CQ} = V_{CEQ} = V_{CC}$$

$$I_{CQ(max)} = \frac{I_{C(max)}}{2}$$

DC Input Power :-

$$P_{dc} = I_C V_{CC}$$

$$= \frac{I_{cmax}}{\pi} V_{CC}$$

$$I_C = \frac{I_{cmax}}{\pi}$$

$\pi \rightarrow 180^\circ$

Efficiency $\eta_{(max)}$:-

$$\eta_{(max)} = \frac{P_{ac}}{P_{dc}} = \frac{\frac{I_{cmax} V_{CC}}{4}}{\frac{I_{cmax} V_{CC}}{\pi}}$$

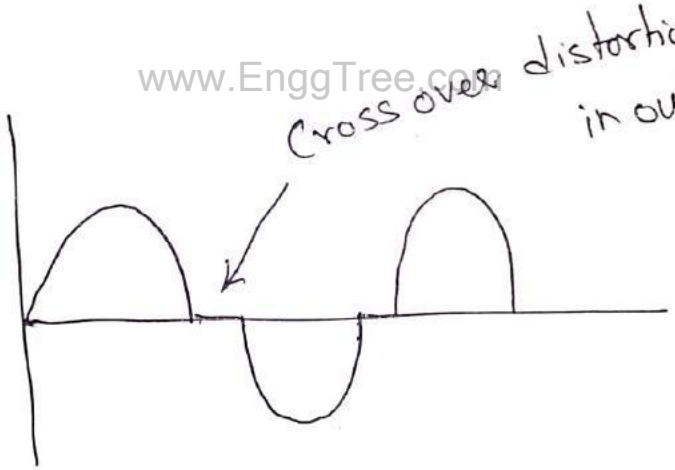
$$= \frac{\pi}{4} = \boxed{\eta_{max} = 78.54\%}$$

Advantages :-

* Impedance with load is Possible
* Second harmonic is cancelled automatically
* Zero Power dissipation
* Higher efficiency than class A Amplifiers

Disadvantages :-

* Cross over distortion is Present in the output waveform.

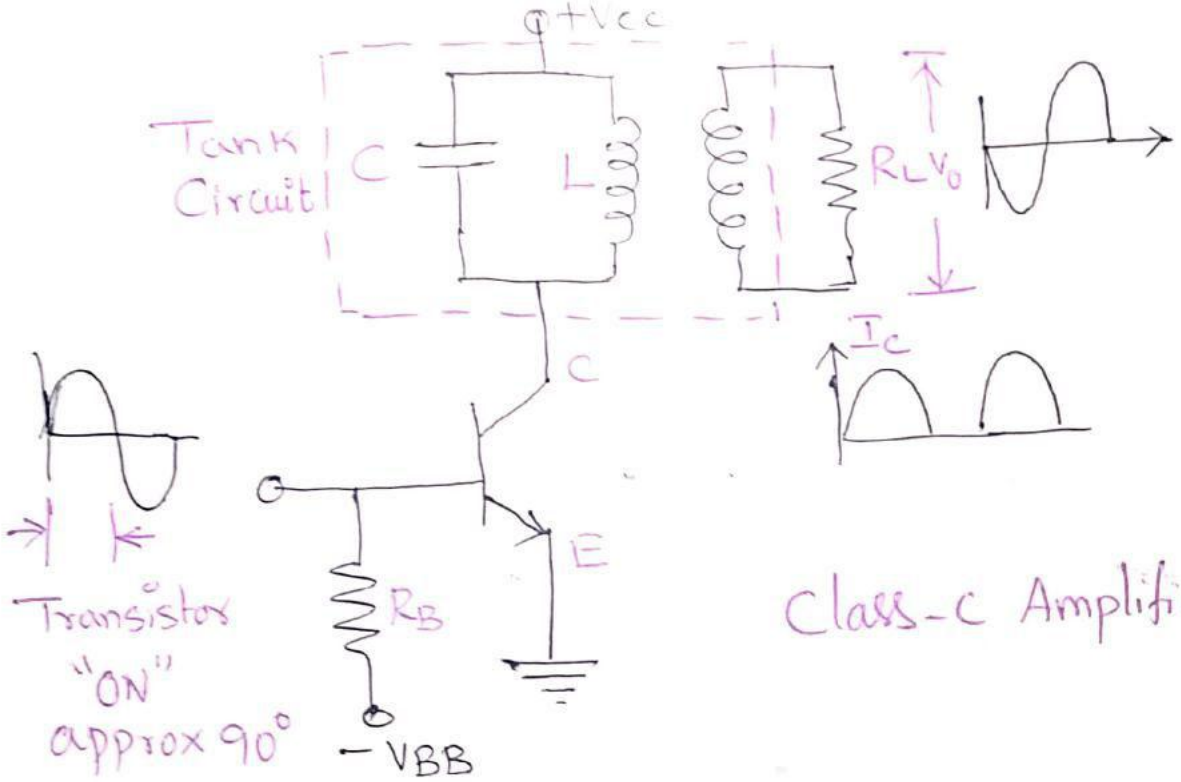


Since the transistor is biased at Cut off region, the wave form is distorted near Zero Crossing.

3. Explain the operation of class c amplifier with neat diagram.

Class c amplifier are biased deep into Cut off. The negative Voltage at the base terminal reverse-biases the base-emitter junction of the transistor such that it will not conduct until the input signal overcomes this reverse bias.

The figure shows the class-c Power amplifier



Class-C Amplifier

The negative voltage at the base terminal reverse-biases the base-emitter junction of the transistor such that it will not conduct until the input signal overcomes this reverse bias.

This occurs only for a small part of positive half cycle of input signal. I_C is in the form of pulses. So distortion occurs in class-C amplifiers.

Class-C amplifiers are suitable for audio amplifier and used at radio frequencies.

A tank circuit is connected in the collector circuit of class C amplifiers. It restores the sine waveform of the input signal at the output.

A parallel LC oscillating Circuit is used as a tank Circuit which is excited by collector Current pulse and sets the Circuit into self oscillations.

The energy is transferred back and forth between Capacitor and inductor, thus Producing Sine wave form.

The frequency of oscillation of the tank Circuit is given by

$$f = \frac{1}{2\pi\sqrt{LC}}$$

Practical class c amplifiers have efficiency as high as 85 %.

Advantages :-

* Less physical size
* Used in RF amplifier
* High efficiency (> 95%)
* Low power loss in transistor.

Disadvantages :-

* RF interference occurs
* Ideal inductor should be selected
* Not suitable for audio applications

Applications

* Tuned amplifiers.
* RF amplifiers
* Oscillators
* Booster amplifier
* Higher frequency repeaters.

---

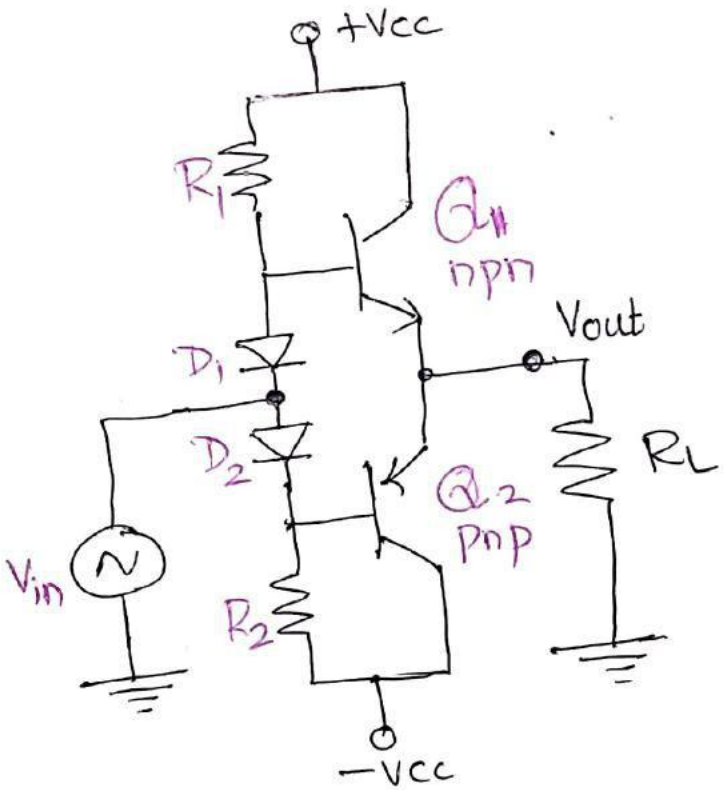
4. Explain the operation of class AB amplifiers and derive its efficiency.

To overcome the Cross over distortion in Class-B amplifiers, Class-AB amplifiers used.

The output signal is obtained for more than 180° but less than 360° of the ac input signal.

The Q-Point is adjusted to be slightly above the cut off region.

To overcome crossover distortion, the biasing is adjusted to just overcome the V_{BE} of the transistors.

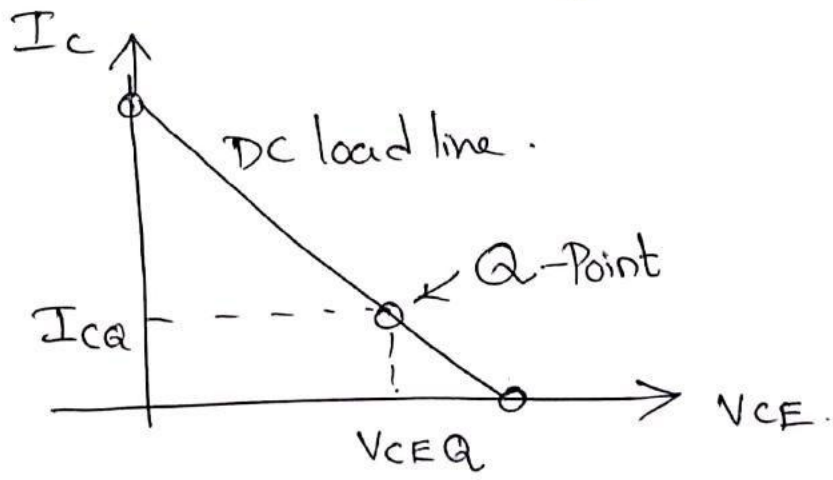


when the diode characteristics of D_1 and D_2 are closely matched to the characteristics of the transistor BE. [Base-Emitter] Junctions,

[ie the Current in the diodes and the Current in the transistors are the Same] so that Cross over distortion is overcomed.

The diode Current will be the Same as I_{CQ}

$$I_{CQ} = \frac{V_{CC} - 0.7}{R_1}$$



Advantages :-

* No Cross over distortion
* Bulky Coupling transformers are not required.

Disadvantages :-

* Less efficiency compared to class B Amp.
* There will be some dc components in the output as the load is directly coupled
* Capacitive Coupling can eliminated dc components - but it is not practical for heavy load.

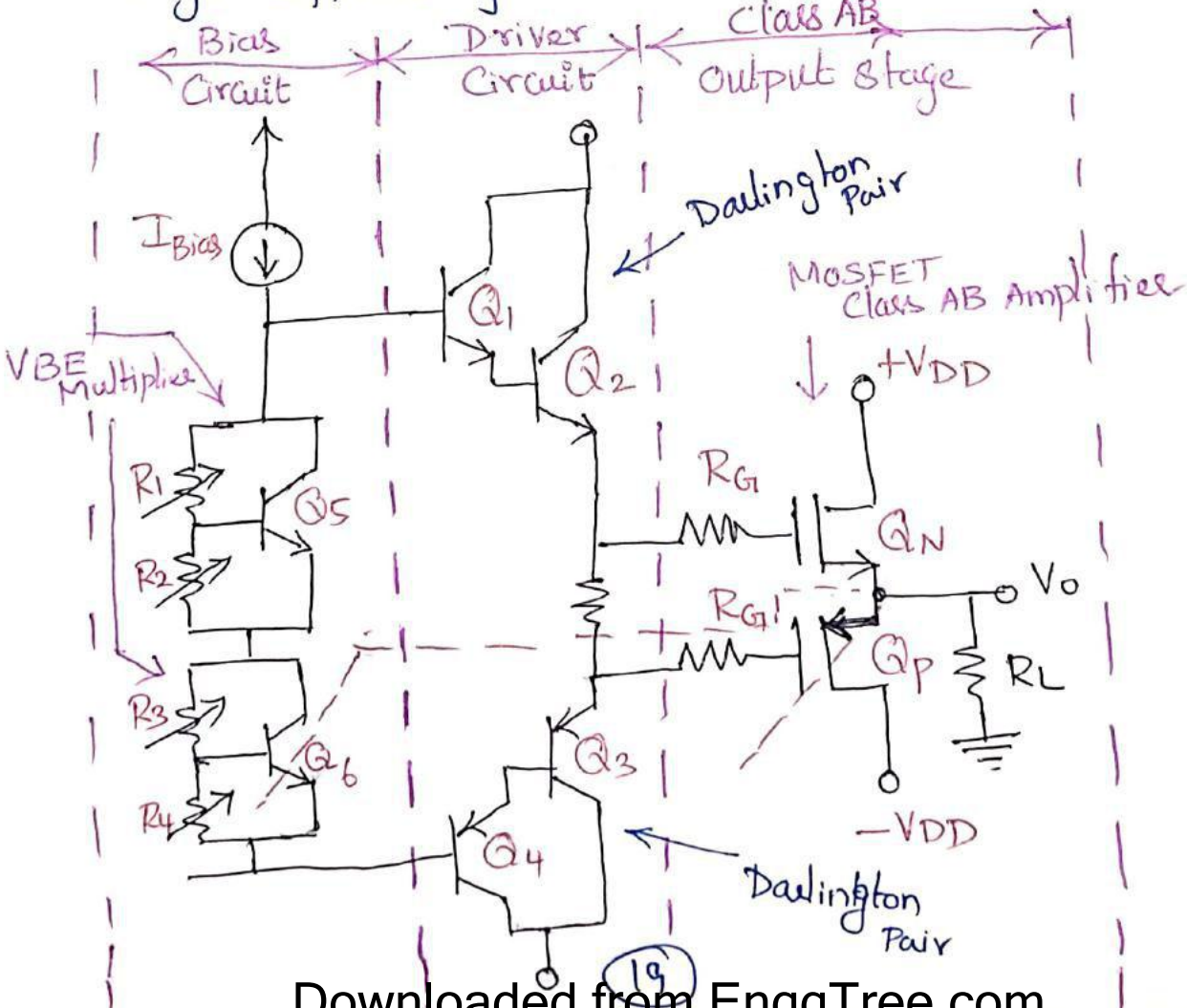
Efficiency :-

The efficiency of class AB power amplifier is around 70 %.

5. With neat diagram explain the operation of MOSFET class AB amplifier.

Class -AB Power amplifier using MOSFET

Class AB amplifier can be designed using MOSFET to generate an output Power of 100 Watts. This amplifier has high efficiency and less harmonics.



This Circuit Consists of drivers, bias Circuit and power amplifieation using MOSFET with class AB amplifier MOSFET is Preferred over BJT because of its simple drive circuit, less Susceptibility to thermal stability and high input impedance.

Bias Circuit :-

It Consist of two V_{BE} multipliers formed by transistor Q_5 and Q_6

Q_6 is Connected in direct thermal Contact with output MOSFET transistor Q_p on their Common heat sink.

Driver Circuit :-

Complementary Darlington emitter followers are formed by Q_1, Q_2, Q_3 and Q_4 It provides the low output resistance necessary for driving the output MOSFET at high Speeds.

V_{GG} is given by

$$V_{GG} = \left[1 + \frac{R_3}{R_4}\right] V_{BE6} + \left[1 + \frac{R_1}{R_2}\right] V_{BE5} - 4V_{BE}.$$

V_{BE} is thermally coupled to the output devices, d.w.r.t T above equation became

So, $$\frac{\partial V_{GG}}{\partial T} = \left[1 + \frac{R_3}{R_4}\right] \frac{\partial V_{BE6}}{\partial T}$$

we need to adjust the value of $\frac{R_3}{R_4}$ Such that.

$$\frac{\partial V_{GG}}{\partial T} = \frac{\partial \left[V_{tN} + |V_{tp}|\right]}{\partial T}$$

The class AB amplifier using MOSFET is known as Hi-Fi amplifier circuit and is suitable for following application.

* Key Board Amplifiers
* Guitar amplifiers
* Subwoofer amplifiers

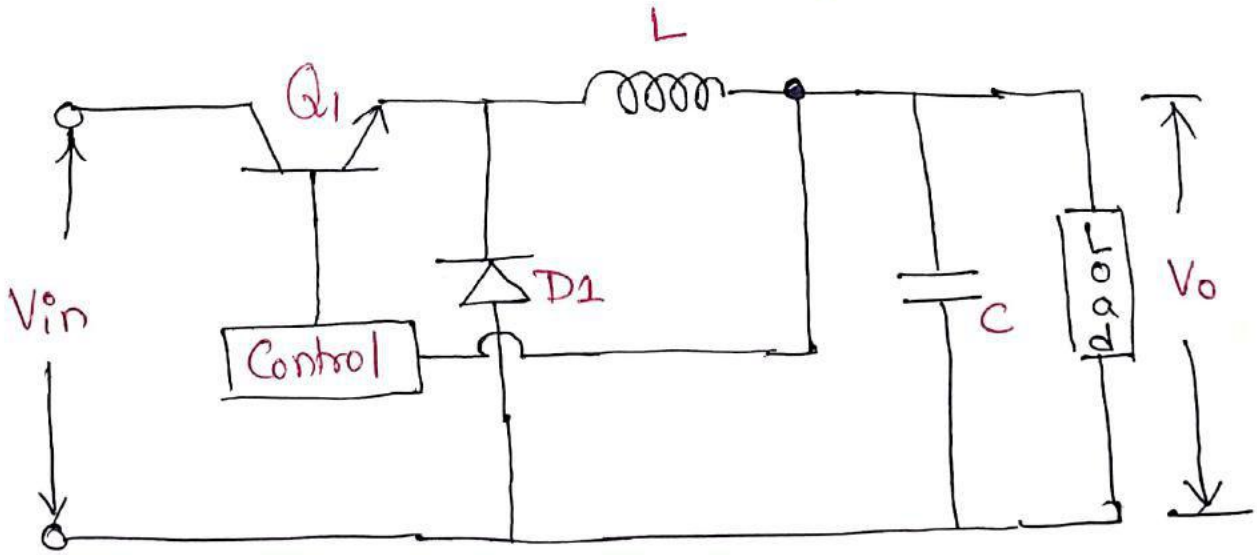
6. Explain the operation of Buck Converter in detail.

Buck Converter / Regulator :-

Buck Converter is also known as Step down Converter and produces a lower output voltage than input voltage.

The average output voltage is less than the input voltage.

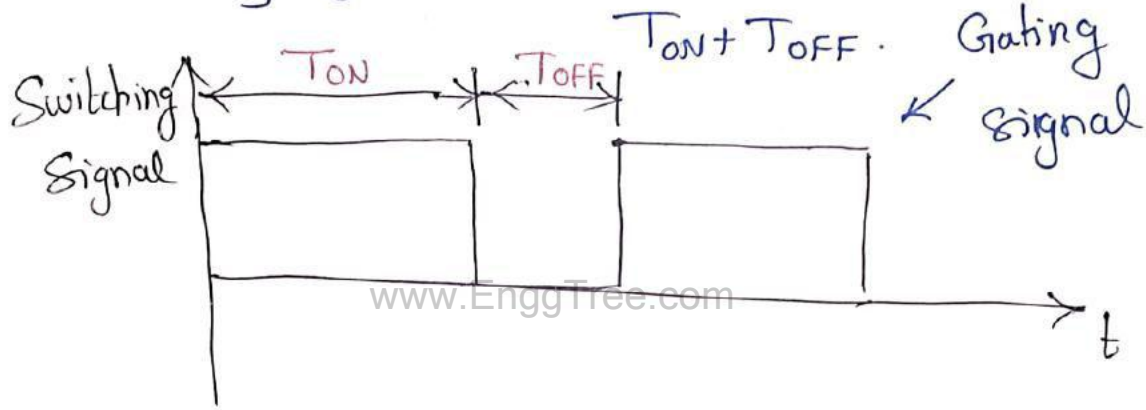
Figure shows the circuit diagram of a buck regulator using Power BJT.



Buck Converter.

i) The Switch is implemented by using BJT, MOSFET (or) IGBT [insulated Gate Bipolar Transistor]. The duty cycle K Varies from 0 to 1

$$\text{Duty cycle } K = \frac{T_{ON}}{T_{ON} + T_{OFF}}$$



ii) The output voltage has harmonics which requires Dc filter for Smoothing out ripples.

iii) Gating Signal is obtained by Comparing required Dc voltage and output voltage at load (output). Difference between required Dc voltage and o/p voltage used to generate Gating Signal with help of Control Block.

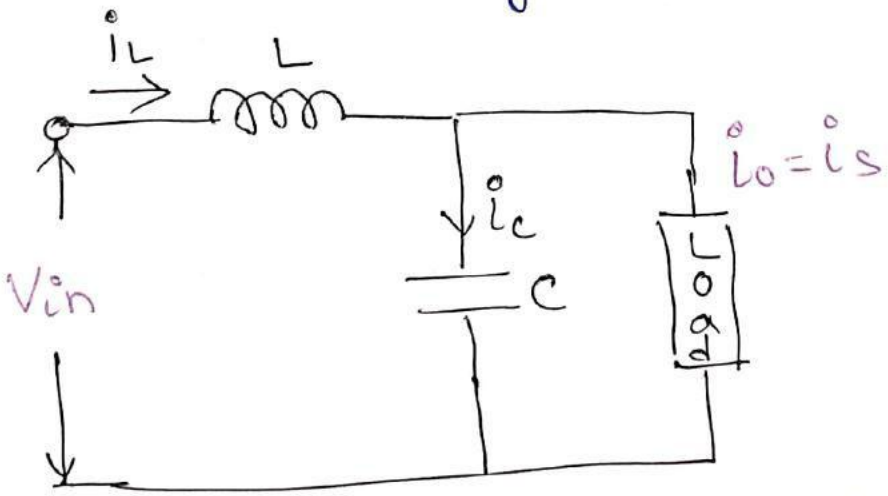
iv) The Control Circuit Produce Gating Signal and Q_1 transistor ON and OFF based on Gating Signal.

The indicator Current forward biases the diode D_1 and D_1 Conducts for the remaining Switching Period. This diode is known as Free wheeling Diode.

Operation :-

The Circuit operates in 2 modes.

Mode 1 :- During Q_1 is "ON"

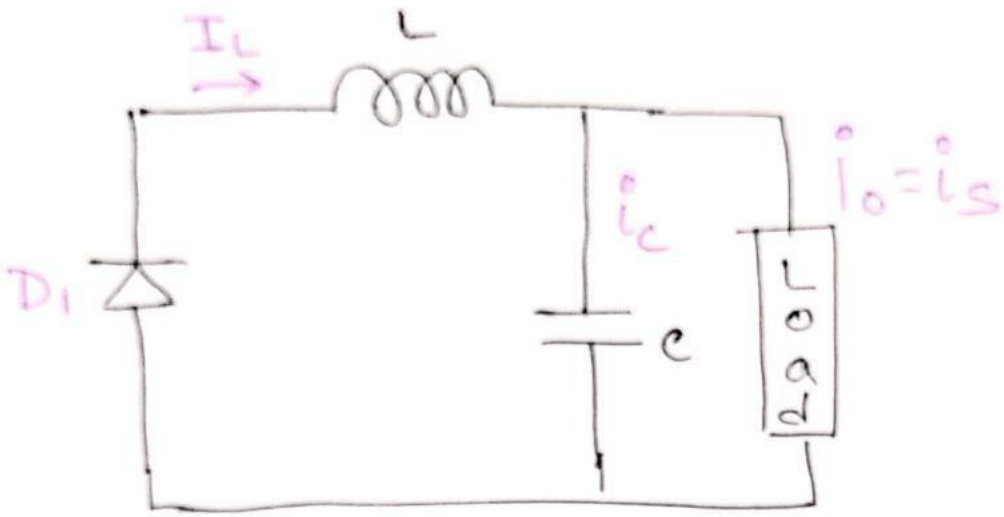


At $t=0$, Q_1 is Switched "ON"

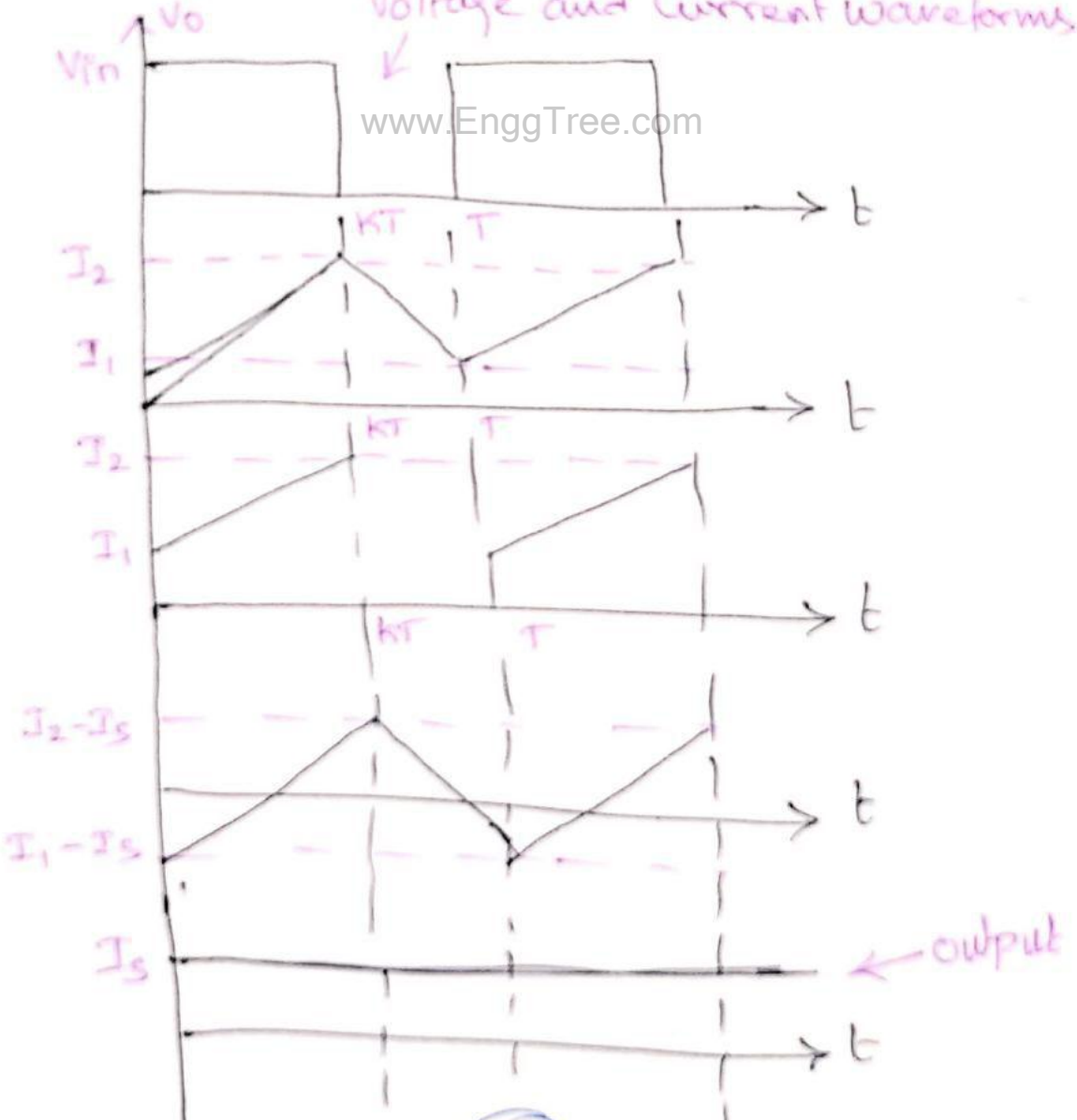
i) The input Current flows through filter (L and C) inductor and Capacitor and Load resistor.

Mode 2 :- During Q_1 is "OFF"

At $t = t_1$, Q_1 is switched "OFF"



Voltage and Current waveforms



Assume that inductor current rises linearly from I_1 to I_2 in time t_1,

$$V_{in} - V_a = L \frac{I_2 - I_1}{t_1} = L \frac{\Delta I}{t_1}$$

$$t_1 (V_{in} - V_a) = L \Delta I \quad \text{——— (1)}$$

$$t_1 = \frac{L \Delta I}{V_{in} - V_a} \quad \text{——— (2)}$$

$$\Delta I = \frac{t_1 (V_{in} - V_a)}{L} \quad \text{——— (3)}$$

at time t_2, inductor current falls linearly from I_2 to I_1,

$$V_a = L \frac{\Delta I}{t_2} \quad \text{——— (4)}$$

$$t_2 = L \frac{\Delta I}{V_a} \quad \text{——— (5)}$$

$$\Delta I = \frac{t_2 V_a}{L} \quad \text{——— (6)}$$

Equate equation (3) and (6)

$$\Delta I = \frac{t_1 (V_{in} - V_a)}{L} = \frac{t_2 V_a}{L}$$

$$t_1 (V_{in} - V_a) = t_2 V_a$$

$t_1 = kT$ and $t_2 = (1-k)T$

$$kT(V_{in} - V_a) = (1-k)T\, V_a$$

$$kTV_{in} - kTV_a = TV_a - kTV_a$$

$$kTV_{in} = TV_a$$

$$V_a = kV_{in}$$

By choose duty cycle k, we Can get step down voltage output at load V_a.

Advantages :-

* Requires only one transistor
* Simple Construction.

* High efficiency
* Less expensive

Disadvantages :-

* $\frac{di}{dt}$ of the load current is limited by inductor
* Smoothing input filter is required.
* Need Protection Circuit to avoid short circuits
* Input current and charging current of output capacitor is discontinuous which require large filter size.

Applications :-

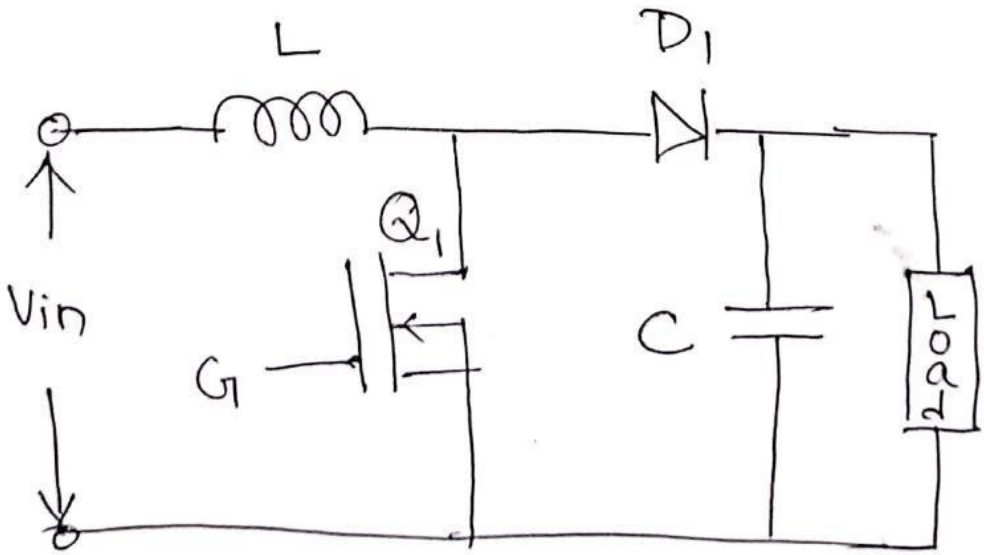
* Used to drive high current loads, used in Pc's, mother board.
* Battery chargers
* Solar chargers.

7. Discuss the modes of operation of Boost Converter, draw its waveform and Derive the equation for output voltage.

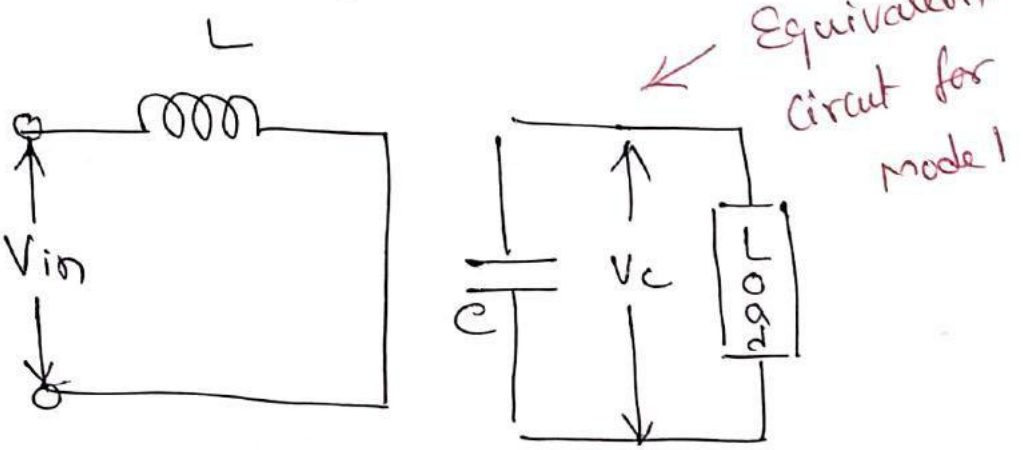
Boost Converter / Regulator :-

The Boost regulator Produces an output voltage greater than input voltage.

The figure shows the Circuit diagram of boost regulator using Power MOSFET. The Circuit operation has 2 Modes.

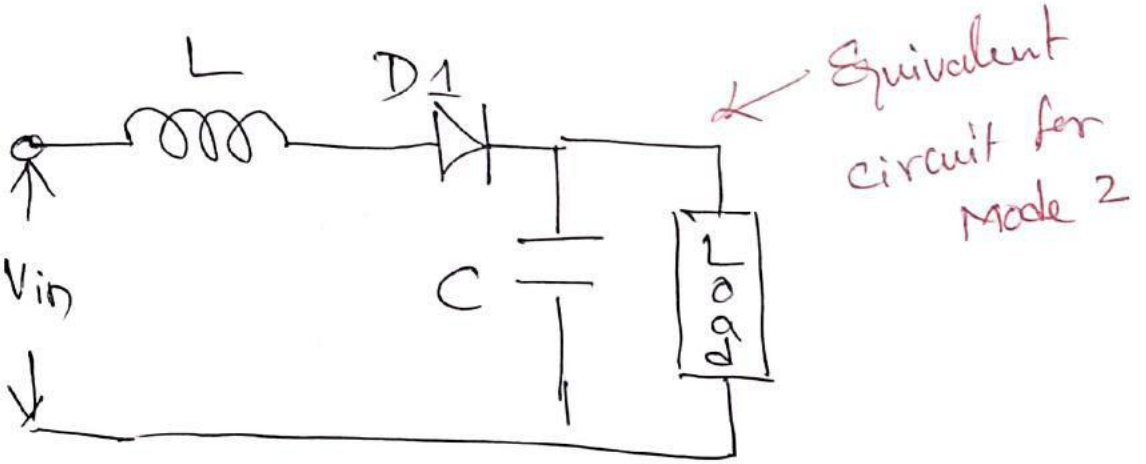


Mode 1 :- During Q_1 is "ON"



In mode1 inductor L is charge with input voltage Vin.

Mode 2 :- During Q_1 is "OFF"



In mode 2 inductor L is discharge to load

$$V_{in} = \frac{L(I_2 - I_1)}{t_1} = \frac{L\Delta I}{t_1} \quad \text{— (1)}$$

$$t_1 = \frac{L\,\Delta I}{V_{in}} \qquad \text{——— (2)}$$

$$\Delta I = \frac{V_{in}\,t_1}{L} \qquad \text{——— (3)}$$

at time t_2 the inductor current falls linearly from I_2 to I_1

$$V_a - V_{in} = \frac{L\,\Delta I}{t_2} \qquad \text{——— (4)}$$

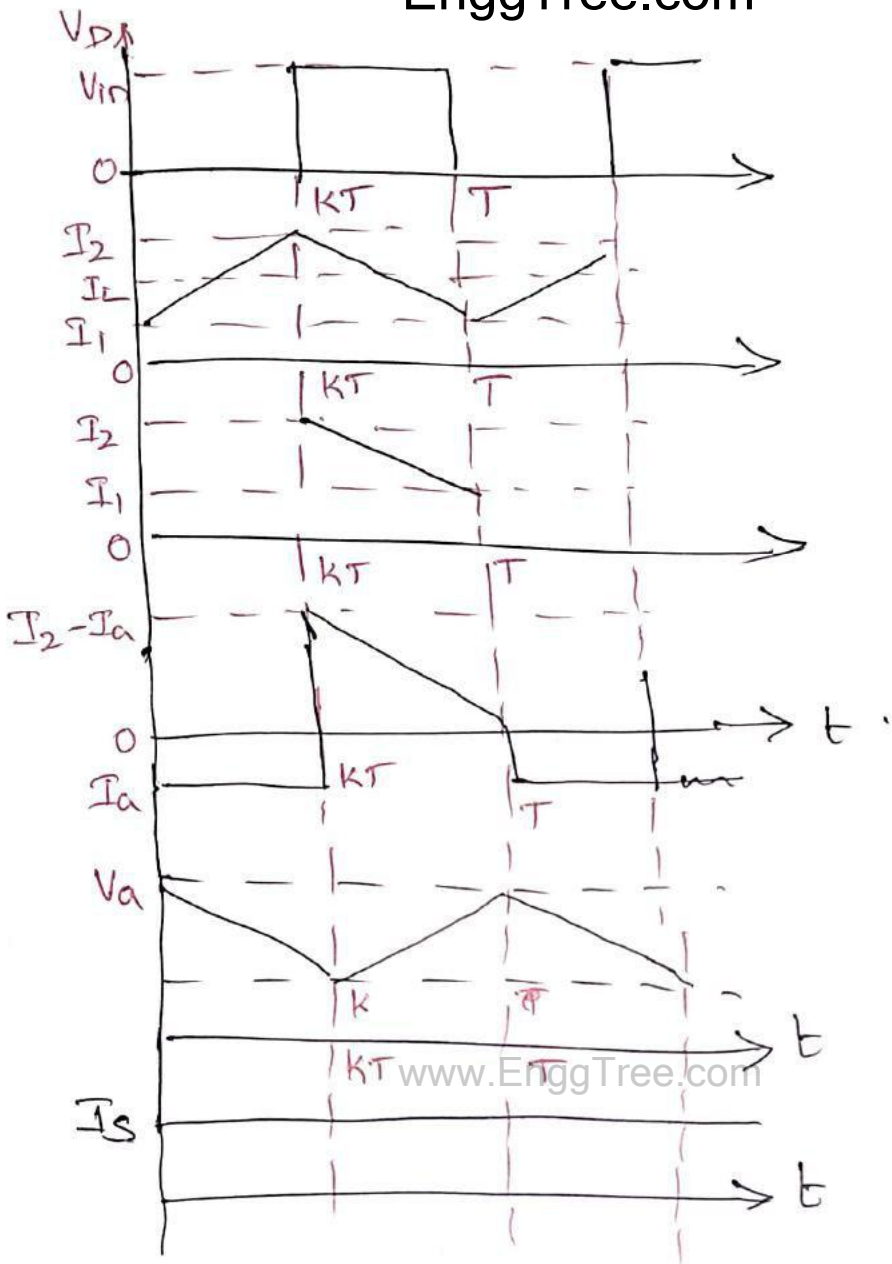
$$t_2 = \frac{L\,\Delta I}{V_a - V_{in}} \qquad \text{——— (5)}$$

$$\Delta I = \frac{t_2\,(V_a - V_{in})}{L} \qquad \text{——— (6)}$$

equating (3) and (6)

$$\Delta I = \frac{V_{in}\,t_1}{L} = \frac{t_2\,(V_a - V_{in})}{L}$$

$$V_{in}\,t_1 = t_2\,(V_a - V_{in})$$



Sub $t_1 = kT$ and $t_2 = (1-k)T$

$$V_{in}\, kT = (V_a - V_{in})(1-k)T$$

$$V_{in}kT = V_aT - V_{in}T \Rightarrow V_akT + V_{in}kT$$

$$V_{in}T = V_aT(1-k)$$

$$V_a = \frac{V_{in}}{1-k}$$

Advantages o/o

* No transformer required
* High efficiency due to single transistor
* Input current is continuous which is very desirable for sources like battery.

Disadvantages o/o

* output voltage is very sensitive to variations in the duty cycle k and is difficult to stabilize the regulator.
* It is difficult to protect the output circuit in case of short circuit as the transistor is connected in shunt with the load
* Requires large filte capacitor & inductor.
* There is no isolation from input to output

Applications o/o

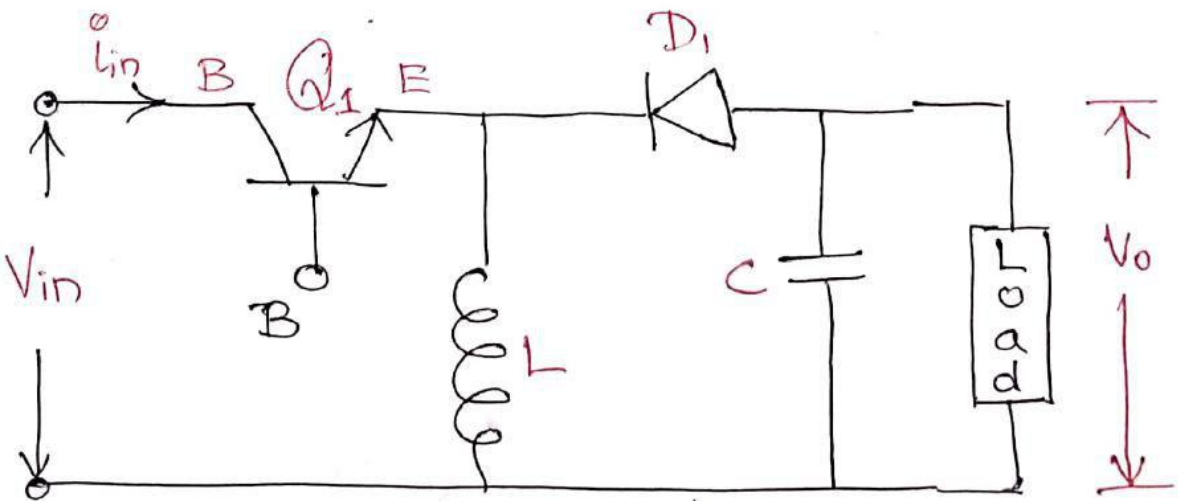
* Hybrid electric vehicles
* Lighting systems

8. Explain the operation of Buck-Boost Converter in detail.

Buck - Boost Converter :-

A Buck-Boost Converter Produces an output voltage which may be less than (or) greater than the input voltage.

The Polarity of output voltage is oppositetothat of input voltage. So this regulator is also known as inverting (or) flyback regulator.

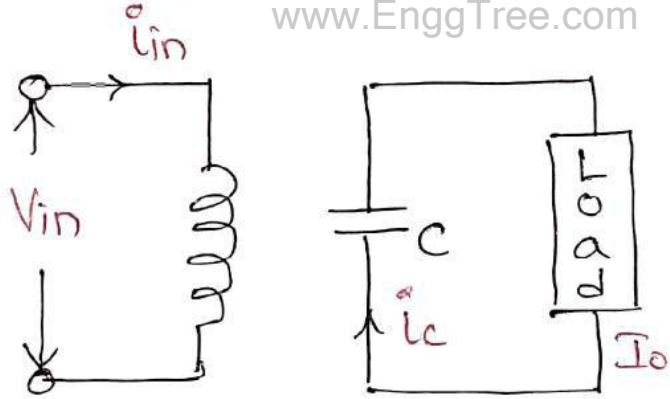


Buck-Boost Converter

Transistor Q_1 act as Switch. Diode is Connected in Series with the load. The inductor L is Connected in parallel after the Switch and before the diode. A Capacitor C is Connected in Parallel with load.

The Circuit operation is divided into two modes.

Mode 1 :-

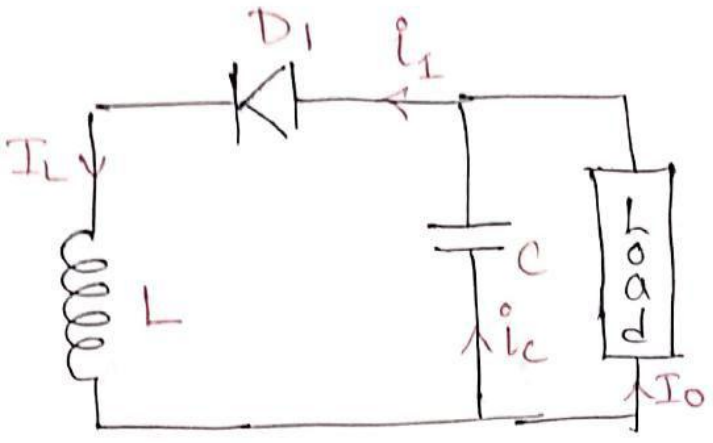


Q_1 is turned "ON" and D_1 is reverse biased. The input current increases and flows through inductor L and transistor Q_1

Mode 2 :-

Q_1 is Switched "OFF"

i) Current flowing through L will flow through L, C, D_1 and load.



ii) The energy stored in inductor L will be transferred to the load and the inductor current will fall until Q_1 is switched "ON" again in the next cycle.

$$V_{in} = L\left[\frac{i_2 - i_1}{t_1}\right] = L\frac{\Delta I}{t_1} \quad \text{——— (1)}$$

$$t_1 = \frac{L\Delta I}{V_{in}} \quad \text{——— (2)}$$

$$\Delta I = \frac{t_1 V_{in}}{L} \quad \text{——— (3)}$$

$$V_a = -\frac{L\Delta I}{t_2} \quad \text{——— (4)}$$

$$t_2 = -\frac{L\Delta I}{V_a} \quad \text{——— (5)}$$

$$\Delta I = \frac{-t_2 V_a}{L} \quad \text{——— (6)}$$

equating equ (3) and (6)

$$\Delta I = \frac{V_{in} t_1}{L} = \frac{-V_a t_2}{L}$$

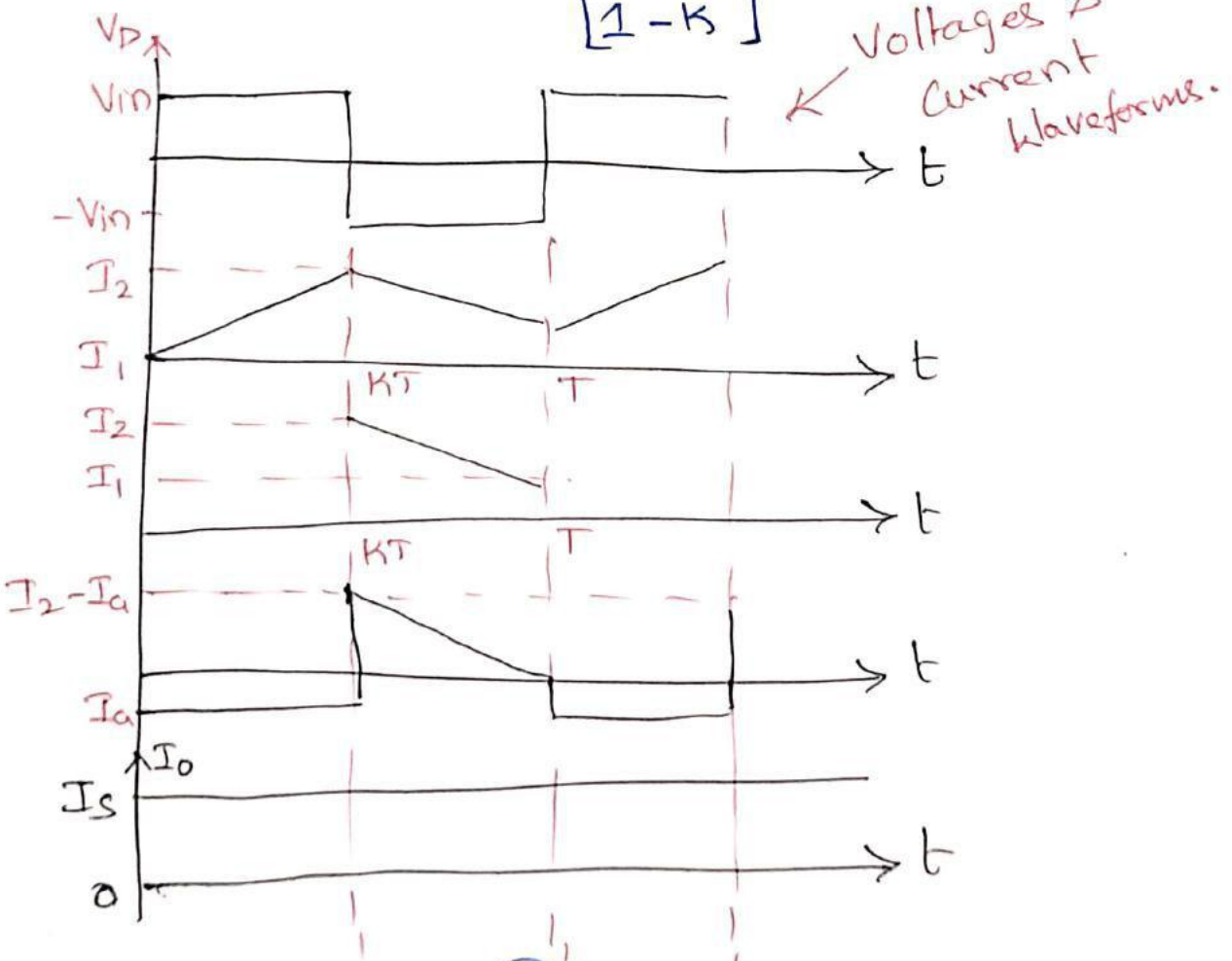
$$V_{in} t_1 = -V_a t_2$$

$t_1 = kT$ and $t_2 = (1-k)T$

$$V_{in} kT = -V_a (1-k) T$$

$$V_{in} k = -V_a - k V_a$$

$$V_a = -V_{in}\left[\frac{k}{1-k}\right]$$



Advantages :-

* A buck-boost regulator does not use a transformer
* High efficiency
* Easy to implement Short-Circuit Protection.
* Less expensive.

Disadvantages :-

* Input Current is discontinuous and high Peak Current flows through transistor Q1
* Slow response to fast load steps
* As Sensed voltage is negative inverting op-amp is required for feedback and closed loop control.
* No isolation between input and output.