Reg. No. : | E | N | G | G | T | R | E | E | . | C | O | M |

Question Paper Code : 30138

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2023.

Third Semester

Electronics and Communication Engineering

EC 3352 — DIGITAL SYSTEMS DESIGN

(Common to Electronics and Telecommunication Engineering)

(Regulations 2021)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert the decimal number 431 to binary.
2. State DeMorgan's theorem.
3. What is an encoder?
4. State the difference between parity generator and parity checker.
5. How are the outputs of Mealy model and Moore model decided?
6. What is a universal shift register?
7. When does a race condition exist in an asynchronous sequential circuit?
8. What is the cause of an essential hazard?
9. Define noise margin.
10. List the types of ROMs with their expansion.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Simplify the Boolean function $(BC'+A'D)(AB'+CD')$ to a minimum number of literals. (6)

(ii) Express the following function as a sum of minterms and as a product of maxterms:

$F(A,B,C,D) = B'D + A'D + BD$ (4 + 3)

Or

(b) Simplify the following function using Karnaugh map and implement it with two level NOR gate circuits. $F = wx' + y'z' + w'yz'$. (13)

12. (a) Implement a full adder with two half adders and an OR gate by deriving Boolean expression from its truth table and draw the logic circuit. (13)

Or

(b) Implement the following function with a multiplexer.

$F(A,B,C,D) = \Sigma(0,2,5,8,10,14)$ (13)

13. (a) Explain the principle of JK flip flop with logic diagram, graphic symbol, characteristic table, and characteristic equation. (13)

Or

(b) Describe the principle of BCD ripple counter with state diagram and logic diagram. (13)

14. (a) Find a critical race-free state assignment for the reduced flow table shown in Figure Q 14 (a). (13)

	00	01	11	10
a	(a)	d	(a)	c
b	a	(b)	(b)	d
c	d	(c)	b	(c)
d	(d)	(d)	(e)	(d)
e	f	c	(e)	c
f	(f)	b	a	(f)

Figure 14 (a).

Or

(b) Describe various types of hazards and the methods to eliminate hazards in combinational and sequential circuits. (13)

15. (a) (i) Draw and explain CMOS logic circuits. (7)

(ii) Explain a TTL gate with totem pole output. (6)

Or

(b) (i) Using 64 × 8 ROM chips with an enable input, construct a 512 × 8 ROM with 8 chips and a decoder. (7)

(ii) Draw a PLA circuit to implement the functions (6)

$F_1 = A'B + AC + A'BC'$

$F_2 = (AC + AB + BC)$

PART C — (1 × 15 = 15 marks)

16. (a) Simplify the following Boolean function by using the tabulation method.

$F = \Sigma(0,1,2,8,10,11,14,15)$ (15)

Or

(b) A sequential circuit has two JK flip flops A and B and one input X. The circuit is described by the following flip flop input equations.

$J_A = x \qquad K_A = B$

$J_B = x \qquad K_B = A'$

(i) Derive the state equations A (t + 1) and B (t + 1) by substituting the input equations for the J and K variables. (8)

(ii) Draw the state diagram of the circuit. (7)