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Question Paper Code : 50958

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2024.

Third Semester

Electronics and Communication Engineering

EC 3352 – DIGITAL SYSTEMS DESIGN

(Common to Electronics and Telecommunication Engineering)

(Regulations 2021)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. A and B are integer variables in a computer program, with A = $(25)_{10}$ and B = $-(46)_{10}$. Assuming that the computer uses 8-bit two's complement arithmetic, show how it would compute A – B, B – A and –A – B.

2. Draw the logic diagram using only two input NAND gates to implement the following expression F = (AB + A'B') (CD' + C'D).

3. A network router connects multiple computers together and allows them to send messages to each other. If two or more computers send message simultaneously, they collide and the messages must be resent. Implement a collision detection circuit using discrete ICs for a router that connects 3 computers.

4. Obtain the logic circuit diagram for a one bit magnitude comparator.

5. Design a 4-bit serial adder.

6. Draw the state diagram for moore model based sequence detector to detect the sequence 101 with one bit overlap.

7. Distinguish stable and unstable states.

8. What is pulse mode sequential circuit?

9. Construct an open-collector TTL 3-input NAND gate.

10. Show the memory cycle timing waveform for the memory read operation.

PART B — (5 × 13 = 65 marks)

11. (a) Develop a minimized Boolean implementation of a "ones count" circuit that works as follows. The subsystem has four inputs A, B, C, D and generates a 3-bit output : XYZ . XYZ is 000 if none of the inputs are 1, 001 if one input is 1,010 if two inputs are 1, 011 if three inputs are 1 and 100 if all four inputs are 1.

Or

(b) Using Karnaugh map method, simplify the following Boolean function.

$F(A, B, C, D) = \Sigma m(4, 6, 7, 13, 14) + d(5, 10, 12, 15)$

12. (a) Design a 4-bit adder that should have a computational complexity of O(1).

Or

(b) Develop the truth table and deduce a logic circuit for the BCD to seven segment display decoder using common anode LEDs.

13. (a) Design a synchronous counter that counts as 000, 010, 101, 110, 000, 101, ... Ensure that unused states of 001, 011, 100 and 111 go to 000 on next clock pulse. Use J-K flip-flops. How will the counter hardware look like if the unused states are to be considered as "don't cares"?

Or

(b) Design a pulse train generator using a shift register to generate the following sequence 10111101011110....

14. (a) An asynchronous sequential circuit has two internal states and one output. The excitation and output functions describing the circuit are as follows :

$Y_1 = x_1x_2 + x_1y_2' + x_2'y_1$

$Y_2 = x_2 + x_1y_1'y_2 + x_1'y_1$

$z = x_2 + y_1$

(i) Draw the logic diagram of the circuit. (3)

(ii) Derive the transition table and output map. (5)

(iii) Obtain a flow table for the circuit. (5)

Or

(b) For the reduced flow table shown in Fig. 1 obtain a binary state assignment without critical race conditions. Also obtain the logic diagram of the circuit using NAND latches and gates.

	x_1x_2 = 00	01	11	10
a	ⓐ, 0	ⓐ, 1	b, –	d, –
b	a, –	ⓑ, 0	ⓑ, 0	c, –
c	a, –	–, –	d, –	ⓒ, 0
d	a, –	a, –	ⓓ, 1	ⓓ, 1

Fig. 1

15. (a) The following are the specifications of the Schottky TTL 74LS00 quadruple 2-input NAND gates. Calculate the fan-out, power dissipation, propagation delay and noise margin of the Schottky NAND gate.

Parameter	Name	Value
V_{CC}	Supply voltage	5V
I_{CCH}	High-level supply current (four gates)	10mA
I_{CCL}	Low-level supply current (four gates)	20mA
V_{OH}	High-level output voltage (min)	2.7V
V_{OL}	Low-level output voltage (max)	0.5V
V_{IH}	High-level input voltage(min)	2V
V_{IL}	Low-level input voltage(max)	0.8V
I_{OH}	High-level output current(max)	1mA
I_{OL}	Low-level output current(max)	20mA
I_{IH}	High-level input current(max)	0.05mA
I_{IL}	Low-level input current(max)	2mA
t_{PLH}	Low-to-High delay	3 ns
t_{PHI}	High-to-low delay	3 ns

Or

(b) Obtain a BCD to excess-3 code converter using PLA program table.

PART C — (1 × 15 = 15 marks)

16. (a) Deduce the logic diagram for the state diagram shown in Fig. 2 using one hot encoding method. Compare the hardware implementation resources with binary encoding method.

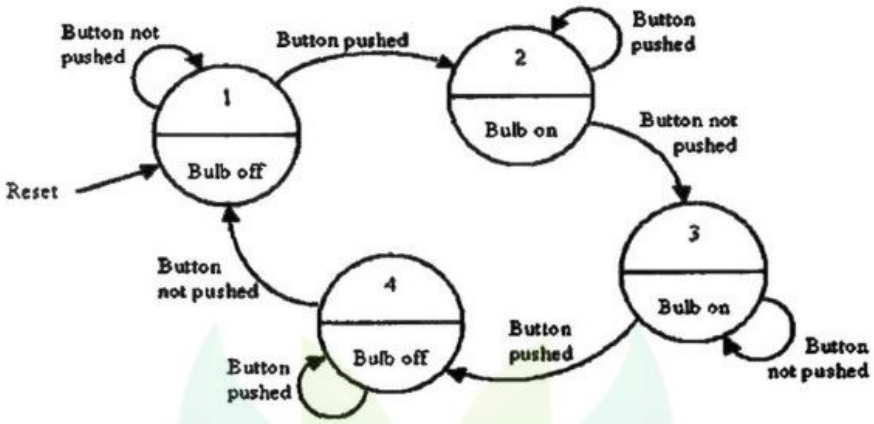

Fig. 2

Or

(b) Design a circuit that controls the elevator door in a three story building as given in Fig. 3. Let M is a logic signal that indicates the elevator is moving (M = 1) or stopped (M = 0). F1, F2 and F3 are floor indicator signals that are normally LOW, and they go HIGH only when the elevator is positioned at that particular floor. For example, when the elevator is lined with second floor where M = 0, F2 = 1 and F1 = F3 = 0. The circuit output is OPEN which is identified as "Low" when moving and will go "HIGH" when the elevator door is to be opened at the particular floor. Since the elevator cannot be lined up with more than one floor at a time, only one of the floor inputs can be HIGH at any given time. This means that all those cases in the truth table where more than one floor input is a 1 are assumed to be don't care conditions. Obtain the simplified expression using K-Map and draw the logic diagram for the expression.

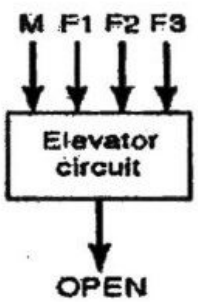

Fig. 3